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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e3016seg

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

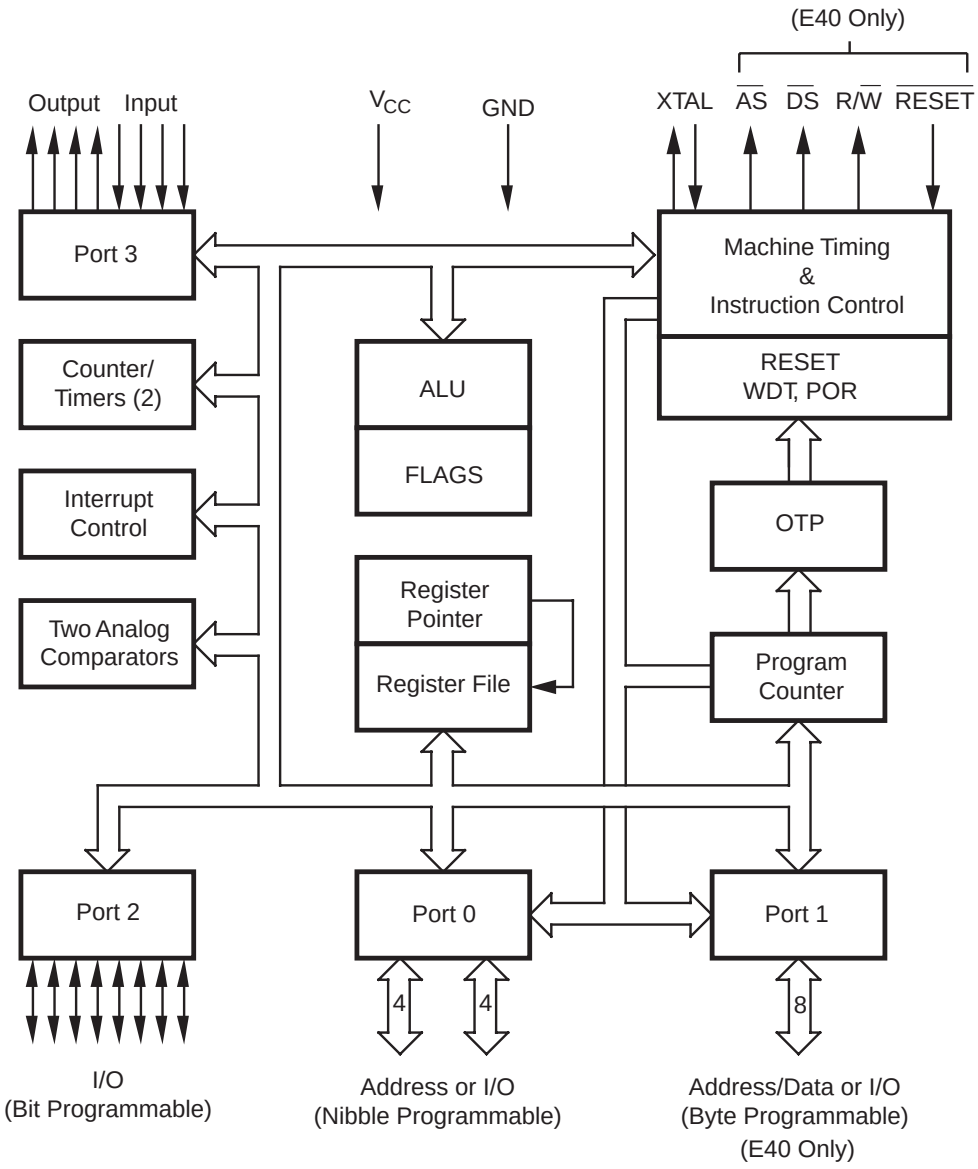


Figure 1. Z86E30/E31/E40 Functional Block Diagram

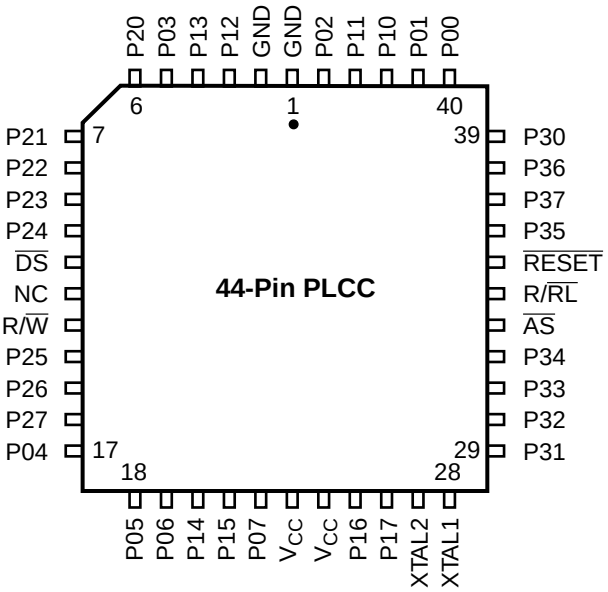


Figure 4. 44-Pin PLCC Pin Configuration
Standard Mode

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1–2	GND	Ground	
3–4	P12–P13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6–10	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output
11	$\overline{DS}$	Data Strobe	Output
12	NC	No Connection	
13	R/$\overline{W}$	Read/Write	Output
14–16	P25–P27	Port 2, Pins 5,6,7	In/Output
17–19	P04–P06	Port 0, Pins 4,5,6	In/Output
20–21	P14–P15	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23–24	V_{CC}	Power Supply	
25–26	P16–P17	Port 1, Pins 6,7	In/Output
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29–31	P31–P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
33	$\overline{AS}$	Address Strobe	Output
34	R/$\overline{RL}$	ROM/ROMless select	Input
35	$\overline{RESET}$	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40–41	P00–P01	Port 0, Pins 0,1	In/Output
42–43	P10–P11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

			T_A= 0 °C to +70 °C					
Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V 5.5V	0.7 V_{CC} 0.7 V_{CC}	V_{CC}+0.3 V_{CC}+0.3	1.8 2.5	V V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V 4.5V	GND -0.3 GND -0.3	0.2 V_{CC} 0.2 V_{CC}	0.9 1.5	V V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V 5.5V	0.7 V_{CC} 0.7 V_{CC}	V_{CC}+0.3 V_{CC}+0.3	2.5 2.5	V V		
V_{IL}	Input Low Voltage	3.5V 5.5V	GND -0.3 GND -0.3	0.2 V_{CC} 0.2 V_{CC}	1.5 1.5	V V		
V_{OH}	Output High Voltage Low EMI Mode	3.5V 5.5V	V_{CC} -0.4 V_{CC} -0.4		3.3 4.8	V V	I_{OH} = – 0.5 mA	
V_{OH1}	Output High Voltage	3.5V 5.5V	V_{CC} -0.4 V_{CC} -0.4		3.3 4.8	V V	I_{OH} = -2.0 mA I_{OH} = -2.0 mA	
V_{OL}	Output Low Voltage Low EMI Mode	3.5V 4.5V		0.4 0.4	0.2 0.2	V V	I_{OL} = 1.0 mA I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	3.5V 4.5V		0.4 0.4	0.1 0.1	V V	I_{OL} = + 4.0 mA I_{OL} = + 4.0 mA	8 8
V_{OL2}	Output Low Voltage	3.5V 4.5V		1.2 1.2	0.5 0.5	V V	I_{OL} = + 12 mA I_{OL} = + 12 mA	8 8
V_{RH}	Reset Input High Voltage	3.5V 5.5V	.8 V_{CC} .8 V_{CC}	V_{CC} V_{CC}	1.7 2.1	V V		
V_{RL}	Reset Input Low Voltage	3.5V 5.5V	GND -0.3 GND -0.3	0.2 V_{CC} 0.2 V_{CC}	1.3 1.7	V V		13
V_{OLR}	Reset Output Low Voltage	3.5V 5.5V		0.6 0.6	0.3 0.2	V V	I_{OL} = 1.0 mA I_{OL} = 1.0 mA	
V_{OFFSET}	Comparator Input Offset Voltage	3.5V 4.5V		25 25	10 10	mV mV		
V_{ICR}	Input Common Mode Voltage Range	3.5V 5.5V	0 0	V_{CC} -1.0V V_{CC} -1.0V		V V		10 10
I_{IL}	Input Leakage	3.5V 4.5V	-1 -1	2 2	0.032 0.032	µA µA	V_{IN} = 0V, V_{CC} V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V 4.5V	-1 -1	2 2	0.032 0.032	µA µA	V_{IN} = 0V, V_{CC} V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.5V 4.5V	-20 -20	-130 -180	-65 -112	µA µA		

Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
			T_A=–40 °C to +105 °C					
V_{CH}	Clock Input High Voltage	4.5V 5.5V	0.7 V_{CC} 0.7 V_{CC}	V_{CC}+0.3 V_{CC}+0.3	2.5 2.5	V V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V 5.5V	GND-0.3 GND-0.3	0.2 V_{CC} 0.2 V_{CC}	1.5 1.5	V V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V 5.5V	0.7 V_{CC} 0.7 V_{CC}	V_{CC}+0.3 V_{CC}+0.3	2.5 2.5	V V		
V_{IL}	Input Low Voltage	4.5V 5.5V	GND-0.3 GND-0.3	0.2 V_{CC} 0.2 V_{CC}	1.5 1.5	V V		
V_{OH}	Output High Voltage Low EMI Mode	4.5V 5.5V	V_{CC} -0.4 V_{CC} -0.4		4.8 4.8	V V	I_{OH} = – 0.5 mA I_{OH} = – 0.5 mA	8 8
V_{OH1}	Output High Voltage	4.5V 4.5V	V_{CC} -0.4 V_{CC} -0.4		4.8 4.8	V V	I_{OH} = -2.0 mA I_{OH} = -2.0 mA	8 8
V_{OL}	Output Low Voltage Low EMI Mode	4.5V 5.5V		0.4 0.4	0.2 0.2	V V	I_{OL} = 1.0 mA I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	4.5V 5.5V		0.4 0.4	0.1 0.1	V V	I_{OL} = + 4.0 mA I_{OL} = +4.0 mA	8 8
V_{OL2}	Output Low Voltage	4.5V 5.5V		1.2 1.2	0.5 0.5	V V	I_{OL} = + 12 mA I_{OL} = + 12 mA	8 8
V_{RH}	Reset Input High Voltage	3.5V 5.5V	.8 V_{CC} .8 V_{CC}	V_{CC} V_{CC}	1.7 2.1	V V		13 13
V_{OLR}	Reset Output Low Voltage	3.5V 5.5V		0.6 0.6	0.3 0.2	V V	I_{OL} = 1.0 mA I_{OL} = 1.0 mA	13 13
V_{OFFSET}	Comparator Input Offset Voltage	4.5V 5.5V		25 25	10 10	mV mV		
V_{ICR}	Input Common Mode Voltage Range	4.5V 5.5V	0 0	V_{CC}-1.5V V_{CC}-1.5V		V V		10 10
I_{IL}	Input Leakage	4.5V 5.5V	-1 -1	2 2	<1 <1	µA µA	V_{IN} = 0V, V_{CC} V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V 5.5V	-1 -1	2 2	<1 <1	µA µA	V_{IN} = 0V, V_{CC} V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	4.5V 5.5V	-18 -18	-180 -180	-112 -112	µA µA		
I_{CC}	Supply Current	4.5V 5.5V		25 25	20 20	mA mA	@ 16 MHz @ 16 MHz	4,5 4,5
I_{CC1}	Standby Current Halt Mode	4.5V 5.5V		8 8	3.7 3.7	mA mA	V_{IN} = 0V, V_{CC} @ 16 MHz V_{IN} = 0V, V_{CC} @ 16 MHz	4,5 4,5
I_{CC2}	Standby Current (Stop Mode)	4.5V 5.5V		10 10	2 3	µA µA	V_{IN} = 0V, V_{CC} V_{IN} = 0V, V_{CC}	6,11,14 6,11,14
I_{ALL}	Auto Latch Low Current	4.5V 5.5V	1.4 1.4	20 20	4.7 4.7	µA µA	0V < V_{IN} < V_{CC} 0V < V_{IN} < V_{CC}	9 9

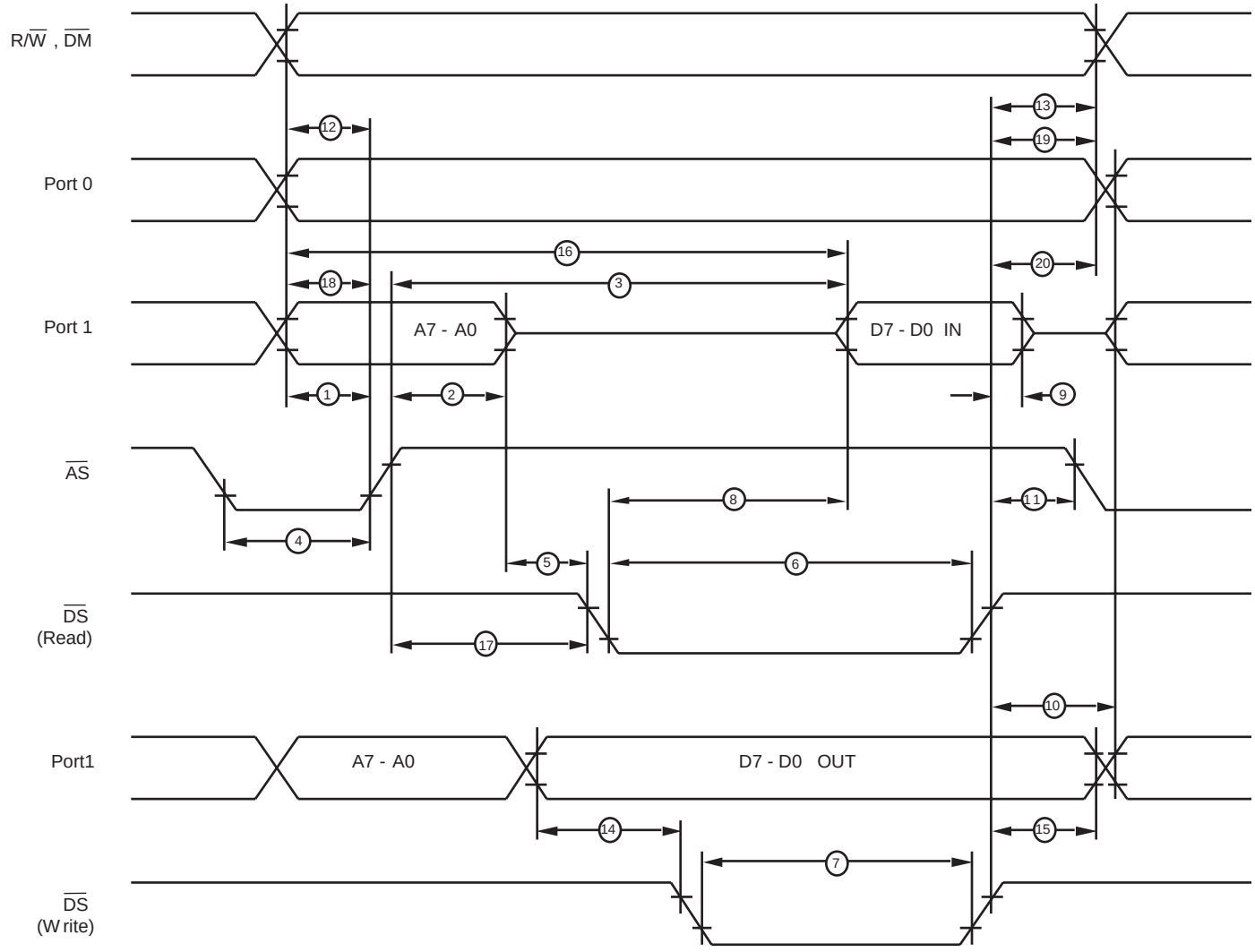


Figure 14. External I/O or Memory Read/Write Timing
Z86E40 Only

			T_A = -40°C to 105°C 16 MHz Note [3]				
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	4.5V 5.5V	25 25		ns ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	4.5V 5.5V	35 35		ns ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	4.5V 5.5V		180 180	ns ns	1,2
4	TwAS	$\overline{AS}$ Low Width	4.5V 5.5V	40 40		ns ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	4.5V 5.5V	0 0		ns ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	4.5V 5.5V	135 135		ns ns	1,2
7	TwDSW	$\overline{DS}$ (Write) Low Width	4.5V 5.5V	80 80		ns ns	1,2
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid	4.5V 5.5V		75 75	ns ns	1,2
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	4.5V 5.5V	0 0		ns ns	2
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	4.5V 5.5V	50 50		ns ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	4.5V 5.5V	35 35		ns ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	4.5V 5.5V	25 25		ns ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	4.5V 5.5V	35 35		ns ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	4.5V 5.5V	55 55	25 25	ns ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	4.5V 5.5V	35 35		ns ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	4.5V 5.5V		230 230	ns ns	1,2
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	4.5V 5.5V	45 45		ns ns	2
18	TdDM(AS)	/DM Valid to $\overline{AS}$ Fall Delay	4.5V 5.5V	30 30		ns ns	2
20	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	4.5V 5.5V	35 35		ns ns	

Notes:

1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

Additional Timing Table (Divide-By-One Mode)

				T_A = 0 °C to +70 °C		T_A = -40 °C to +105 °C			
				4 MHz		4 MHz			
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.5V	250	DC	250	DC	ns	1,7,8
			5.5V	250	DC	250	DC	ns	1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		25		25	ns	1,7,8
			5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	3.5V	100		100		ns	1,7,8
			5.5V	100		100		ns	1,7,8
4	TwTinL	Timer Input Low Width	3.5V	100		100		ns	1,7,8
			5.5V	70		70		ns	1,7,8
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC			1,7,8
			5.5V	5TpC		5TpC			1,7,8
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC			1,7,8
			5.5V	8TpC		8TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns	1,7,8
			5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low Time	3.5V	100		100		ns	1,2,7,8
			5.5V	70		70		ns	1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC			1,3,7,8
			5.5V	5TpC		5TpC			1,3,7,8
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC			1,2,7,8
			5.5V	5TpC		5TpC			1,2,7,8
10	Twsm	STOP Mode Recovery Width Spec	3.5V	12		12		ns	4,8
			5.5V	12		12		ns	4,8
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC		4,8,9
			5.5V		5TpC				

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31–P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 1, POR STOP Mode Delay is on.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V and the V_{CC} voltage specification of 3.5V guarantees 3.5V only.
7. SMR D1 = 0.
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

PIN FUNCTIONS

EPROM Programming Mode

D7–D0 Data Bus. The data can be read from or written to external memory through the data bus.

A11–A0 Address Bus. During programming, the EPROM address is written to the address bus.

V_{CC} Power Supply. This pin must supply 5V during the EPROM read mode and 6V during other modes.

$\overline{CE}$ Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

$\overline{OE}$ Output Enable (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM EPROM Program Mode. This pin controls the different EPROM Program Mode by applying different voltages.

V_{PP} Program Voltage. This pin supplies the program voltage.

$\overline{PGM}$ Program Mode (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if excessive noise surges above V_{CC} occur on pins XTAL1 and $\overline{RESET}$.

In addition, processor operation of Z8 OTP devices may be affected by excessive noise surges on the V_{PP}, $\overline{CE}$, $\overline{EPM}$, $\overline{OE}$ pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{CC}
- Adding a capacitor to the affected pin

Standard Mode

XTAL Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network, or external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network to the on-chip oscillator output.

R/$\overline{W}$ Read/Write (output, write Low). The R/$\overline{W}$ signal is Low when the CCP is writing to the external program or data memory (Z86E40 only).

$\overline{RESET}$ Reset (input, active Low). Reset will initialize the MCU. Reset is accomplished either through Power-On, Watch-Dog Timer reset, STOP-Mode Recovery, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin low for the POR time. Any devices driving the reset line must be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. After the POR time, $\overline{RESET}$ is a Schmitt-triggered input.

To avoid asynchronous and noisy reset problems, the Z86E40 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. During the reset cycle, $\overline{DS}$ is held active Low while $\overline{AS}$ cycles at a rate of TpC/2. Program execution begins at location 000CH, 5–10 TpC cycles after $\overline{RESET}$ is released. For Power-On Reset, the reset output time is 5 ms. The Z86E40 does not reset WDTMR, SMR, P2M, and P3M registers on a STOP-Mode Recovery operation.

$\overline{ROMless}$ (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90/C89 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC}, the device functions normally as a Z8 ROM version).

Note: When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC}.

PIN FUNCTIONS (Continued)

Port 3 (P37–P30). Port 3 is an 8-bit, CMOS-compatible port with four fixed inputs (P33–P30) and four fixed outputs (P37–P34). These eight lines can be configured by software for interrupt and handshake control functions. Port 3, Pin 0 is Schmitt- triggered. P31, P32, and P33 are standard CMOS inputs with single trip point (no Auto Latches) and P34, P35, P36, and P37 are push-pull output lines. Low EMI output buffers can be globally programmed by the software. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by setting the D1 of Port 3 Mode Register (P3M). The comparator output can be outputted from P34 and P37, respectively, by setting PCON register Bit D0 to 1 state. For the interrupt function, P30 and P33 are falling edge triggered interrupt inputs. P31 and P32 can be programmed as falling, rising or both edges triggered interrupt inputs (Figure 21). Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Port 0, Port 1, and Port 2 are also available on Port 3 (Table 9).

Note: When enabling/ or disabling analog mode, the following is recommended:

1. Allow two NOP delays before reading this comparator output.
2. Disable global interrupts, switch to analog mode, clear interrupts, and then re-enable interrupts.
3. IRQ register bits 3 to 0 must be cleared after enabling analog mode.

Note: P33–P30 differs from the Z86C30/C31/C40 in that there is no clamping diode to V_{CC} due to the EPROM high-voltage circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode.

PIN FUNCTIONS (Continued)

Comparator Inputs. Port 3, P31, and P32, each have a comparator front end. The comparator reference voltage P33 is common to both comparators. In analog mode, P31 and P32 are the positive input of the comparators and P33 is the reference voltage of the comparators.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33–P31) that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Auto Latches are available on Port 0, Port 2, and P30. There are no Auto Latches on P31, P32, and P33.

Low EMI Emission. The Z86E40 can be programmed to operate in a low EMI Emission Mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Low EMI Oscillator.
- Internal SCLK/TCLK= XTAL operation limited to a maximum of 4 MHz – 250 ns cycle time, when Low EMI Oscillator is selected and system clock (SCLK = XTAL, SMR Reg. Bit D1 =1).
- **Note for emulation only:**
  Do not set the emulator to emulate Port 1 in low EMI mode. Port 1 must always be configured in Standard Mode.

FUNCTIONAL DESCRIPTION (Continued)

Data Memory ($\overline{DM}$). In EPROM Mode, the Z86E40 can address up to 60 KB of external data memory beginning at location 4096. In ROMless mode, the Z86E40 can address up to 64 KB of data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 23). The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory.

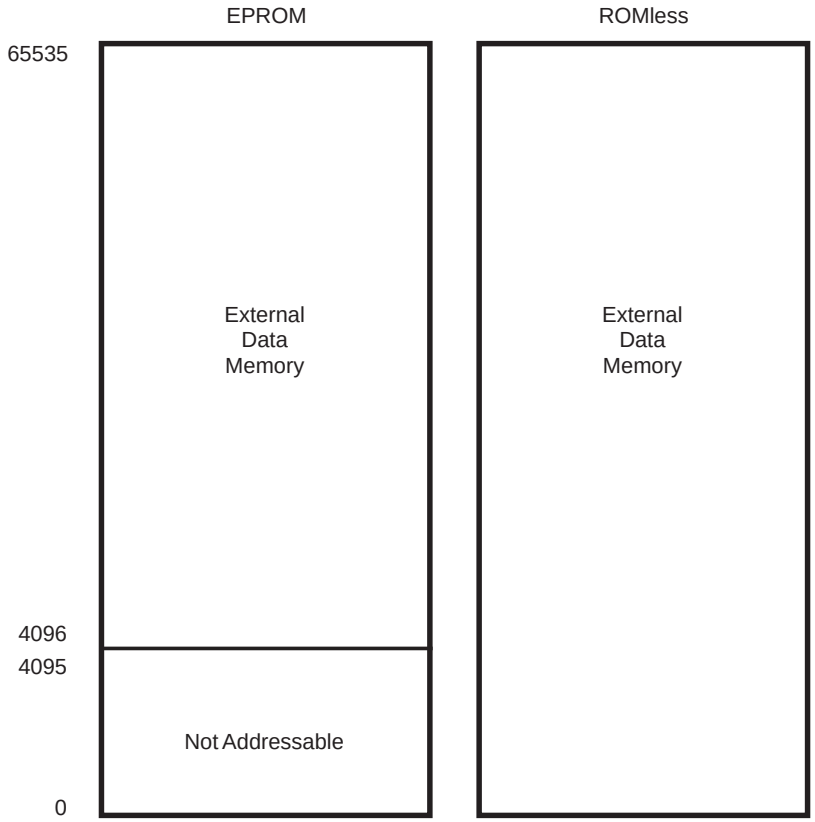


Figure 23. Data Memory Map

FUNCTIONAL DESCRIPTION (Continued)

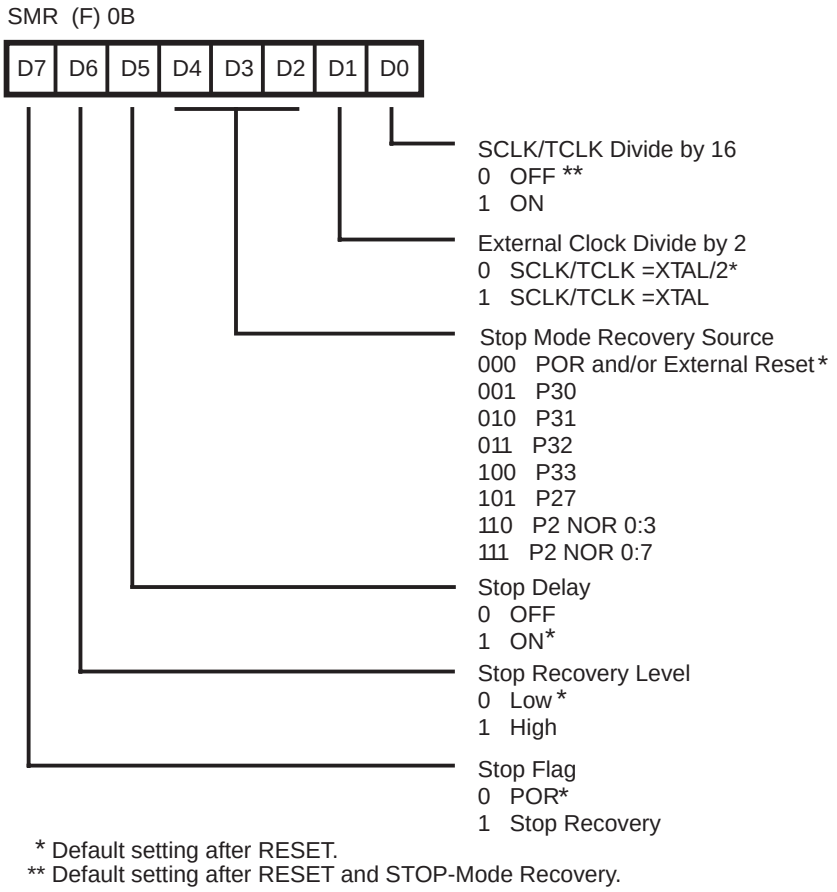


Figure 31. STOP-Mode Recovery Register (Write-Only Except Bit D7, Which is Read-Only)

SCLK/TCLK Divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (i.e., D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake up source of the STOP-Mode Recovery (Figure 32). Table 12 shows the SMR source selected with the setting of D2 to D4. P33–P31 cannot be used to wake up from STOP mode when programmed as analog inputs. When the STOP-Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: If the Port2 pin is configured as an output, this output level will be read by the SMR circuitry.

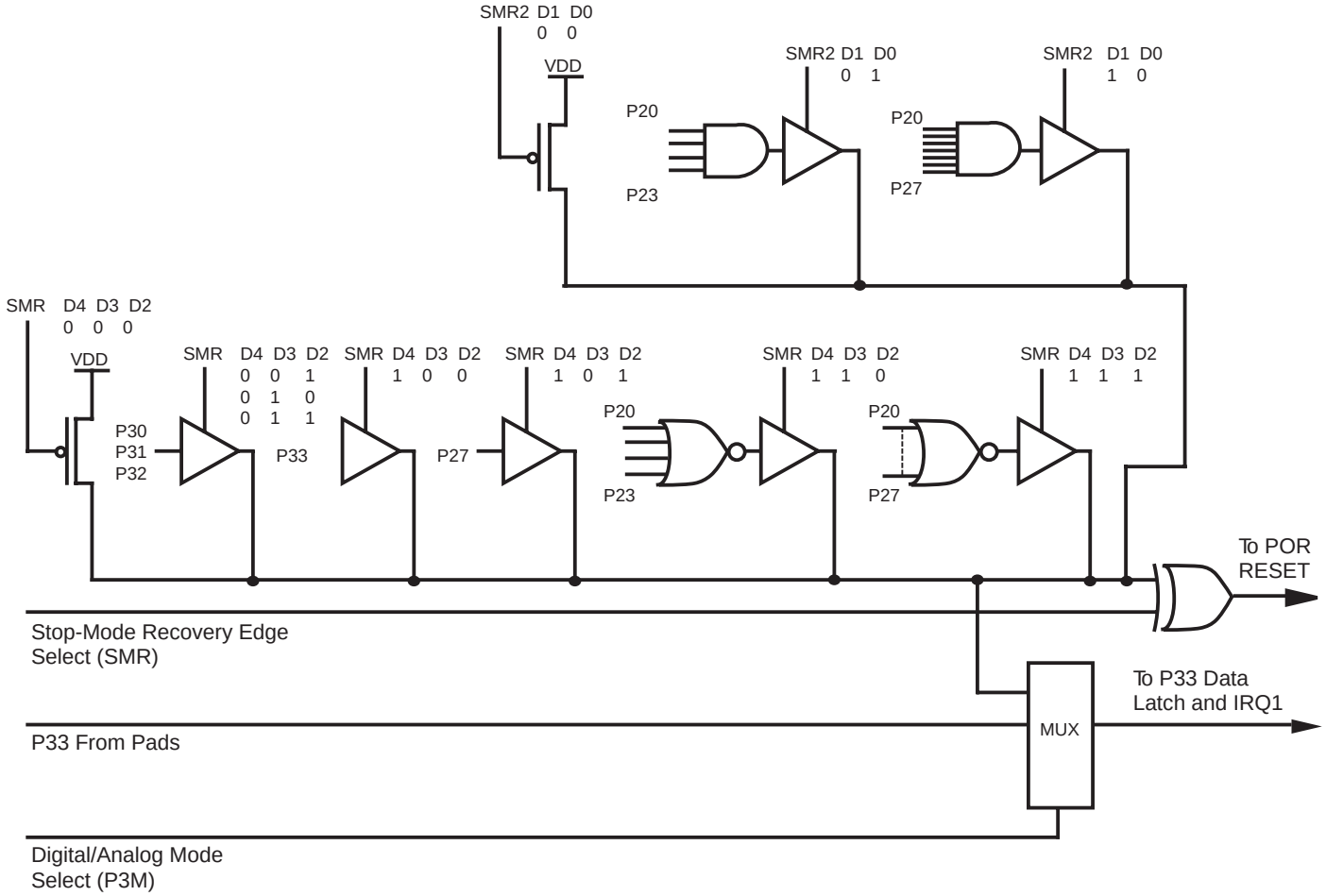


Figure 32. Stop-Mode Recovery Source

FUNCTIONAL DESCRIPTION (Continued)

Table 12. Stop-Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0–3
1	1	1	Logical NOR of Port 2 bits 0–7

Stop-Mode Recovery Delay Select (D5). The 5 ms RESET delay after Stop-Mode Recovery is disabled by programming this bit to a zero. A “1” in this bit will cause a 5 ms RESET delay after Stop-Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the Stop-Mode Recovery source needs to be kept active for at least 5TpC.

Stop-Mode Recovery Level Select (D6). A “1” in this bit defines that a high level on any one of the recovery sources wakes the MCU from STOP Mode. A 0 defines low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A “0” in this bit indicates that the device has been reset by POR (cold). A “1” in this bit indicates the device was awakened by a SMR source (warm).

Stop-Mode Recovery Register 2 (SMR2). This register contains additional Stop-Mode Recovery sources. When the Stop-Mode Recovery sources are selected in this register then SMR Register. Bits D2, D3, and D4 must be 0.

SMR:10		Operation
D1	**D0**	**Description of Action**
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is disabled after Power-On Reset and initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT is driven either by an on-board RC oscillator or an external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register.

Note: Execution of the WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags.

WDT Time-Out Period (D0 and D1). Bits 0 and 1 control a tap circuit that determines the time-out periods that can be obtained (Table 13). The default value of D0 and D1 are 1 and 0, respectively.

Table 13. Time-out Period of WDT

D1	D0	Time-out of the Internal RC OSC	Time-out of the System Clock
0	0	5 ms	128 SCLK
0	1	10 ms*	256 SCLK*
1	0	20 ms	512 SCLK
1	1	80 ms	2048 SCLK

Notes:
*The default setting is 10 ms.

WDT During HALT Mode (D2). This bit determines whether or not the WDT is active during HALT Mode. A “1” indicates that the WDT is active during HALT. A “0” disables the WDT in HALT Mode. The default value is “1”.

WDT During STOP Mode (D3). This bit determines whether or not the WDT is active during STOP mode. A “1” indicates active during STOP. A “0” disables the WDT during STOP Mode. This is applicable only when the WDT clock source is the internal RC oscillator.

Clock Source For WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1, and the WDT is stopped in STOP Mode. The default configuration of this bit is 0, which selects the RC oscillator.

Permanent WDT. When this feature is enabled, the WDT is enabled after reset and will operate in Run and Halt Mode. The control bits in the WDTMR do not affect the WDT operation. If the clock source of the WDT is the internal RC oscillator, then the WDT will run in STOP mode. If the clock source of the WDT is the XTAL1 pin, then the WDT will not run in STOP mode.

Note: WDT time-out in STOP Mode will not reset SMR,SMR2,PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers.

WDTMR Register Accessibility. The WDTMR register is accessible only during the **first 60** internal system clock

Z86E40 TIMING DIAGRAMS (Continued)

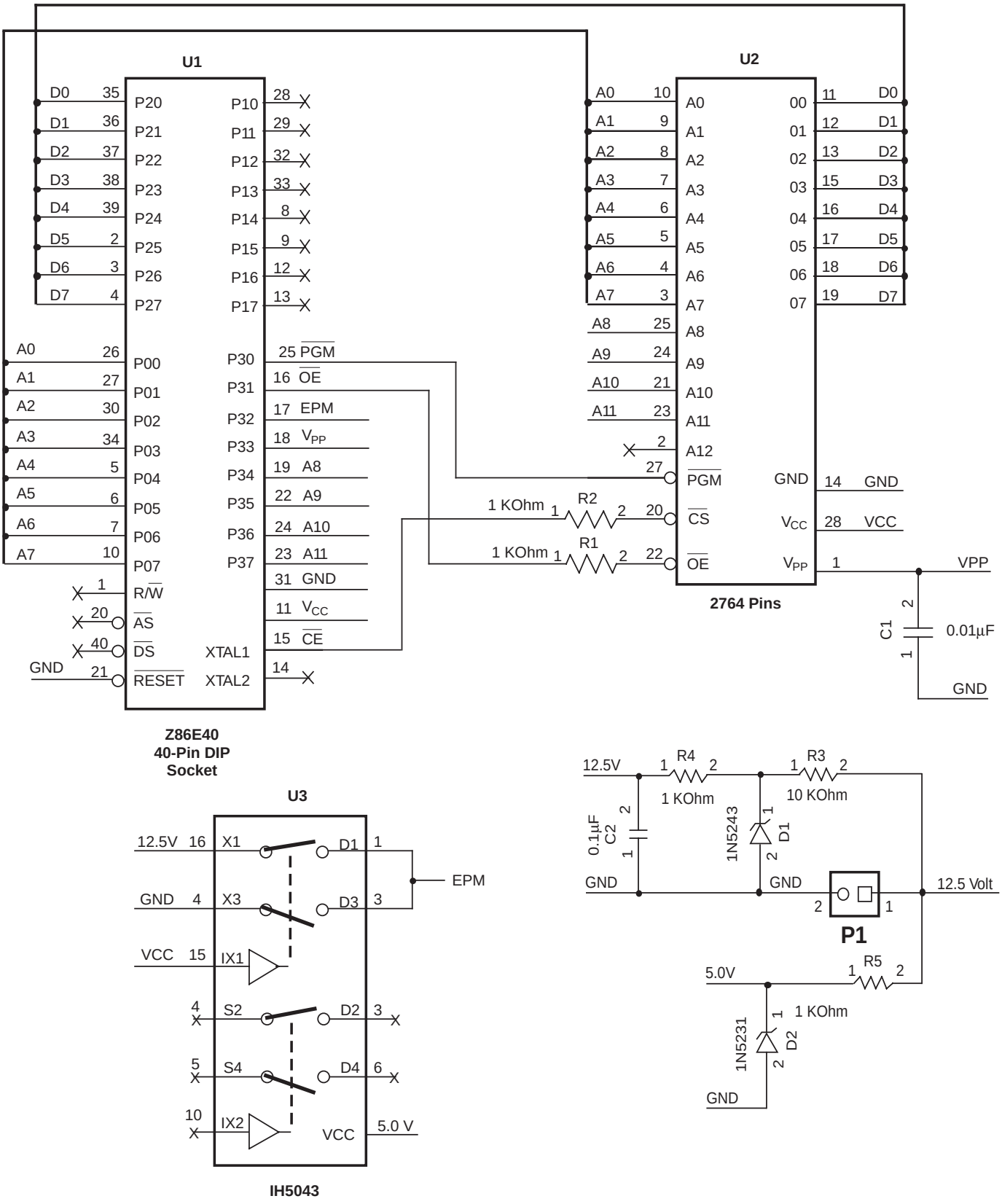


Figure 38. Z86E40 Z8 OTP Programming Adapter
For use with Standard EPROM Programmers

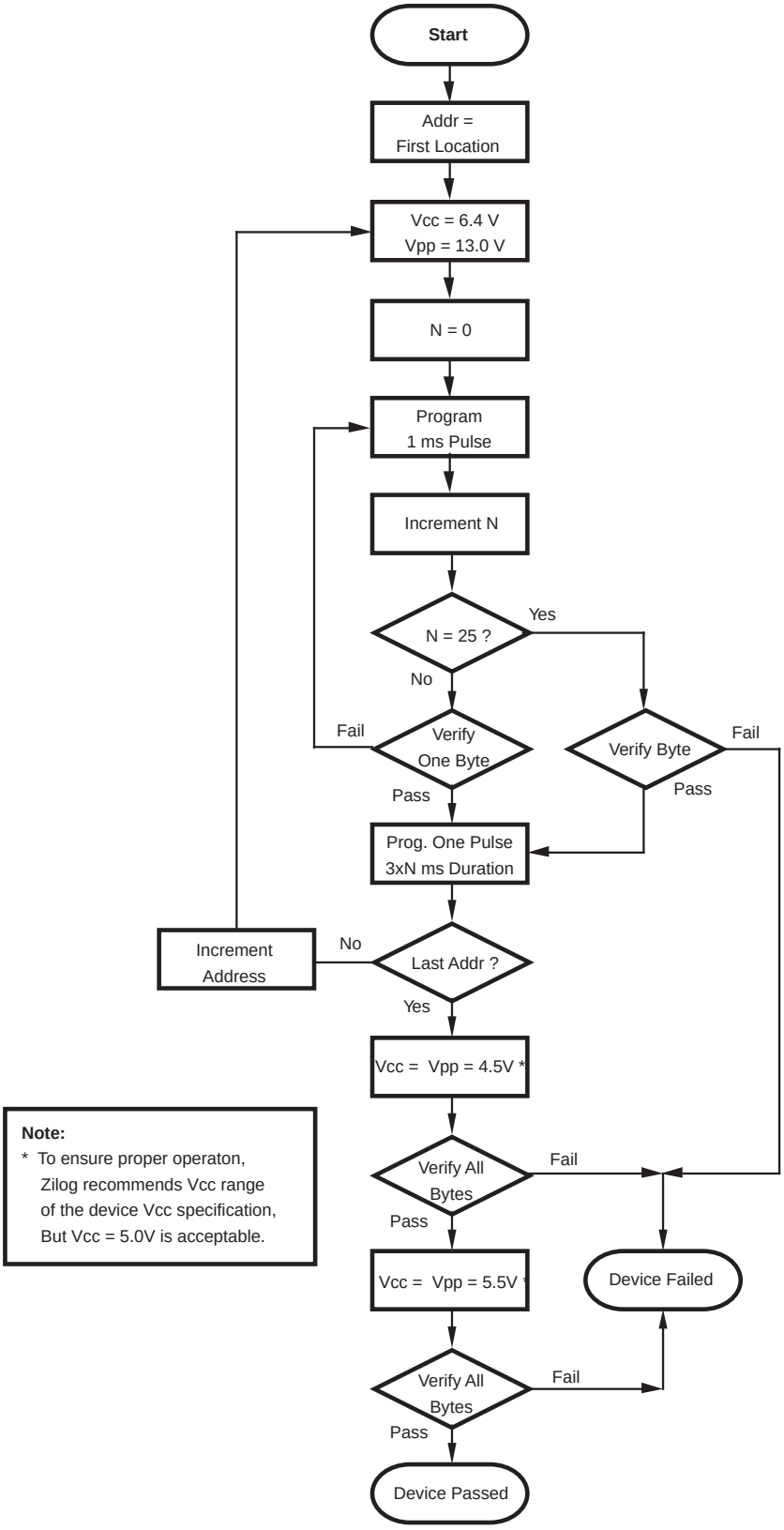


Figure 40. Z86E40 Programming Algorithm

EXPANDED REGISTER FILE CONTROL REGISTERS

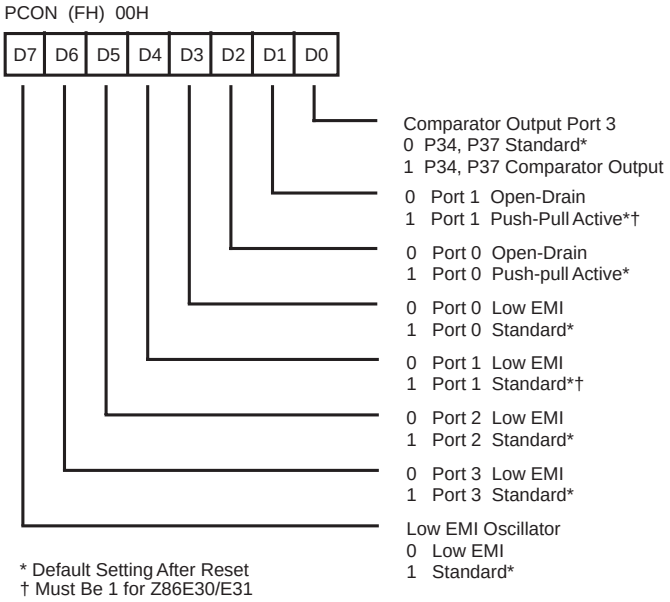


Figure 41. Port Configuration Register Write Only

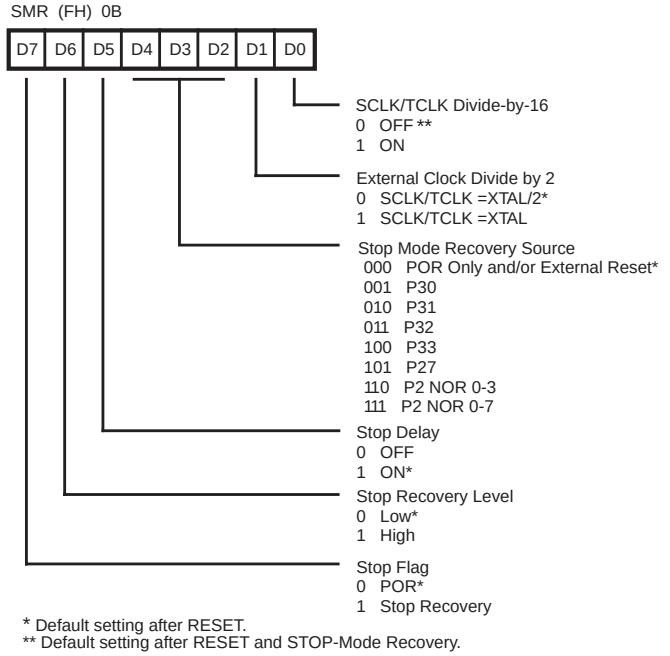


Figure 42. STOP-Mode Recovery Register Write Only Except Bit D7, Which is Read Only

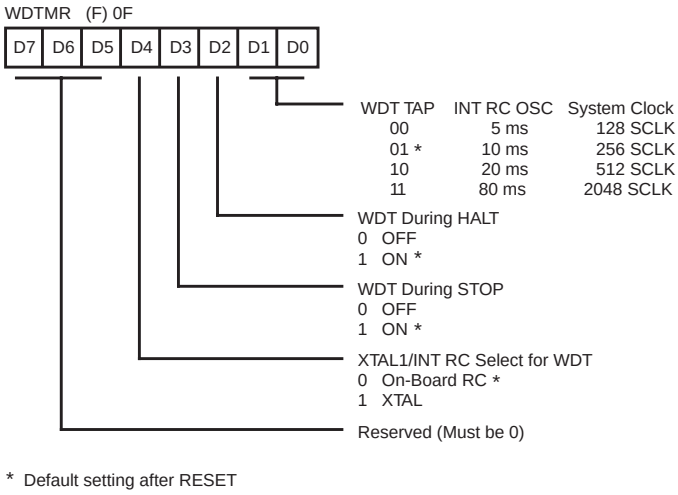


Figure 43. Watch-Dog Timer Mode Register Write Only

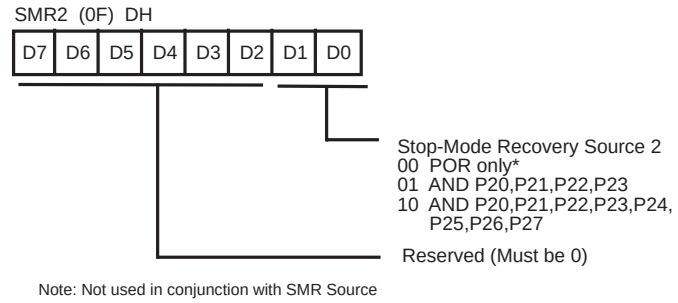
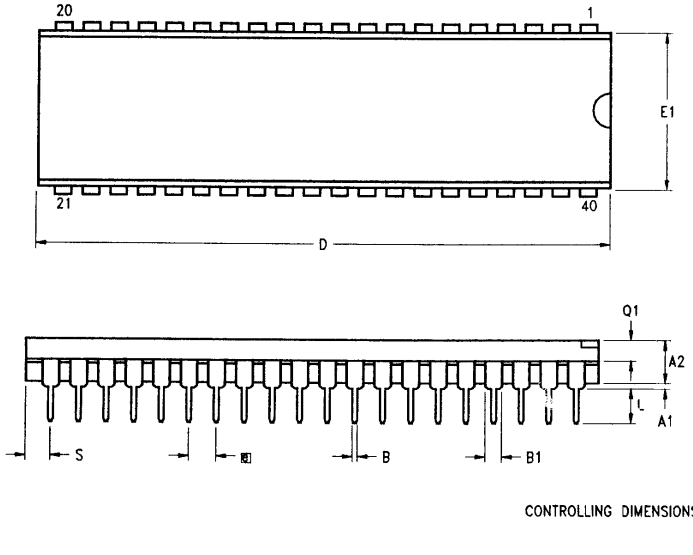


Figure 44. STOP-Mode Recovery Register 2 Write Only

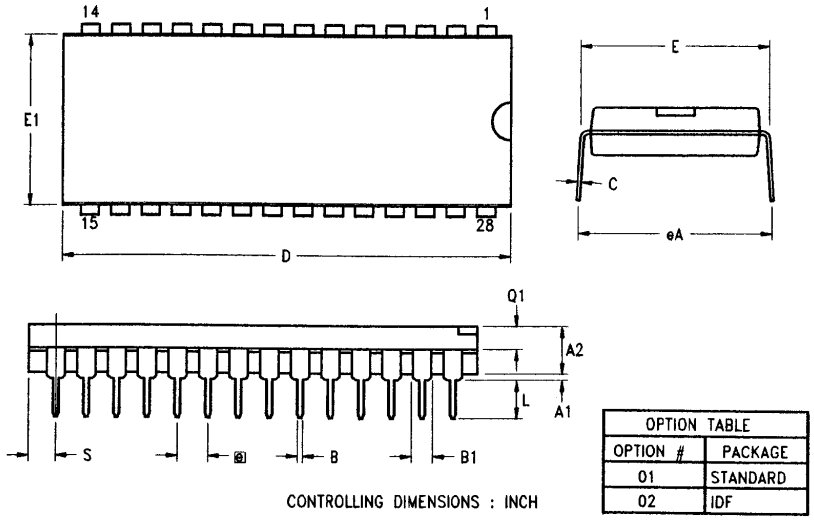
PACKAGE INFORMATION (Continued)

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

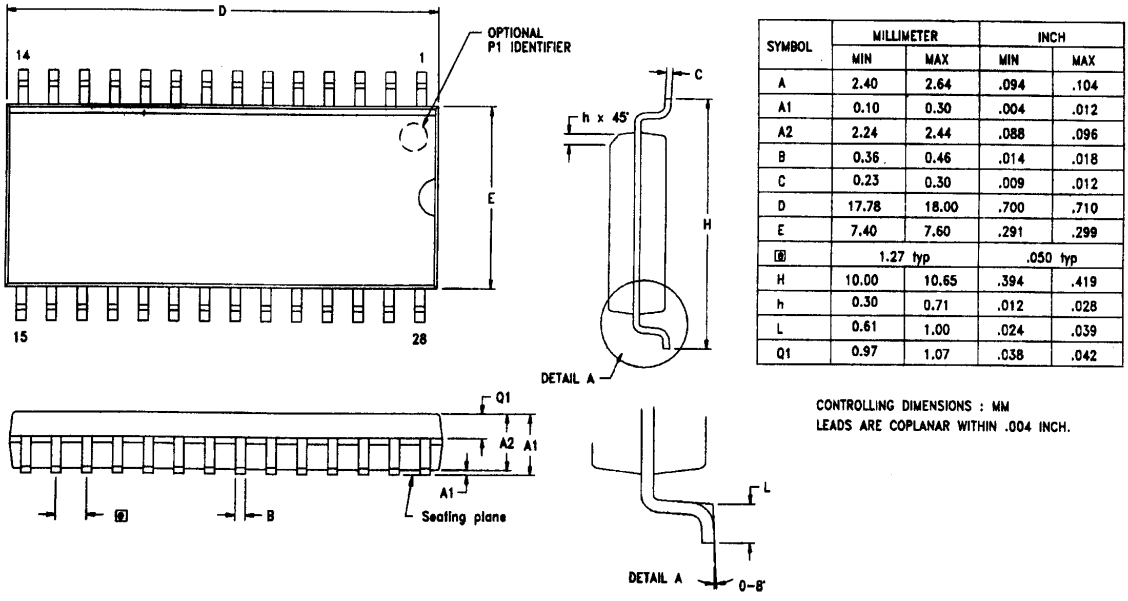
Figure 61. 40-Pin DIP Package Diagram



OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

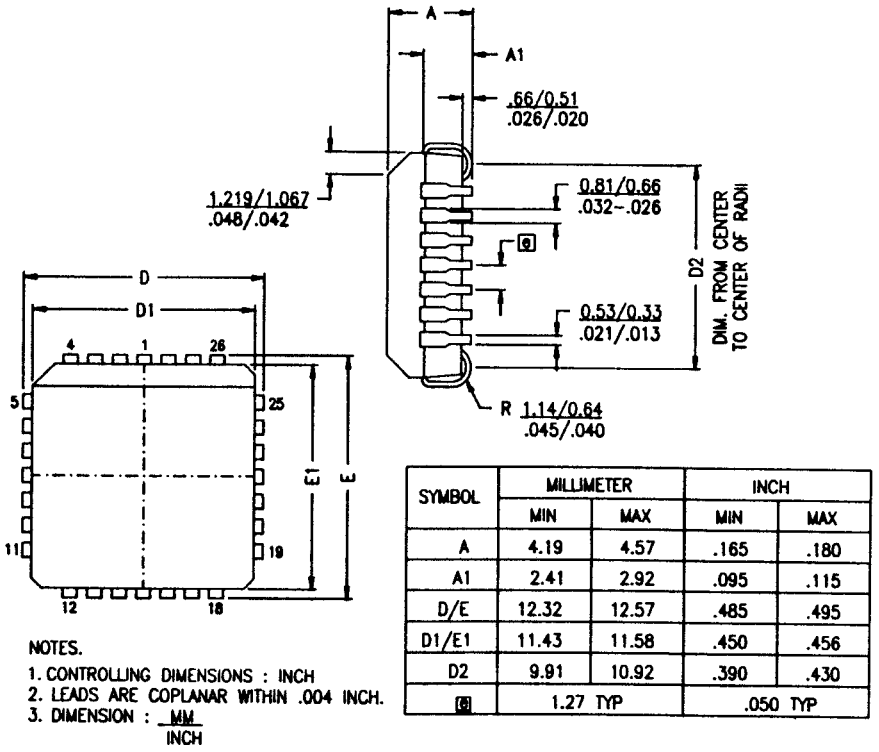
SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.51	1.02	.020	.040
A2		3.18	3.94	.125	.155
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.52	1.91	.060	.075
	02	1.52	1.78	.060	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

Figure 64. 28-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 typ		.050 typ	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.07	.038	.042

Figure 65. 28-Pin SOIC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.19	4.57	.165	.180
A1	2.41	2.92	.095	.115
D/E	12.32	12.57	.485	.495
D1/E1	11.43	11.58	.450	.456
D2	9.91	10.92	.390	.430
e	1.27 TYP		.050 TYP	

Figure 66. 28-Pin PLCC Package Diagram