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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e3016ssc00tr

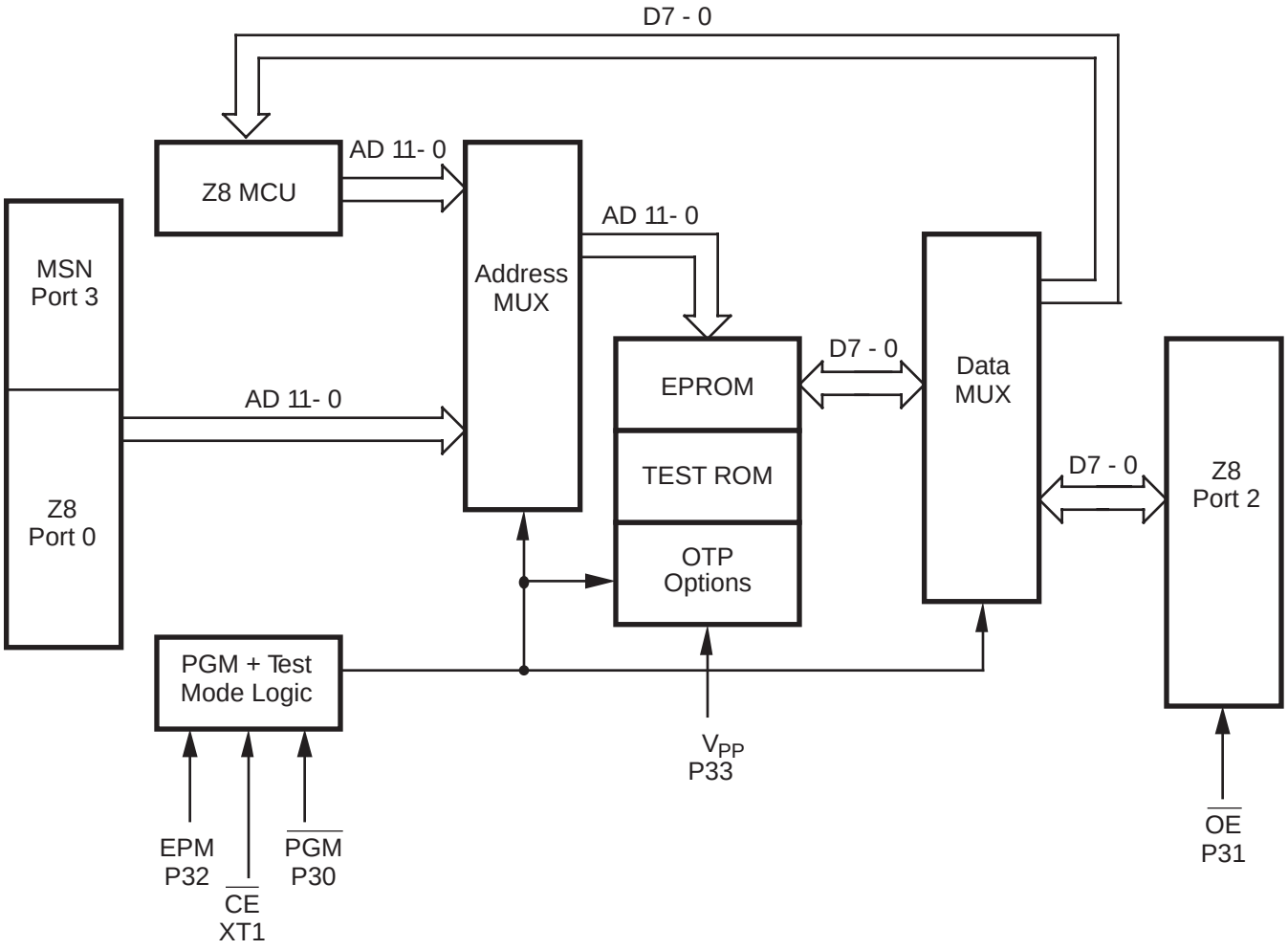


Figure 2. EPROM Programming Block Diagram

PIN IDENTIFICATION (Continued)

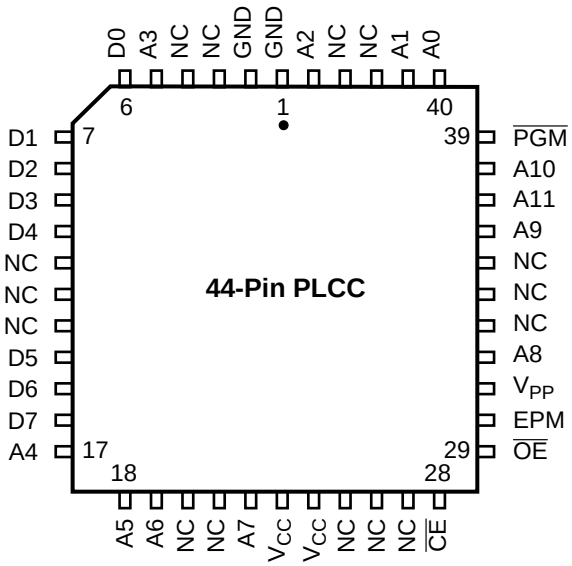


Figure 7. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Table 5. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Pin #	Symbol	Function	Direction
1–2	GND	Ground	
3–4	NC	No Connection	
5	A3	Address 3	Input
6–10	D0–D4	Data 0,1,2,3,4	In/Output
11–13	NC	No Connection	
14–16	D5–D7	Data 5,6,7	In/Output
17–19	A4–A6	Address 4,5,6	Input
20–21	NC	No Connection	
22	A7	Address 7	Input
23–24	V_{CC}	Power Supply	
25–27	NC	No Connection	
28	$\overline{CE}$	Chip Select	Input
29	$\overline{OE}$	Output Enable	Input
30	EPM	EPROM Prog. Mode	Input

Table 5. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Pin #	Symbol	Function	Direction
31	V_{PP}	Prog. Voltage	Input
32	A8	Address 8	Input
33–35	NC	No Connection	
36	A9	Address 9	Input
37	A11	Address 11	Input
38	A10	Address 10	Input
39	$\overline{PGM}$	Prog. Mode	Input
40–41	A0,A1	Address 0,1	Input
42–43	NC	No Connection	
44	A2	Address 2	Input

PIN IDENTIFICATION (Continued)

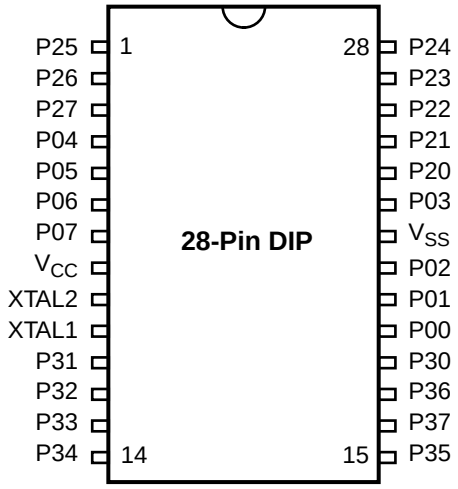


Figure 9. Standard Mode 28-Pin DIP/SOIC Pin Configuration

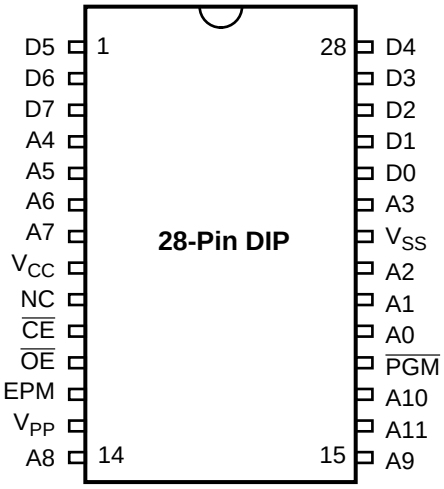


Figure 10. EPROM Programming Mode 28-Pin DIP/SOIC Pin Configuration

Table 7. 28-Pin DIP/SOIC/PLCC Pin Identification*

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Pins 5,6,	In/Output
4–7	P04–P07	Port 0, Pins 4,5,6,7	In/Output
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11–13	P31–P33	Port 3, Pins 1,2,3	Input
14–15	P34–P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19–21	P00–P02	Port 0, Pins 0,1,2	In/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24–28	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output

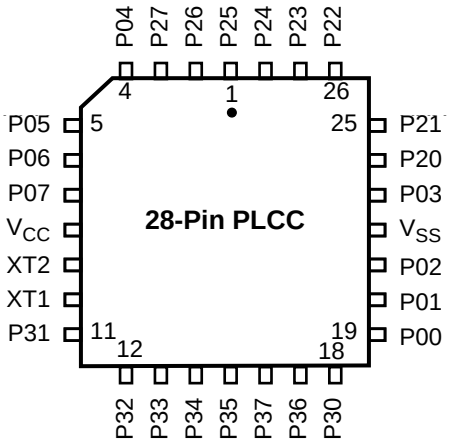


Figure 11. Standard Mode 28-Pin PLCC Pin Configuration

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	–40	+105	C
Storage Temperature	–65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	–0.6	+7	V
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V
Voltage on XTAL1 and $\overline{\text{RESET}}$ Pins with Respect to V_{SS} [Note 2]	–0.6	V_{DD}+1	V
Total Power Dissipation		1.21	W
Maximum Allowable Current out of V_{SS}		220	mA
Maximum Allowable Current into V_{DD}		180	mA
Maximum Allowable Current into an Input Pin [Note 3]	–600	+600	µA
Maximum Allowable Current into an Open-Drain Pin [Note 4]	–600	+600	µA
Maximum Allowable Output Current Sinked by Any I/O Pin		25	mA
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA
Maximum Allowable Output Current Sinked by $\overline{\text{RESET}}$ Pin		3 mA	

Notes:
1. This applies to all pins except XTAL pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 1.2 W for the package. Power dissipation is calculated as follows:

Total Power Dissipation = V_{DD} x [I_{DD} – (sum of I_{OH})]
+ sum of [(V_{DD} – V_{OH}) x I_{OH}]
+ sum of (V_{0L} x I_{0L})

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Test Load).

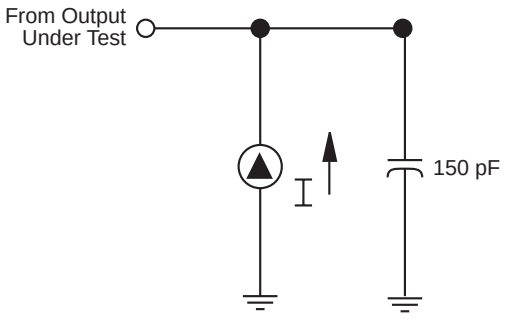


Figure 13. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS (Continued)

				T_A = 0°C to 70°C 16 MHz			
No	Symbol	Parameter	Note [3] V_{CC}	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	3.5V 5.5V	25 25		ns ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	3.5V 5.5V	35 35		ns ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	3.5V 5.5V		180 180	ns ns	1,2
4	TwAS	$\overline{AS}$ Low Width	3.5V 5.5V	40 40		ns ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	3.5V 5.5V	0 0		ns ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	3.5V 5.5V	135 135		ns ns	1,2
7	TwDSW	$\overline{DS}$ (Write) Low Width	3.5V 5.5V	80 80		ns ns	1,2
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid	3.5V 5.5V		75 75	ns ns	1,2
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	3.5V 5.5V	0 0		ns ns	2
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	3.5V 5.5V	50 50		ns ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	3.5V 5.5V	35 35		ns ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	3.5V 5.5V	25 25		ns ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	3.5V 5.5V	35 35		ns ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	3.5V 5.5V	55 55	25 25	ns ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	3.5V 5.5V	35 35		ns ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.5V 5.5V		230 230	ns ns	1,2
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	3.5V 5.5V	45 45		ns ns	2
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Fall Delay	3.5V 5.5V	30 30		ns ns	2
20	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	3.5V 5.5V	35 35		ns ns	

Notes:

1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR D1 = 0, D0 = 0.

			T_A = -40°C to 105°C 16 MHz Note [3]				
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	4.5V 5.5V	25 25		ns ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	4.5V 5.5V	35 35		ns ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	4.5V 5.5V		180 180	ns ns	1,2
4	TwAS	$\overline{AS}$ Low Width	4.5V 5.5V	40 40		ns ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	4.5V 5.5V	0 0		ns ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	4.5V 5.5V	135 135		ns ns	1,2
7	TwDSW	$\overline{DS}$ (Write) Low Width	4.5V 5.5V	80 80		ns ns	1,2
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid	4.5V 5.5V		75 75	ns ns	1,2
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	4.5V 5.5V	0 0		ns ns	2
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	4.5V 5.5V	50 50		ns ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	4.5V 5.5V	35 35		ns ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	4.5V 5.5V	25 25		ns ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	4.5V 5.5V	35 35		ns ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	4.5V 5.5V	55 55	25 25	ns ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	4.5V 5.5V	35 35		ns ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	4.5V 5.5V		230 230	ns ns	1,2
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	4.5V 5.5V	45 45		ns ns	2
18	TdDM(AS)	/DM Valid to $\overline{AS}$ Fall Delay	4.5V 5.5V	30 30		ns ns	2
20	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	4.5V 5.5V	35 35		ns ns	

Notes:

1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

Port 0 (P07–P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble programmed. Either nibble output that can be globally programmed as push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can be placed under handshake control. In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. In ROMless mode, after a hardware reset, Port 0 is configured as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode. In ROM mode, Port 0 is defined as input after reset.

Port 0 can be set in the High-Impedance Mode if selected as an address output state, along with Port 1 and the control signals $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$ (Figure 18).

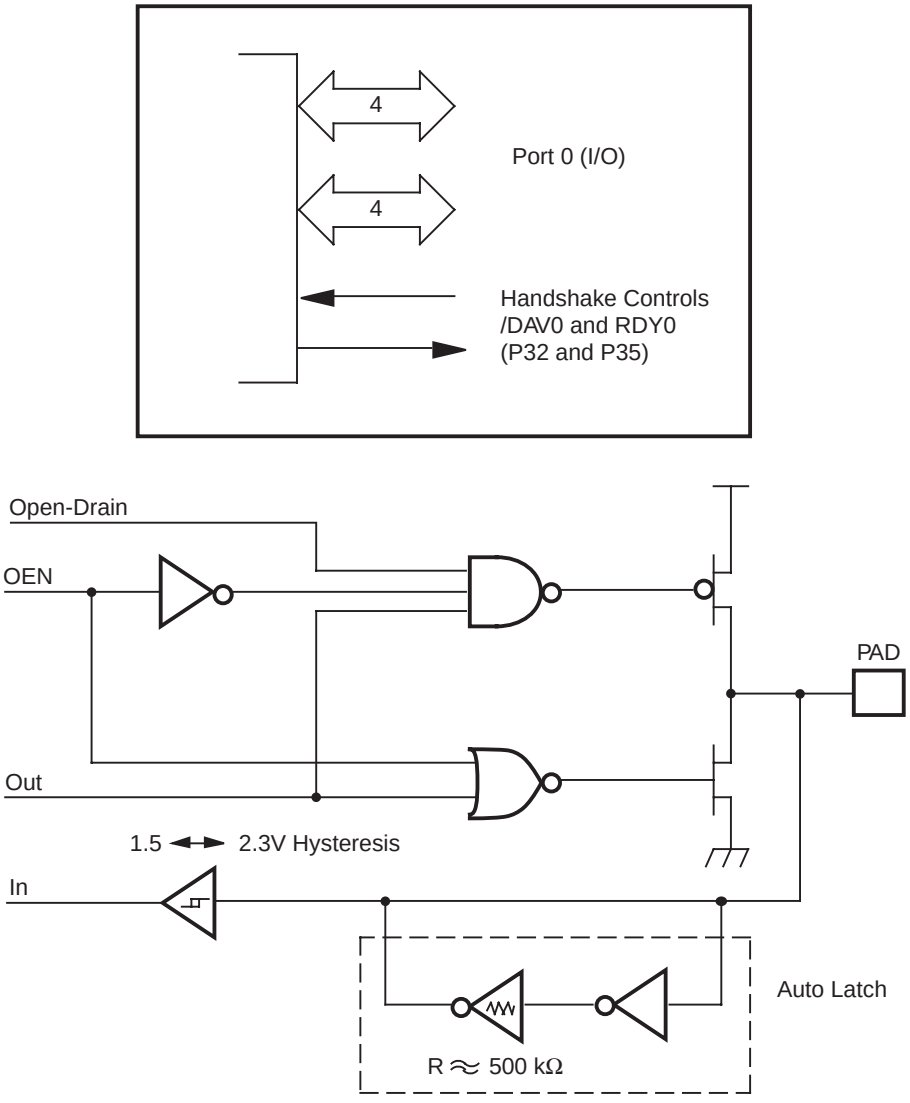


Figure 18. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P17–P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7–A0) and Data (D7–D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and /DAV1 (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (Figure 19).

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z86E40 to share common resources in multiprocessor and DMA applications.

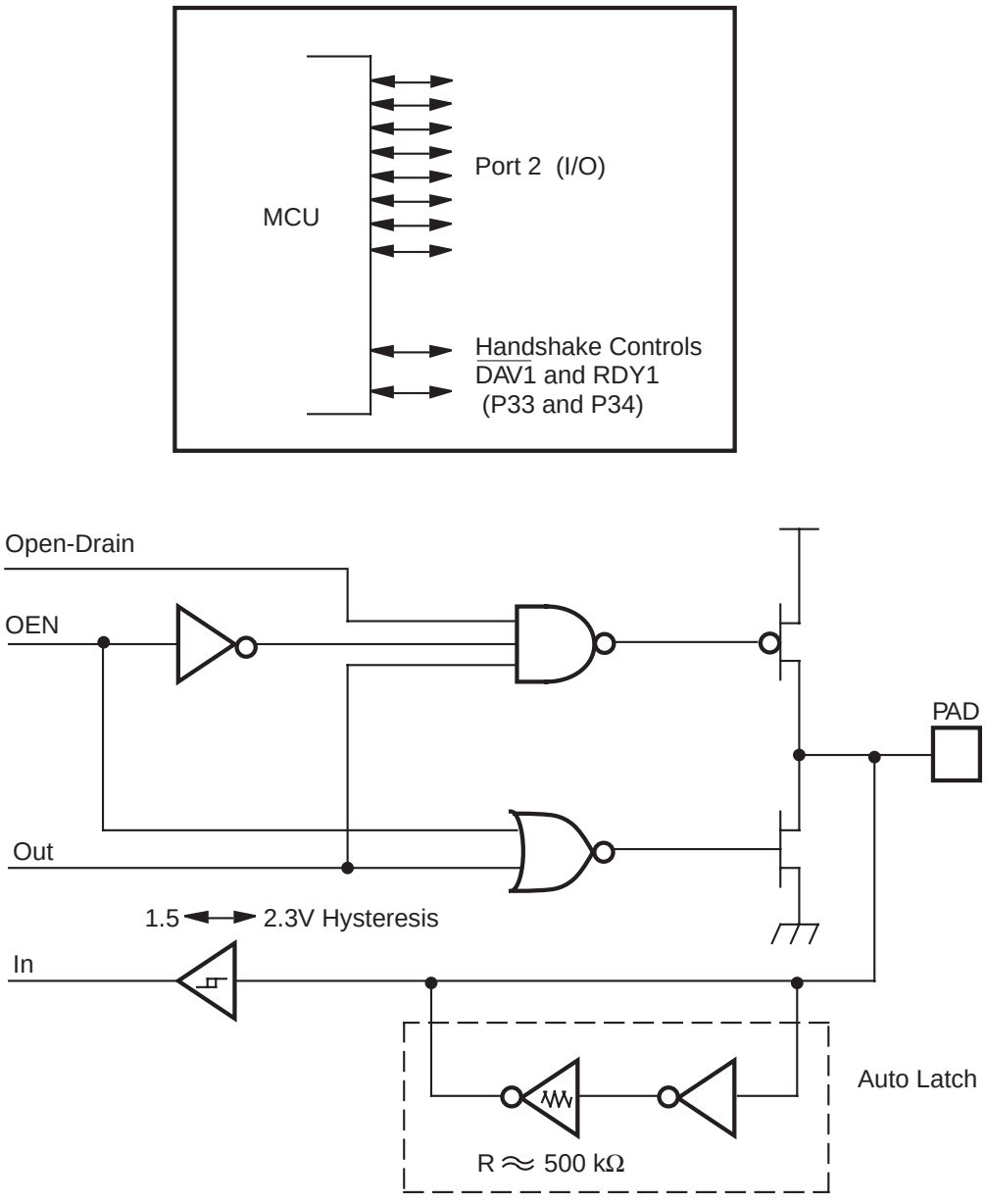


Figure 19. Port 1 Configuration (Z86E40 Only)

PIN FUNCTIONS (Continued)

Port 3 (P37–P30). Port 3 is an 8-bit, CMOS-compatible port with four fixed inputs (P33–P30) and four fixed outputs (P37–P34). These eight lines can be configured by software for interrupt and handshake control functions. Port 3, Pin 0 is Schmitt- triggered. P31, P32, and P33 are standard CMOS inputs with single trip point (no Auto Latches) and P34, P35, P36, and P37 are push-pull output lines. Low EMI output buffers can be globally programmed by the software. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by setting the D1 of Port 3 Mode Register (P3M). The comparator output can be outputted from P34 and P37, respectively, by setting PCON register Bit D0 to 1 state. For the interrupt function, P30 and P33 are falling edge triggered interrupt inputs. P31 and P32 can be programmed as falling, rising or both edges triggered interrupt inputs (Figure 21). Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Port 0, Port 1, and Port 2 are also available on Port 3 (Table 9).

Note: When enabling/ or disabling analog mode, the following is recommended:

1. Allow two NOP delays before reading this comparator output.
2. Disable global interrupts, switch to analog mode, clear interrupts, and then re-enable interrupts.
3. IRQ register bits 3 to 0 must be cleared after enabling analog mode.

Note: P33–P30 differs from the Z86C30/C31/C40 in that there is no clamping diode to V_{CC} due to the EPROM high-voltage circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode.

FUNCTIONAL DESCRIPTION (Continued)

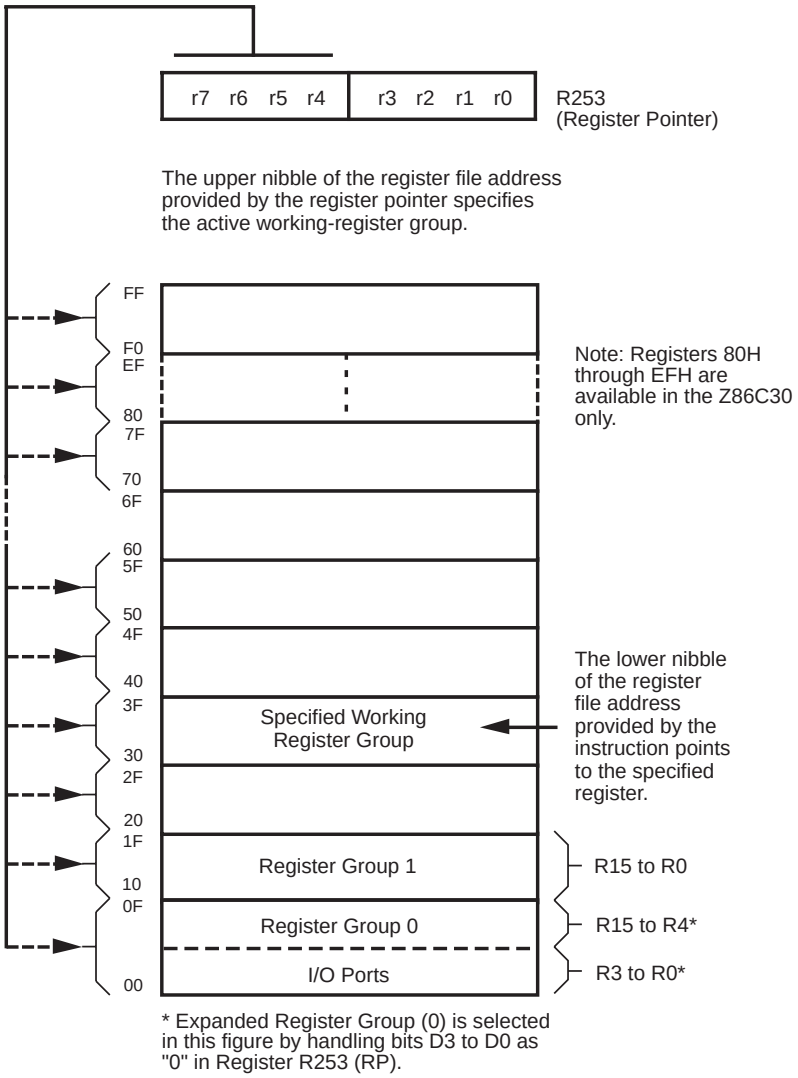


Figure 25. Register Pointer

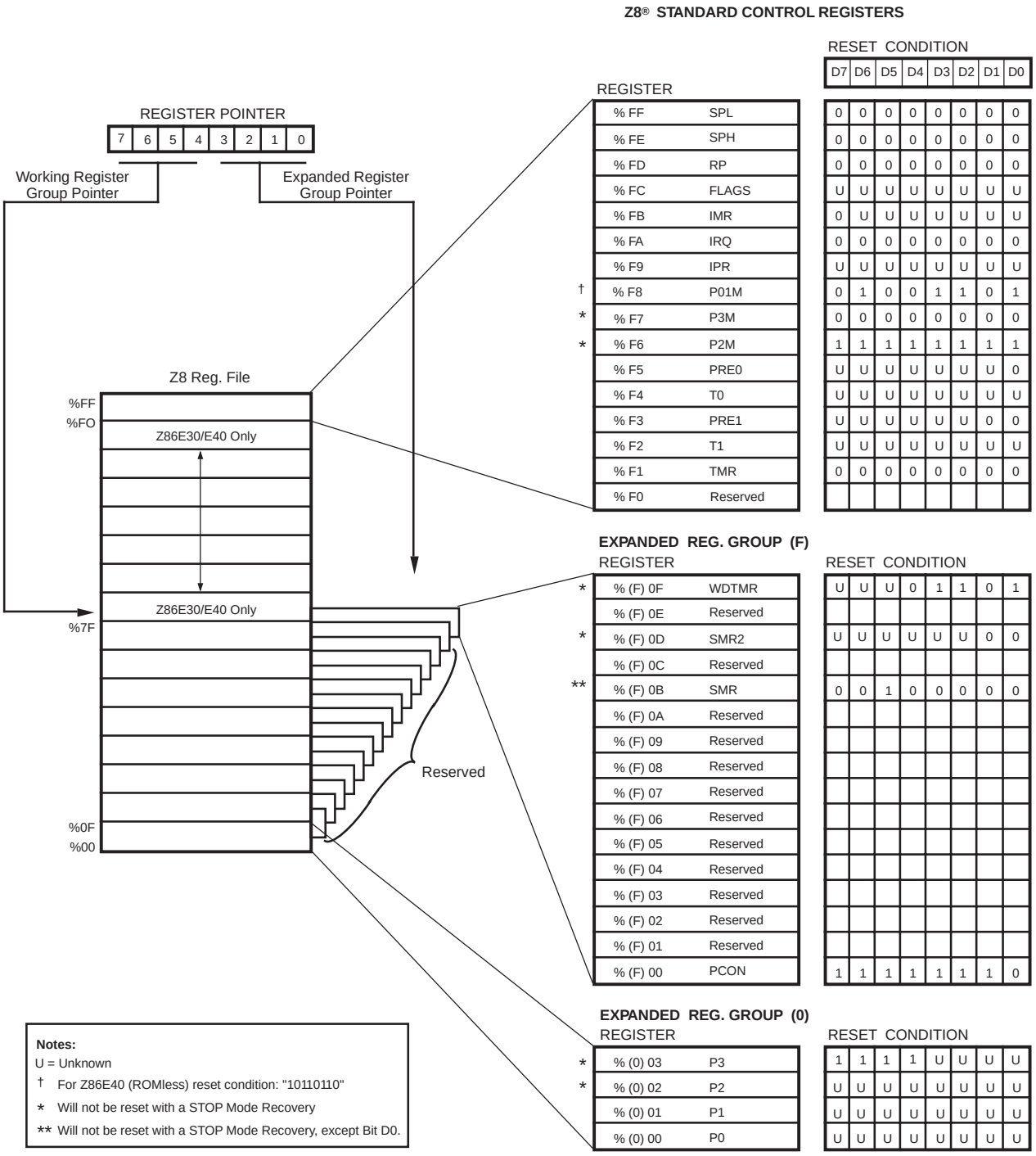


Figure 26. Expanded Register File Architecture

SCLK/TCLK Divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (i.e., D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake up source of the STOP-Mode Recovery (Figure 32). Table 12 shows the SMR source selected with the setting of D2 to D4. P33–P31 cannot be used to wake up from STOP mode when programmed as analog inputs. When the STOP-Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: If the Port2 pin is configured as an output, this output level will be read by the SMR circuitry.

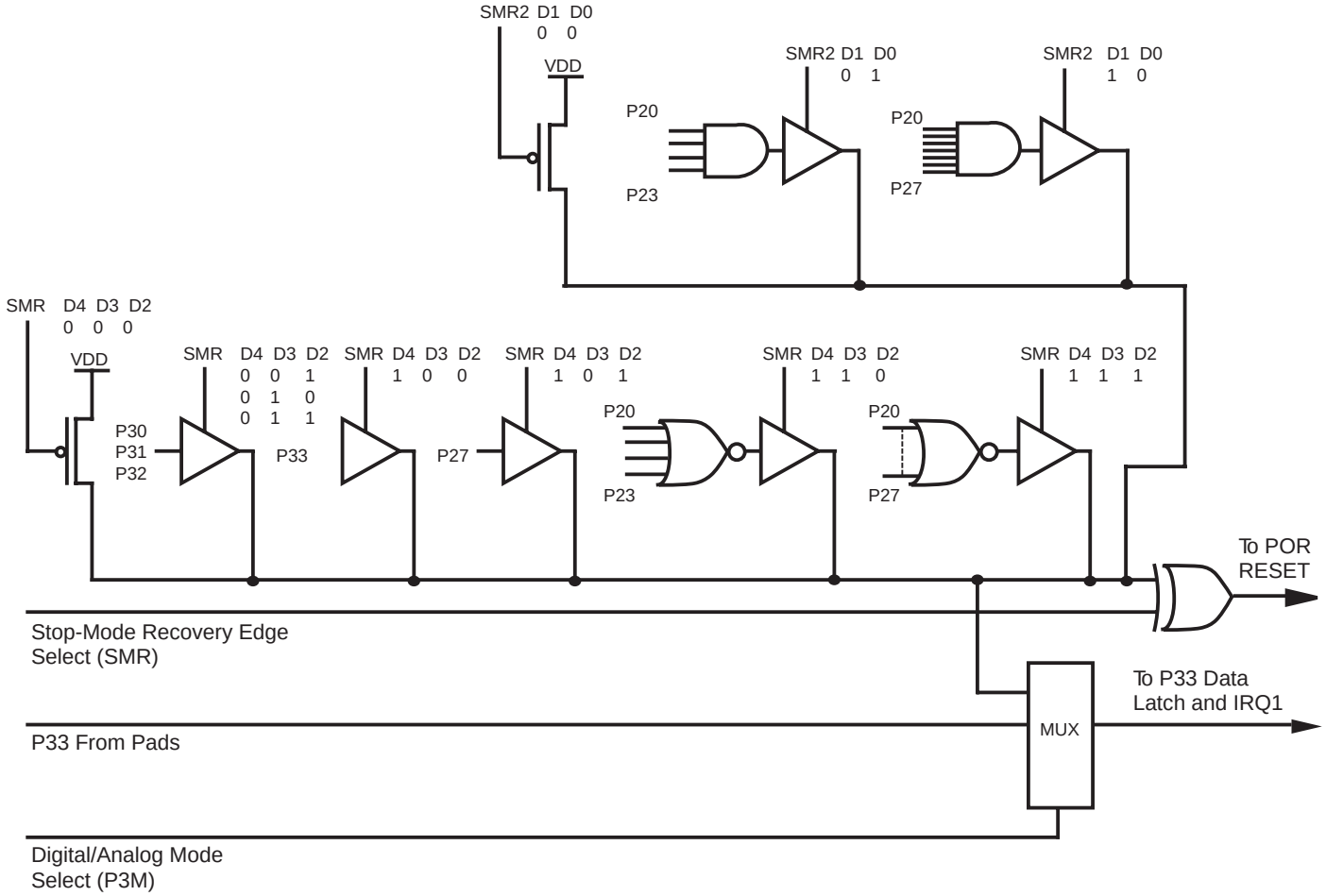


Figure 32. Stop-Mode Recovery Source

FUNCTIONAL DESCRIPTION (Continued)

Table 12. Stop-Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0–3
1	1	1	Logical NOR of Port 2 bits 0–7

Stop-Mode Recovery Delay Select (D5). The 5 ms RESET delay after Stop-Mode Recovery is disabled by programming this bit to a zero. A “1” in this bit will cause a 5 ms RESET delay after Stop-Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the Stop-Mode Recovery source needs to be kept active for at least 5TpC.

Stop-Mode Recovery Level Select (D6). A “1” in this bit defines that a high level on any one of the recovery sources wakes the MCU from STOP Mode. A 0 defines low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A “0” in this bit indicates that the device has been reset by POR (cold). A “1” in this bit indicates the device was awakened by a SMR source (warm).

Stop-Mode Recovery Register 2 (SMR2). This register contains additional Stop-Mode Recovery sources. When the Stop-Mode Recovery sources are selected in this register then SMR Register. Bits D2, D3, and D4 must be 0.

SMR:10		Operation
D1	**D0**	**Description of Action**
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is disabled after Power-On Reset and initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT is driven either by an on-board RC oscillator or an external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register.

Note: Execution of the WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags.

WDT Time-Out Period (D0 and D1). Bits 0 and 1 control a tap circuit that determines the time-out periods that can be obtained (Table 13). The default value of D0 and D1 are 1 and 0, respectively.

Table 13. Time-out Period of WDT

D1	D0	Time-out of the Internal RC OSC	Time-out of the System Clock
0	0	5 ms	128 SCLK
0	1	10 ms*	256 SCLK*
1	0	20 ms	512 SCLK
1	1	80 ms	2048 SCLK

Notes:
*The default setting is 10 ms.

WDT During HALT Mode (D2). This bit determines whether or not the WDT is active during HALT Mode. A “1” indicates that the WDT is active during HALT. A “0” disables the WDT in HALT Mode. The default value is “1”.

WDT During STOP Mode (D3). This bit determines whether or not the WDT is active during STOP mode. A “1” indicates active during STOP. A “0” disables the WDT during STOP Mode. This is applicable only when the WDT clock source is the internal RC oscillator.

Clock Source For WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1, and the WDT is stopped in STOP Mode. The default configuration of this bit is 0, which selects the RC oscillator.

Permanent WDT. When this feature is enabled, the WDT is enabled after reset and will operate in Run and Halt Mode. The control bits in the WDTMR do not affect the WDT operation. If the clock source of the WDT is the internal RC oscillator, then the WDT will run in STOP mode. If the clock source of the WDT is the XTAL1 pin, then the WDT will not run in STOP mode.

Note: WDT time-out in STOP Mode will not reset SMR,SMR2,PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers.

WDTMR Register Accessibility. The WDTMR register is accessible only during the **first 60** internal system clock

FUNCTIONAL DESCRIPTION (Continued)

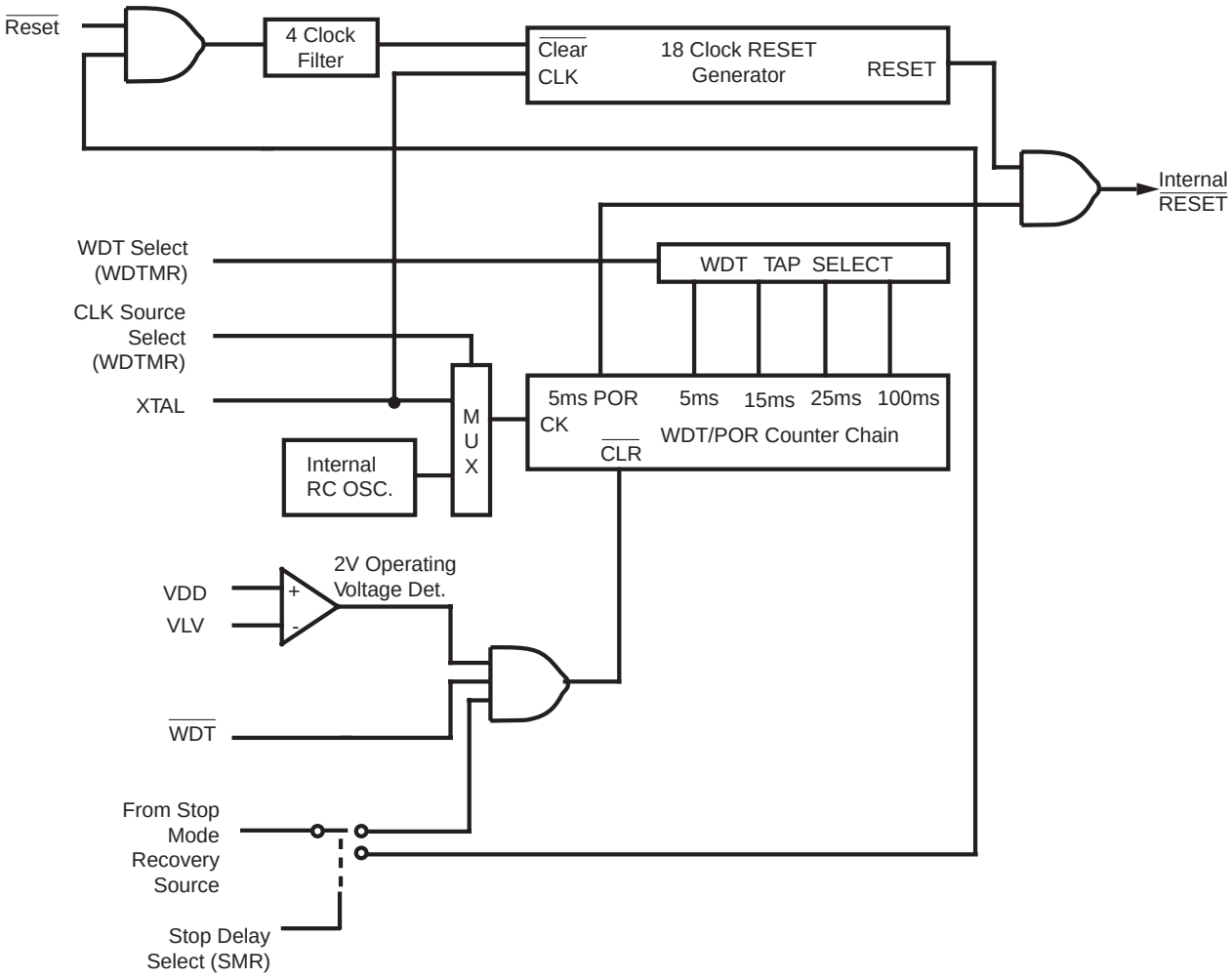


Figure 34. Resets and WDT

FUNCTIONAL DESCRIPTION (Continued)

EPROM MODE

Table 14 shows the programming voltages of each programming mode. Table 15, and figures that follow show the programming timing of each programming mode. Figure 38 shows the circuit diagram of a Z86E40 programming adapter, which adapts from 2764A to Z86E40 and Figure 39 shows the Z86E30/E31 Programming Adapter Circuitry. Figure 40 shows the flowchart of an Intelligent Programming Algorithm, which is compatible with 2764A EPROM (Z86E40 is 4K EPROM, 2764A is 8K EPROM). Since the EPROM size of Z86E30/E31/E40 differs from 2764A, the programming address range has to be set from 0000H to 0FFFH for the Z86E30/E40 and 0000H to 07FFH for Z86E31. Otherwise, the upper portion of EPROM data will overwrite the lower portion of EPROM data. Figure 39 shows the adaptation from the 2764A to Z86E30/E31.

Note: EPROM Protect feature allows the LDC, LDCI, LDE, and LDEI instructions from internal program memory. A ROM lookup table can be used with this feature.

During programming, the V_{PP} input pin supplies the programming voltage and current to the EPROM. This pin is also used to latch which EPROM mode is to be used (R/W EPROM or R/W Option bits). The mode is set by placing the correct mode number on the least significant bits of the address and raising the EPM pin above V. After a setup time, the V_{PP} pin can then be raised or lowered. The latched EPROM mode will remain until the EPM pin is reduced below V_H.

Mode Name	Mode #	LSB Addr
EPROM R/W	0	0000
Option Bit R/W	3	0011

EPROM R/W mode allows the programming of the user mode program ROM.

Option Bit R/W allows the programming of the Z8 option bits. When the device is latched into Option Bit R/W mode, the address must then be changed to 63 decimals (000000111111 Binary). The Options are mapped into this address as follows:

Bit	Option
7	Unused
6	Unused
5	32 KHz XTAL Option
4	Permanent WDT
3	Auto Latch Disable
2	RC Oscillator Option
1	RAM Protect
0	ROM Protect

Table 14 gives the proper conditions for EPROM R/W operations, once the mode is latched.

Z8 CONTROL REGISTER DIAGRAMS (Continued)

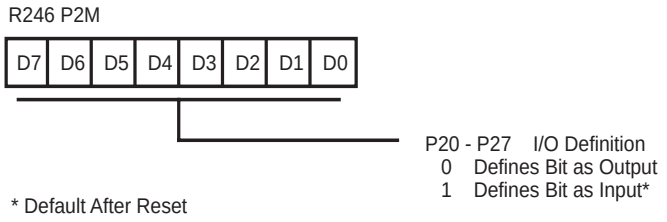


Figure 51. Port 2 Mode Register
F6H: Write Only

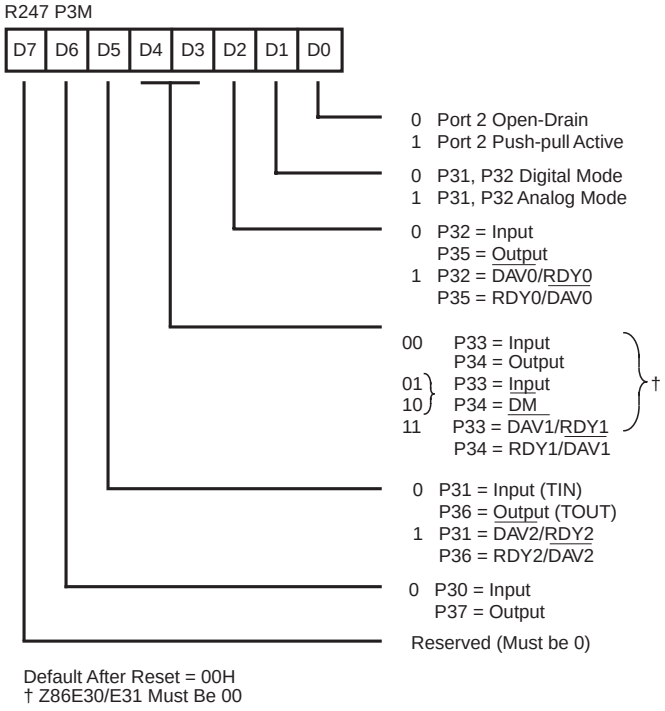


Figure 52. Port 3 Mode Register
F7H: Write Only

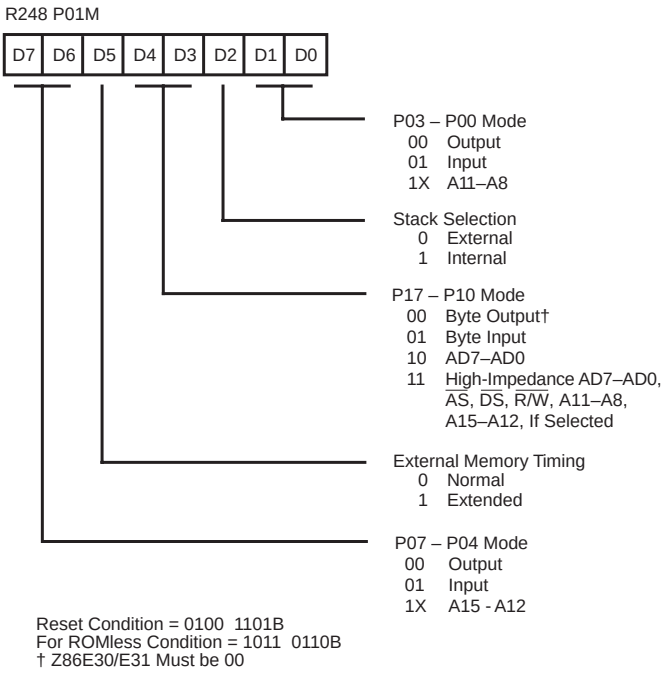


Figure 53. Port 0 and 1 Mode Register
F8H: Write Only
Z86E30/E31 Only

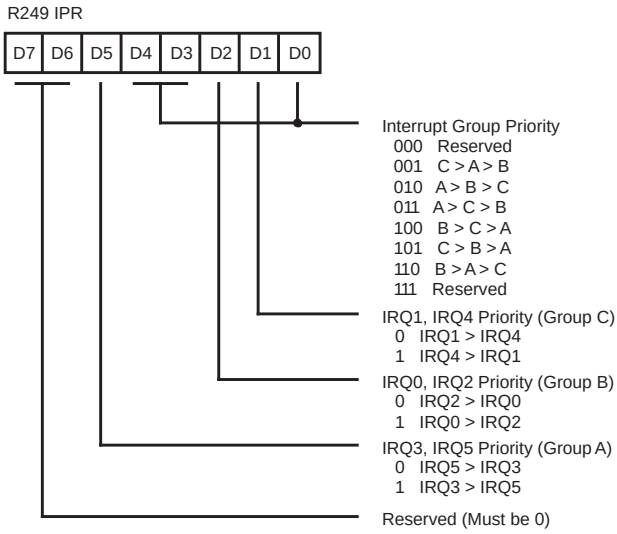


Figure 54. Interrupt Priority Register
F9H: Write Only

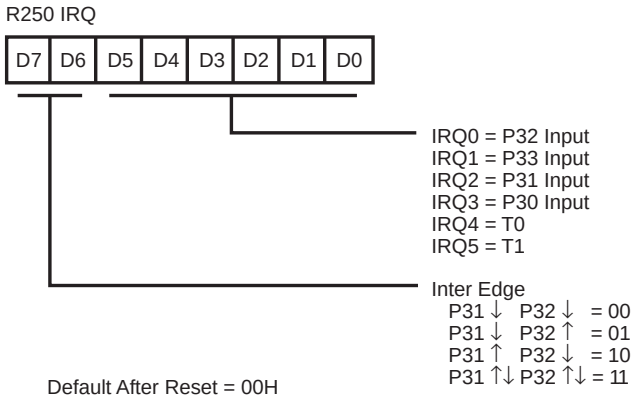
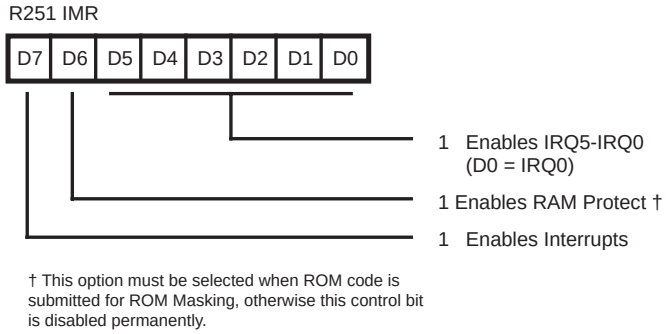


Figure 55. Interrupt Request Register
FAH: Read/Write



† This option must be selected when ROM code is submitted for ROM Masking, otherwise this control bit is disabled permanently.

Figure 56. Interrupt Mask Register
FBH: Read/Write

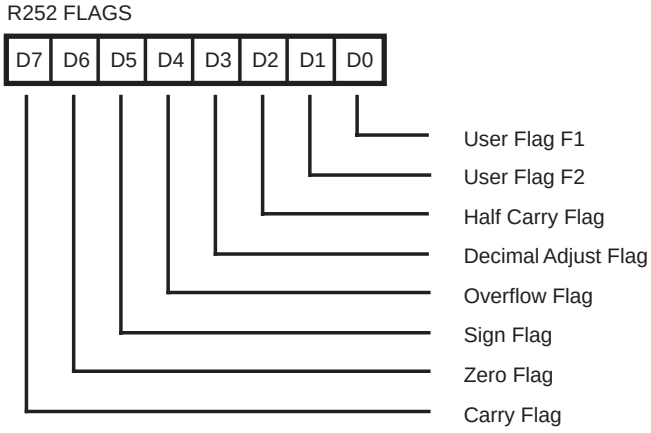


Figure 57. Flag Register
FCH: Read/Write

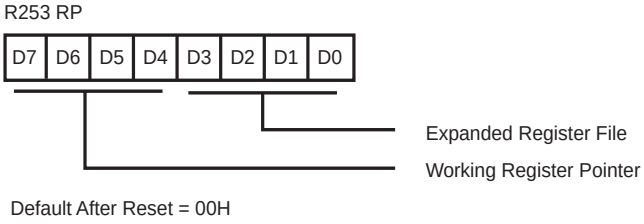


Figure 58. Register Pointer
FDH: Read/Write

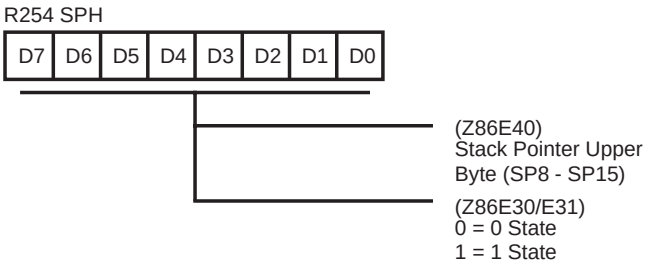


Figure 59. Stack Pointer High
FEH: Read/Write

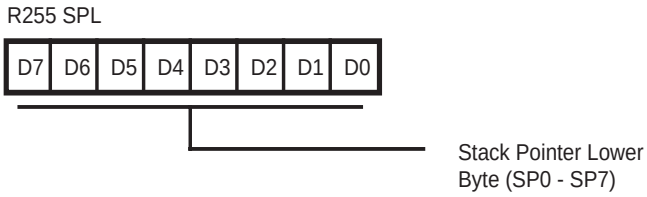
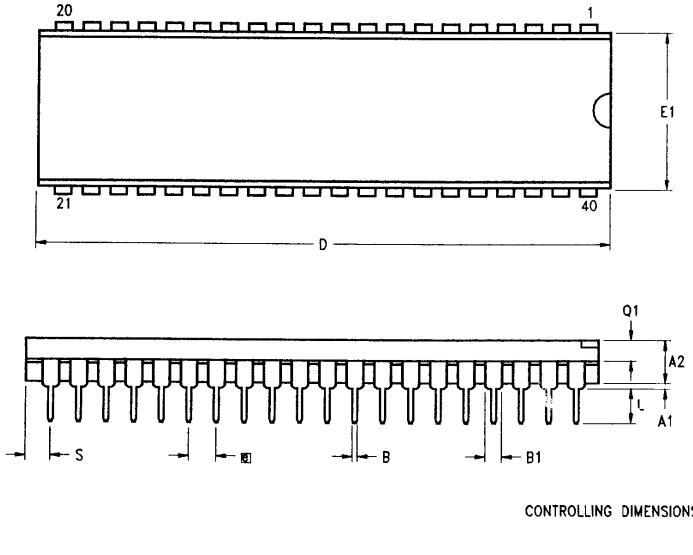


Figure 60. Stack Pointer Low
FFH: Read/Write

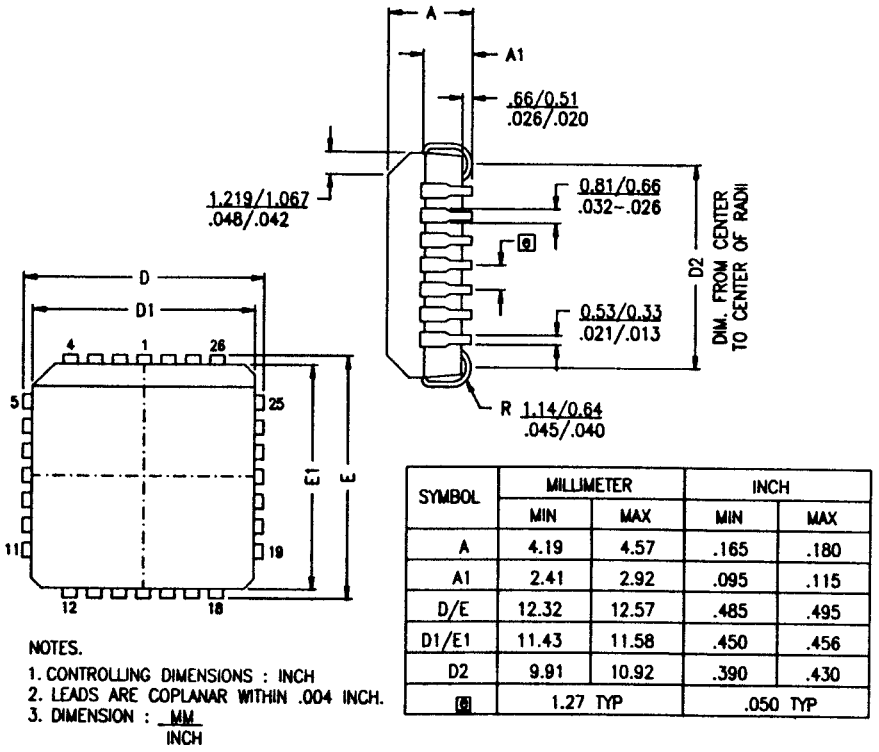
PACKAGE INFORMATION (Continued)

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

Figure 61. 40-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.19	4.57	.165	.180
A1	2.41	2.92	.095	.115
D/E	12.32	12.57	.485	.495
D1/E1	11.43	11.58	.450	.456
D2	9.91	10.92	.390	.430
e	1.27 TYP		.050 TYP	

Figure 66. 28-Pin PLCC Package Diagram

ORDERING INFORMATION

Z86E40 (16 MHz)

40-Pin DIP	44-Pin PLCC	44-Pin LQFP
Z86E4016PSC	Z86E4016VSC	Z86E4016FSC
Z86E4016PEC	Z86E4016VEC	Z86E4016FEC

Z86E30 (16 MHz)

28-Pin DIP	28-Pin SOIC	28-Pin PLCC
Z86E3016PSC	Z86E3016SSC	Z86E3016VSC
Z96E3016PEC	Z86E3016SEC	Z86E3016VEC

Z86E31 (16 MHz)

28-Pin DIP	28-Pin SOIC	28-Pin PLCC
Z86E3116PSC	Z86E3116SSC	Z86E3116VSC
Z86E3116PEC	Z86E3116SEC	Z86E3116VEC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package

P = Plastic DIP

V = Plastic Leaded Chip Carrier

F = Plastic Quad Flat Pack

S = SOIC (Small Outline Integrated Circuit)

Temperature

S = 0 °C to +70 °C
E = -40 °C to +105 °C

Speed

16 = 16 MHz

Environmental

C= Plastic Standard

E = Hermetic Standard

Example:

Z 86E40 16 P S C is a Z86E40, 16 MHz, DIP, 0°C to +70°C, Plastic Standard Flow