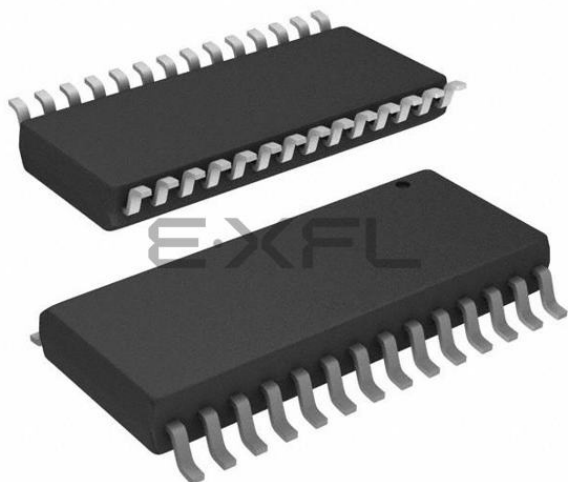




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e3016ssg

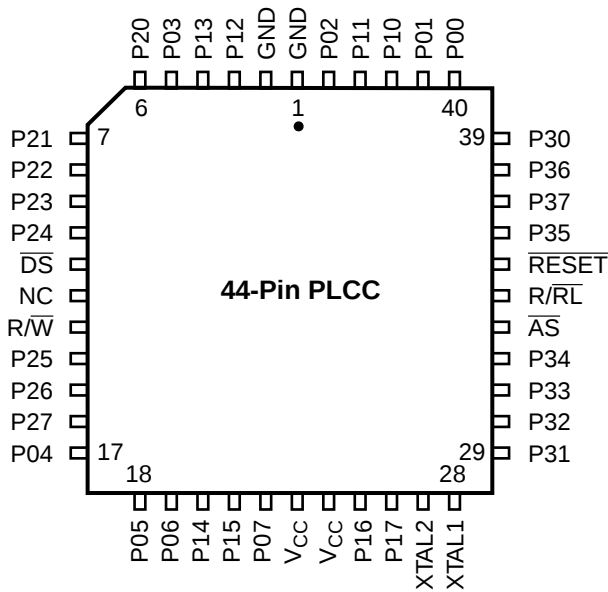


Figure 4. 44-Pin PLCC Pin Configuration
Standard Mode

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1–2	GND	Ground	
3–4	P12–P13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6–10	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output
11	DS	Data Strobe	Output
12	NC	No Connection	
13	R/W	Read/Write	Output
14–16	P25–P27	Port 2, Pins 5,6,7	In/Output
17–19	P04–P06	Port 0, Pins 4,5,6	In/Output
20–21	P14–P15	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23–24	VCC	Power Supply	
25–26	P16–P17	Port 1, Pins 6,7	In/Output
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29–31	P31–P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
33	AS	Address Strobe	Output
34	R/RL	ROM/ROMless select	Input
35	RESET	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40–41	P00–P01	Port 0, Pins 0,1	In/Output
42–43	P10–P11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

PIN IDENTIFICATION (Continued)

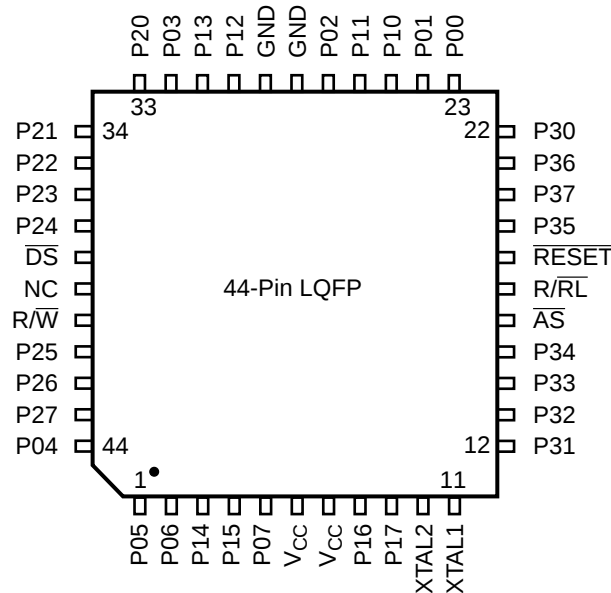


Figure 5. 44-Pin LQFP Pin Configuration
Standard Mode

Table 3. 44-Pin LQFP Pin Identification

Pin #	Symbol	Function	Direction
1–2	P05–P06	Port 0, Pins 5,6	In/Output
3–4	P14–P15	Port 1, Pins 4,5	In/Output
5	P07	Port 0, Pin 7	In/Output
6–7	V _{CC}	Power Supply	
8–9	P16–P17	Port 1, Pins 6,7	In/Output
10	XTAL2	Crystal Oscillator	Output
11	XTAL1	Crystal Oscillator	Input
12–14	P31–P33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	AS	Address Strobe	Output
17	R/RL	ROM/ROMless select	Input
18	RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23–24	P00–P01	Port 0, Pin 0,1	In/Output
25–26	P10–P11	Port 1, Pins 0,1	In/Output

Table 3. 44-Pin LQFP Pin Identification

Pin #	Symbol	Function	Direction
27	P02	Port 0, Pin 2	In/Output
28–29	GND	Ground	
30–31	P12–P13	Port 1, Pins 2,3	In/Output
32	P03	Port 0, Pin 3	In/Output
33–37	P20–4	Port 2, Pins 0,1,2,3,4	In/Output
38	DS	Data Strobe	Output
39	NC	No Connection	
40	R/W	Read/Write	Output
41–43	P25–P27	Port 2, Pins 5,6,7	In/Output
44	P04	Port 0, Pin 4	In/Output

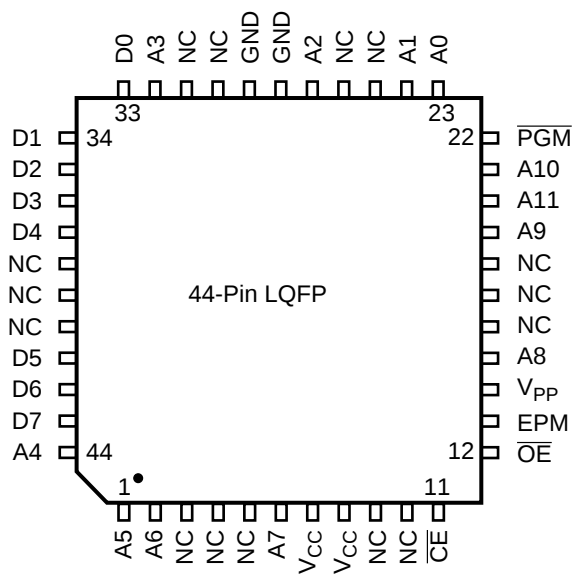


Figure 8. 44-Pin LQFP Pin Configuration
EPROM Programming Mode

Table 6. 44-Pin LQFP Pin Configuration
EPROM Programming Mode

Pin #	Symbol	Function	Direction
1–2	A5–A6	Address 5,6	Input
3–4	NC	No Connection	
5	A7	Address 7	Input
6–7	V _{CC}	Power Supply	
8–10	NC	No Connection	
11	CE	Chip Select	Input
12	OE	Output Enable	Input
13	EPM	EPROM Prog. Mode	Input
14	V _{PP}	Prog. Voltage	Input
15	A8	Address 8	Input
16–18	NC	No Connection	
19	A9	Address 9	Input
20	A11	Address 11	Input
21	A10	Address 10	Input
22	PGM	Prog. Mode	Input

Table 6. 44-Pin LQFP Pin Configuration
EPROM Programming Mode

Pin #	Symbol	Function	Direction
23–24	A0,A1	Address 0,1	Input
25–26	NC	No Connection	
27	A2	Address 2	Input
28–29	GND	Ground	
30–31	NC	No Connection	
32	A3	Address 3	Input
33–37	D0–D4	Data 0,1,2,3,4	In/Output
38–40	NC	No Connection	
41–43	D5–D7	Data 5,6,7	In/Output
44	A4	Address 4	Input

DC ELECTRICAL CHARACTERISTICS (Continued)

$T_A = 0\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$								
Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current	3.5V		20	7	mA	@ 16 MHz	4,5
		5.5V		25	20	mA	@ 16 MHz	4,5
I_{CC1}	Standby Current Halt Mode	3.5V		8	3.7	mA	$V_{IN} = 0V, V_{CC}$	4,5
		5.5V		8	3.7	mA	@ 16 MHz	4,5
		3.5V		7.0	2.9	mA	Clock Divide by	4,5
		5.5V		7.0	2.9	mA	16 @ 16 MHz	4,5
I_{CC2}	Standby Current Stop Mode	3.5V		10	2	μA	$V_{IN} = 0V, V_{CC}$	6,11
		5.5V		10	3	μA	$V_{IN} = 0V, V_{CC}$	6,11
		3.5V		800	600	μA	$V_{IN} = 0V, V_{CC}$	6,11,1 4
		5.5V		800	600	μA	$V_{IN} = 0V, V_{CC}$	6,11,1 4
I_{ALL}	Auto Latch Low Current	3.5V	0.7	8	2.4	μA	$0V < V_{IN} < V_{CC}$	9
		5.5V	1.4	15	4.7	μA	$0V < V_{IN} < V_{CC}$	9
I_{ALH}	Auto Latch High Current	3.5V	-0.6	-5	-1.8	μA	$0V < V_{IN} < V_{CC}$	9
		5.5V	-1	-8	-3.8	μA	$0V < V_{IN} < V_{CC}$	9
T_{POR}	Power On Reset	3.5V	3.0	24	7	ms		
		5.5V	2.0	13	4	ms		
V_{LV}	Auto Reset Voltage		2.3	3.1	2.9	V		1,7

Notes:

1. Device does function down to the Auto Reset voltage.
2. GND=0V
3. The V_{CC} voltage specification of 5.5V guarantees $5.0V \pm 0.5V$ and the V_{CC} voltage specification of 3.5V guarantees only 3.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1= CL2 = 22 pF
6. Same as note [4] except inputs at V_{CC} .
7. Max. temperature is 70°C.
8. STD Mode (not Low EMI Mode)
9. Auto Latch (mask option) selected
10. For analog comparator inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.
12. Typicals are at $V_{CC} = 5.0V$ and $V_{CC} = 3.5V$
13. Z86E40 only
14. WDT running

Additional Timing Table (Divide-By-One Mode)

				$T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$		$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$			
				4 MHz		4 MHz			
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.5V 5.5V	250 250	DC DC	250 250	DC DC	ns ns	1,7,8 1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V 5.5V		25 25		25 25	ns ns	1,7,8 1,7,8
3	TwC	Input Clock Width	3.5V 5.5V	100 100		100 100		ns ns	1,7,8 1,7,8
4	TwTinL	Timer Input Low Width	3.5V 5.5V	100 70		100 70		ns ns	1,7,8 1,7,8
5	TwTinH	Timer Input High Width	3.5V 5.5V	5TpC 5TpC		5TpC 5TpC			1,7,8 1,7,8
6	TpTin	Timer Input Period	3.5V 5.5V	8TpC 8TpC		8TpC 8TpC			1,7,8 1,7,8
7	TrTin, Tftin	Timer Input Rise & Fall Timer	3.5V 5.5V		100 100		100 100	ns ns	1,7,8 1,7,8
8A	TwIL	Int. Request Low Time	3.5V 5.5V	100 70		100 70		ns ns	1,2,7,8 1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V 5.5V	5TpC 5TpC		5TpC 5TpC			1,3,7,8 1,3,7,8
9	TwIH	Int. Request Input High Time	3.5V 5.5V	5TpC 5TpC		5TpC 5TpC			1,2,7,8 1,2,7,8
10	Twsm	STOP Mode Recovery Width Spec	3.5V 5.5V	12 12		12 12		ns ns	4,8 4,8
11	Tost	Oscillator Startup Time	3.5V 5.5V		5TpC 5TpC		5TpC		4,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31–P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 1, POR STOP Mode Delay is on.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 5.5V guarantees 5.0V $\pm$ 0.5V and the V_{CC} voltage specification of 3.5V guarantees 3.5V only.
7. SMR D1 = 0.
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

DC ELECTRICAL CHARACTERISTICS (Continued)

Handshake Timing Diagrams

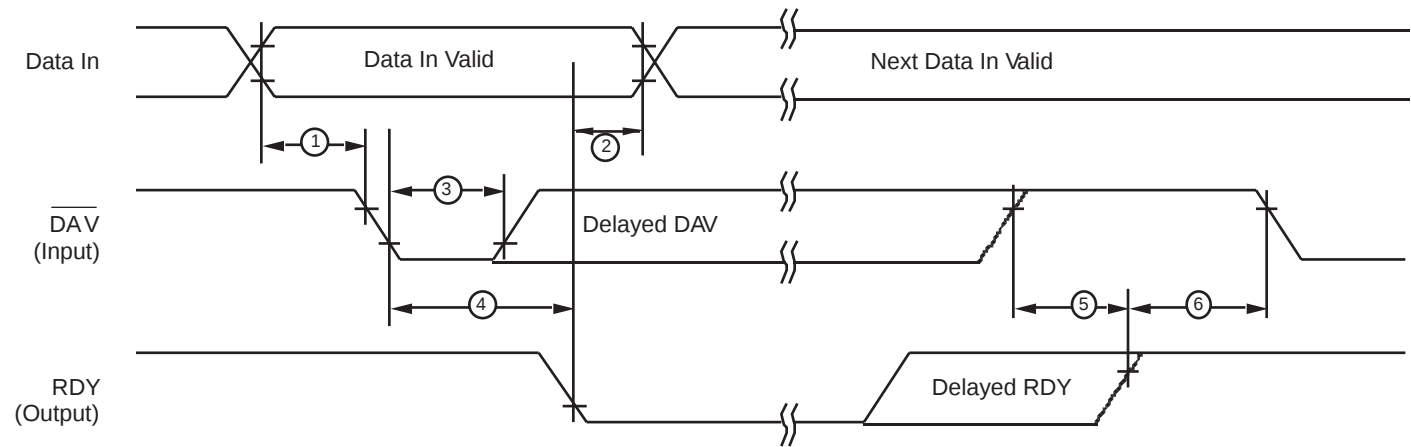


Figure 16. Input Handshake Timing

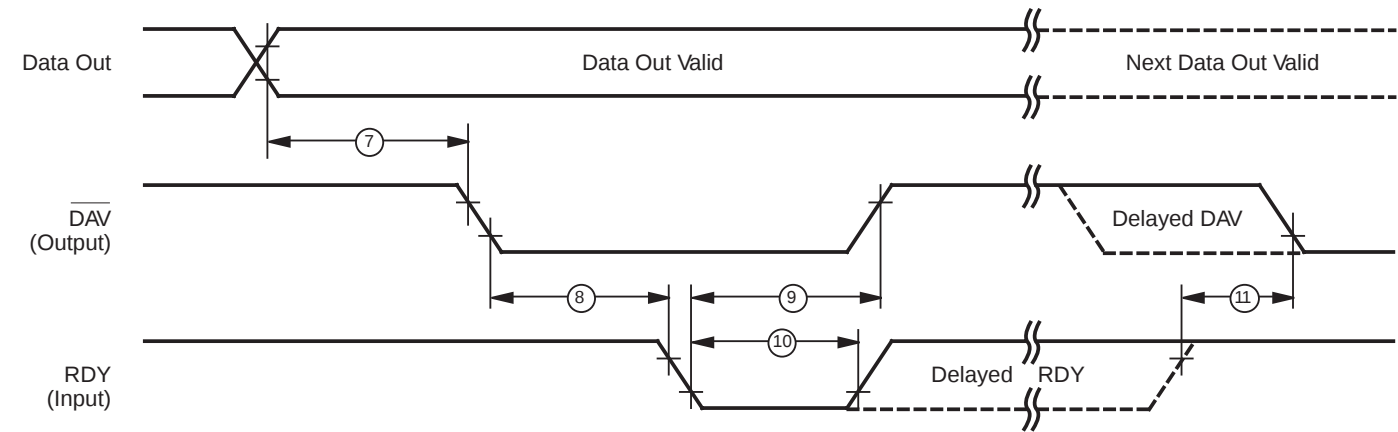


Figure 17. Output Handshake Timing

Additional Timing Table

$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$								
16 MHz								
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Units	Conditions	Notes
1	TpC	Input Clock Period	3.5V	62.5	DC	ns		1,7,8
			5.5V	62.5	DC	ns		1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15	ns		1,7,8
			5.5V		15	ns		1,7,8
3	TwC	Input Clock Width	3.5V	31		ns		1,7,8
			5.5V	31		ns		1,7,8
4	TwTinL	Timer Input Low Width	3.5V	70		ns		1,7,8
			5.5V	70		ns		1,7,8
5	TwTinH	Timer Input High Width	3.5V	5TpC				1,7,8
			5.5V	5TpC				1,7,8
6	TpTin	Timer Input Period	3.5V	8TpC				1,7,8
			5.5V	8TpC				1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100	ns		1,7,8
			5.5V		100	ns		1,7,8
8A	TwIL	Int. Request Low Time	3.5V	70		ns		1,2,7,8
			5.5V	70		ns		1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V	5TpC				1,3,7,8
			5.5V	5TpC				1,3,7,8
9	TwIH	Int. Request Input High Time	3.5V	5TpC				1,2,7,8
			5.5V					
10	Twsm	STOP Mode Recovery Width Spec	3.5V	12		ns		4,8
			5.5V	12		ns		4,8
11	Tost	Oscillator Startup Time	3.5V		5TpC			4,8
			5.5V		5TpC			4,8
12	Twdt	Watch-Dog Timer Delay Time Before Timeout	3.5V	10		ms	D0 = 0	5,11
			5.5V	5		ms	D1 = 0	5,11
			3.5V	20		ms	D0 = 1	5,11
			5.5V	10		ms	D1 = 0	5,11
			3.5V	40		ms	D0 = 0	5,11
			5.5V	20		ms	D1 = 1	5,11
			3.5V	160		ms	D0 = 1	5,11
			5.5V	80		ms	D1 = 1	5,11

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31–P33)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Reg. WDTMR
6. The V_{CC} voltage spec. of 5.5V guarantees 5.0V $\pm$ 0.5V.
7. SMR D1 = 0
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
9. For RC and LC oscillator, and for oscillator driven by clock driver.
10. Standard Mode (not Low EMI output ports)
11. Using internal RC

PIN FUNCTIONS (Continued)

Port 1 (P17–P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7–A0) and Data (D7–D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls

RDY1 and /DAV1 (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (Figure 19).

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and $R/\overline{W}$, allowing the Z86E40 to share common resources in multiprocessor and DMA applications.

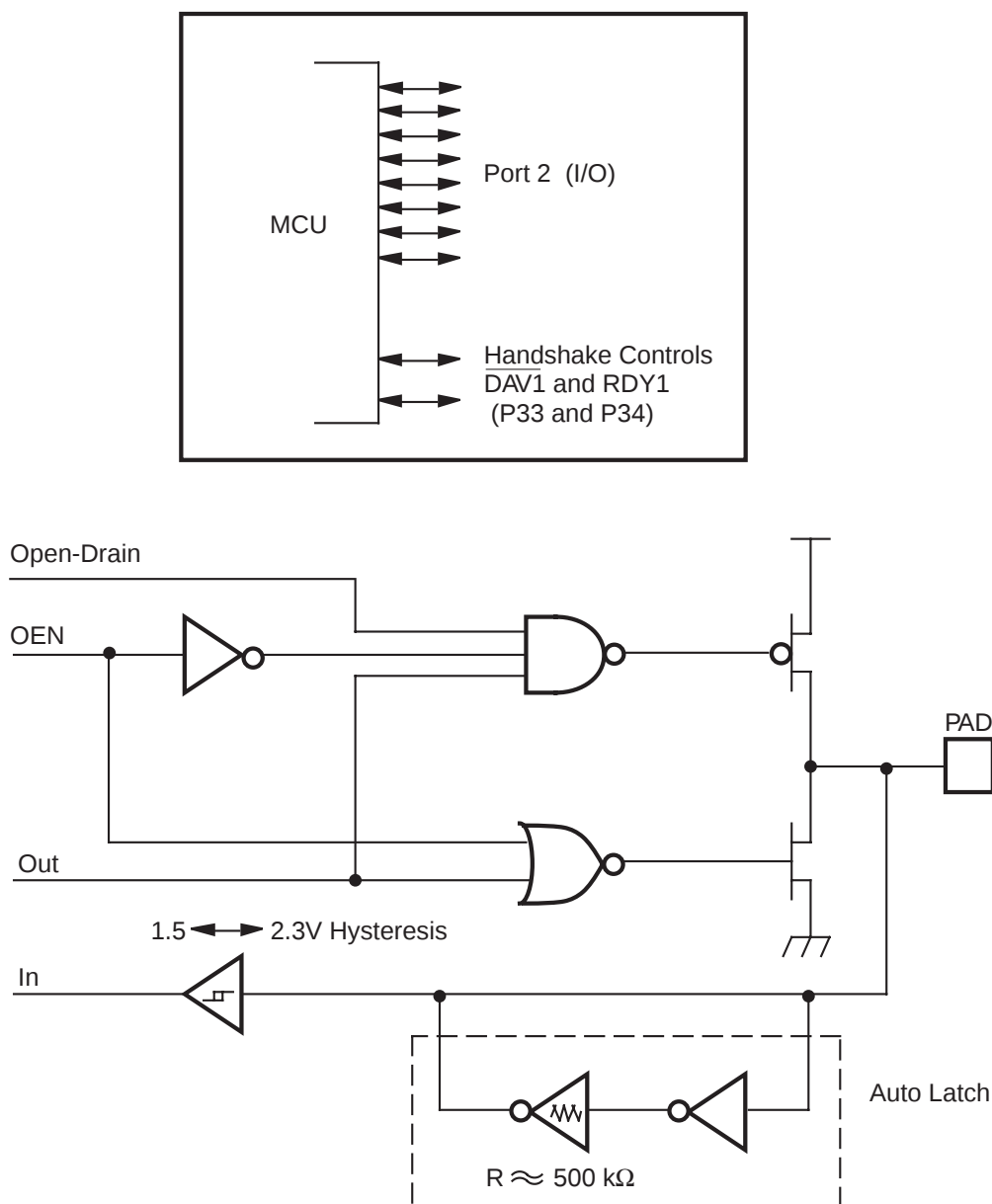


Figure 19. Port 1 Configuration (Z86E40 Only)

Port 2 (P27–P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can

be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control.

In Handshake Mode, Port 3 lines P31 and P36 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2 (Figure 20).

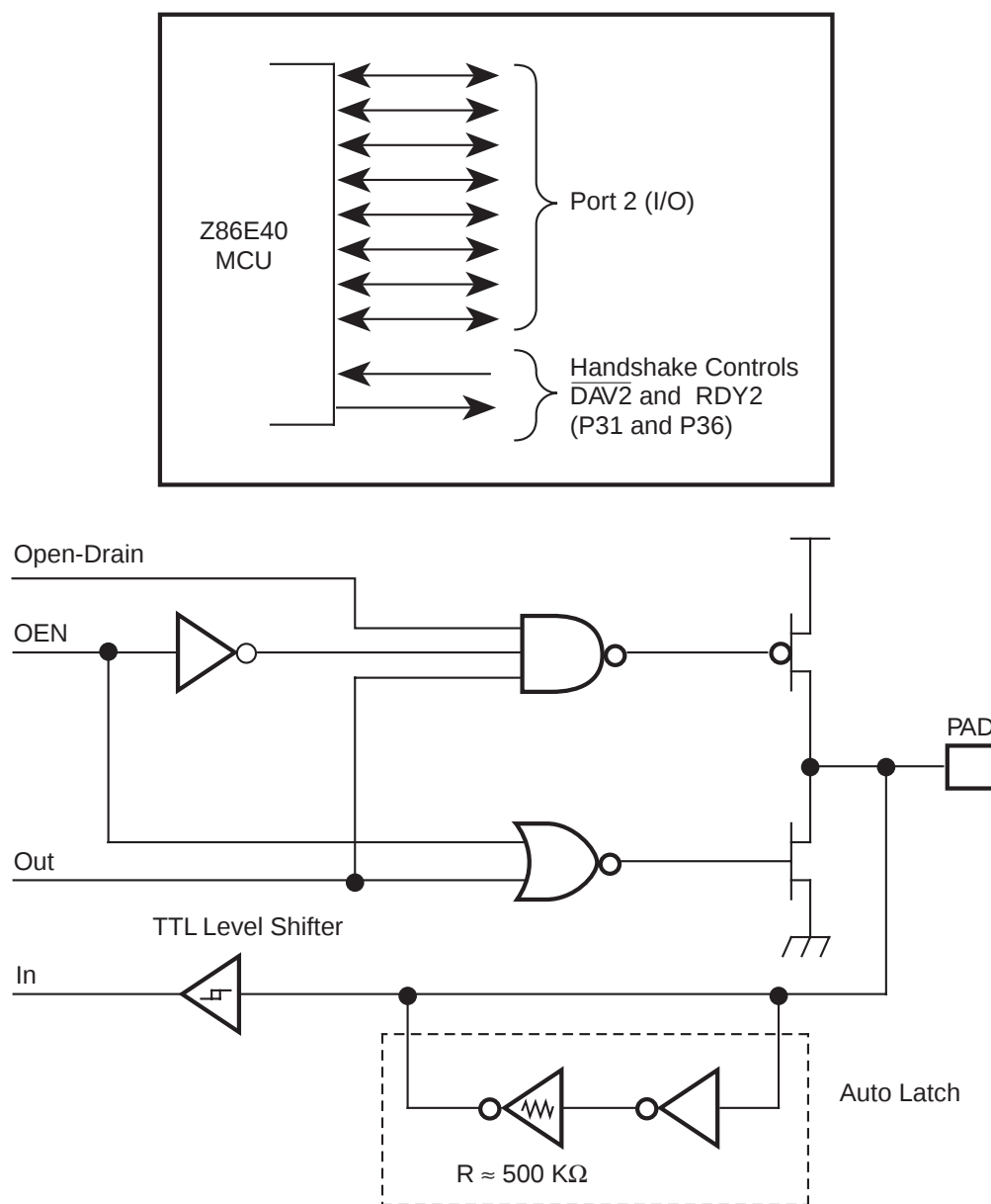


Figure 20. Port 2 Configuration

PIN FUNCTIONS (Continued)

Comparator Inputs. Port 3, P31, and P32, each have a comparator front end. The comparator reference voltage P33 is common to both comparators. In analog mode, P31 and P32 are the positive input of the comparators and P33 is the reference voltage of the comparators.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33–P31) that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Auto Latches are available on Port 0, Port 2, and P30. There are no Auto Latches on P31, P32, and P33.

Low EMI Emission. The Z86E40 can be programmed to operate in a low EMI Emission Mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Low EMI Oscillator.
- Internal SCLK/TCLK= XTAL operation limited to a maximum of 4 MHz – 250 ns cycle time, when Low EMI Oscillator is selected and system clock (SCLK = XTAL, SMR Reg. Bit D1 =1).
- **Note for emulation only:**
Do not set the emulator to emulate Port 1 in low EMI mode. Port 1 must always be configured in Standard Mode.

FUNCTIONAL DESCRIPTION (Continued)

Data Memory ($\overline{DM}$). In EPROM Mode, the Z86E40 can address up to 60 KB of external data memory beginning at location 4096. In ROMless mode, the Z86E40 can address up to 64 KB of data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/O function that can be

programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 23). The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory.

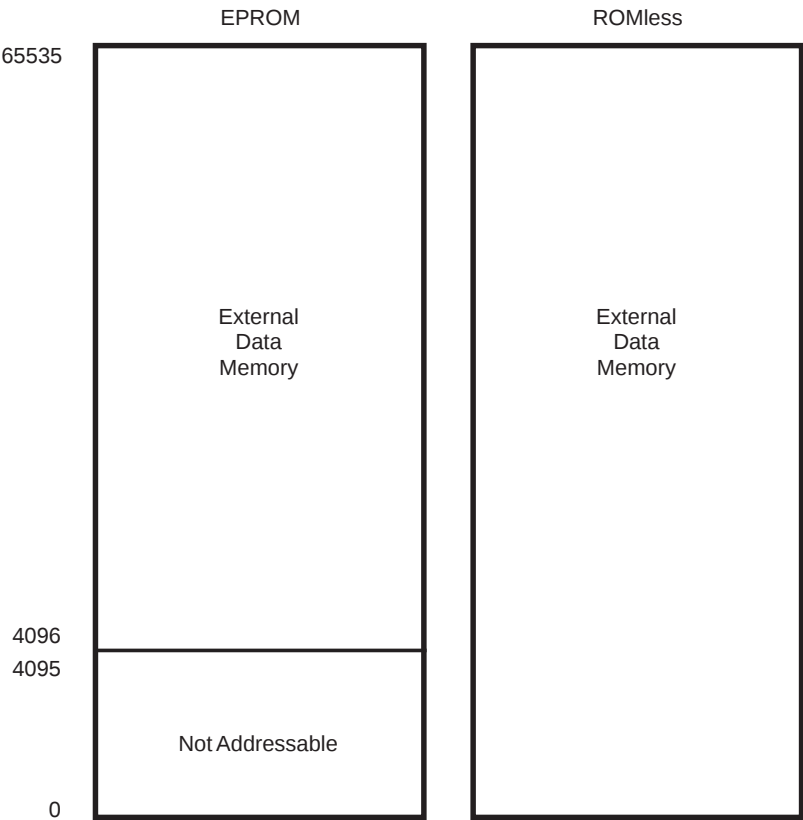


Figure 23. Data Memory Map

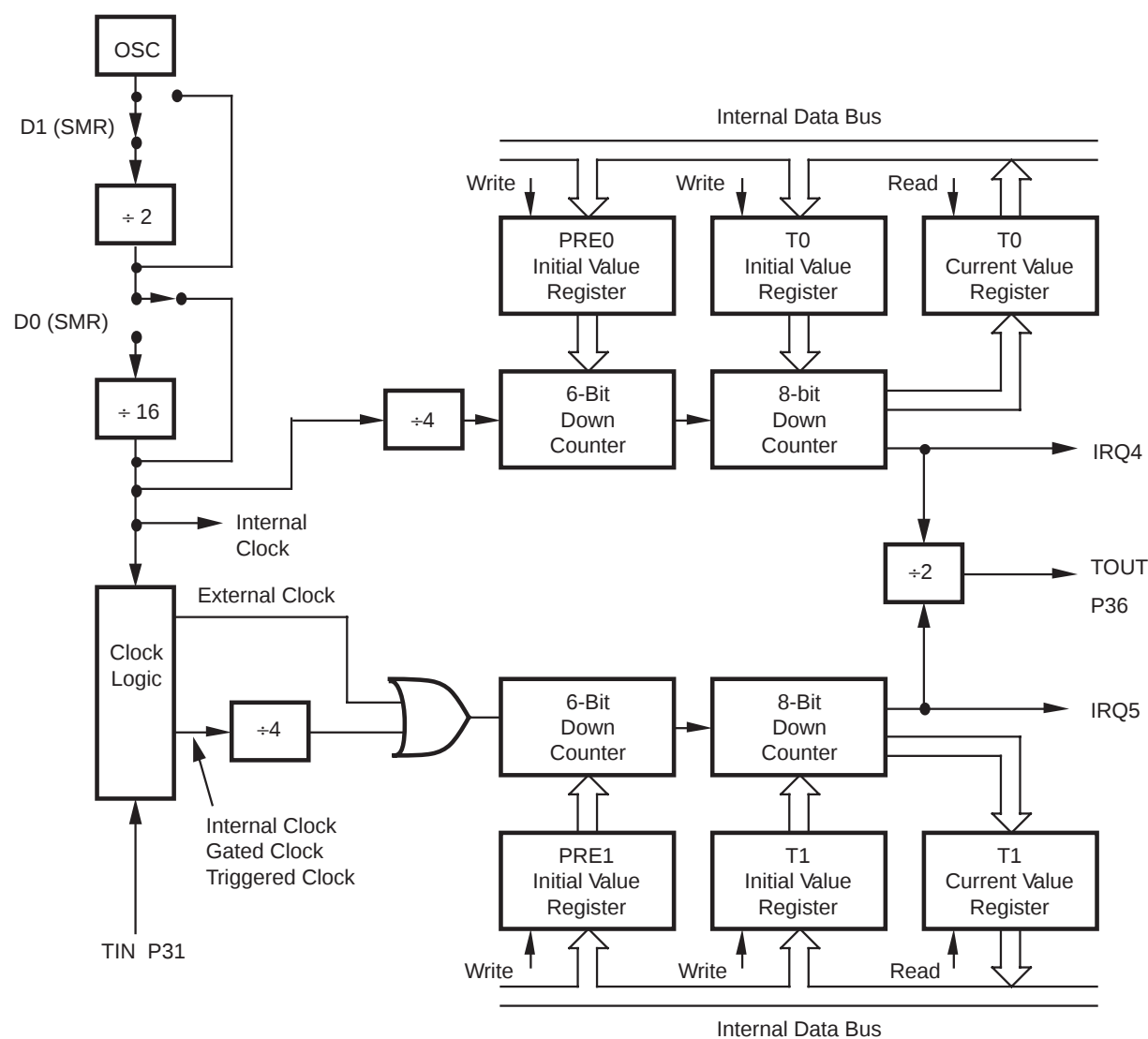


Figure 27. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

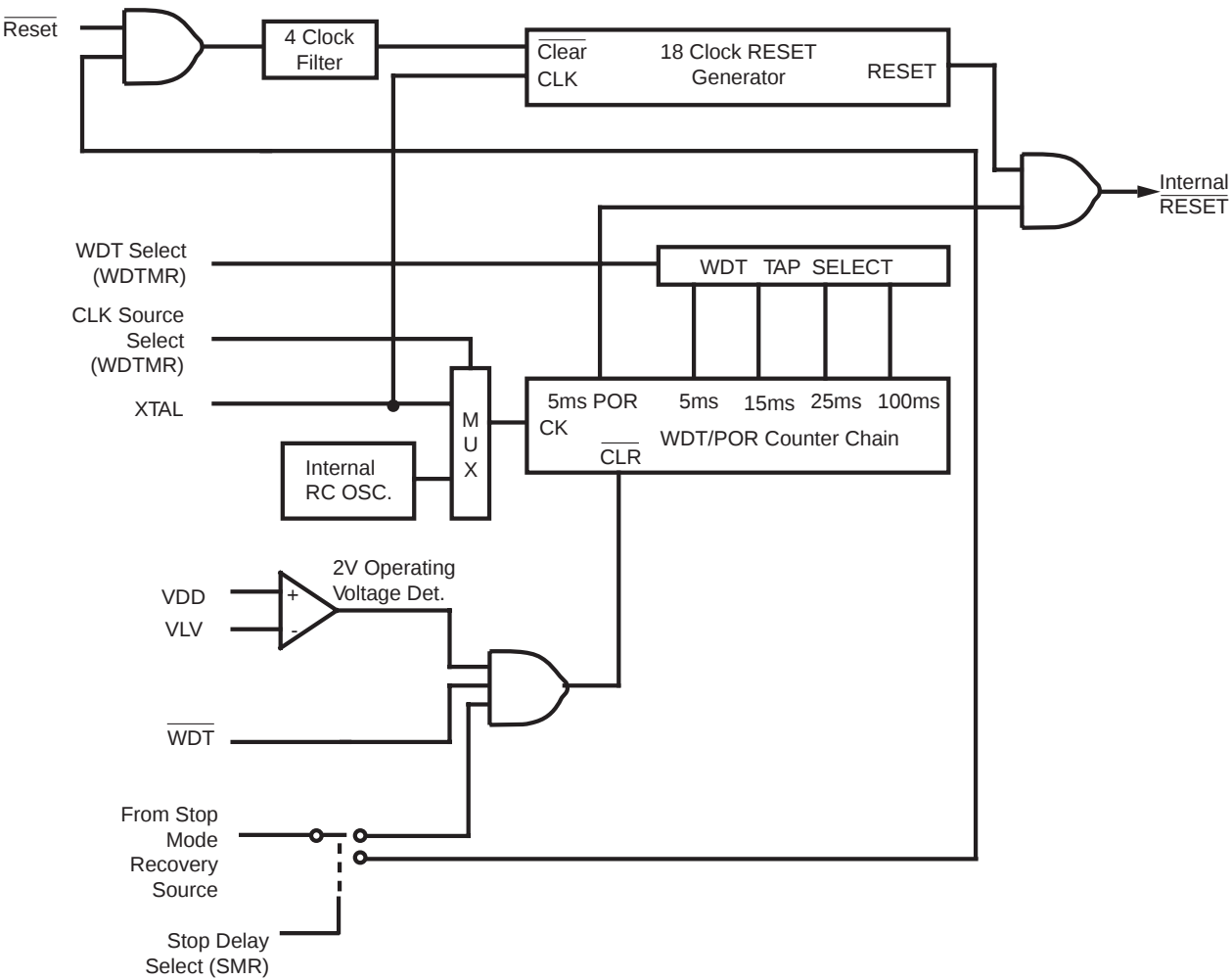


Figure 34. Resets and WDT

Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{LV} (Figure 35).

Note: V_{CC} must be in the allowed operating range prior to the minimum Power-On Reset time-out (T_{POR}).

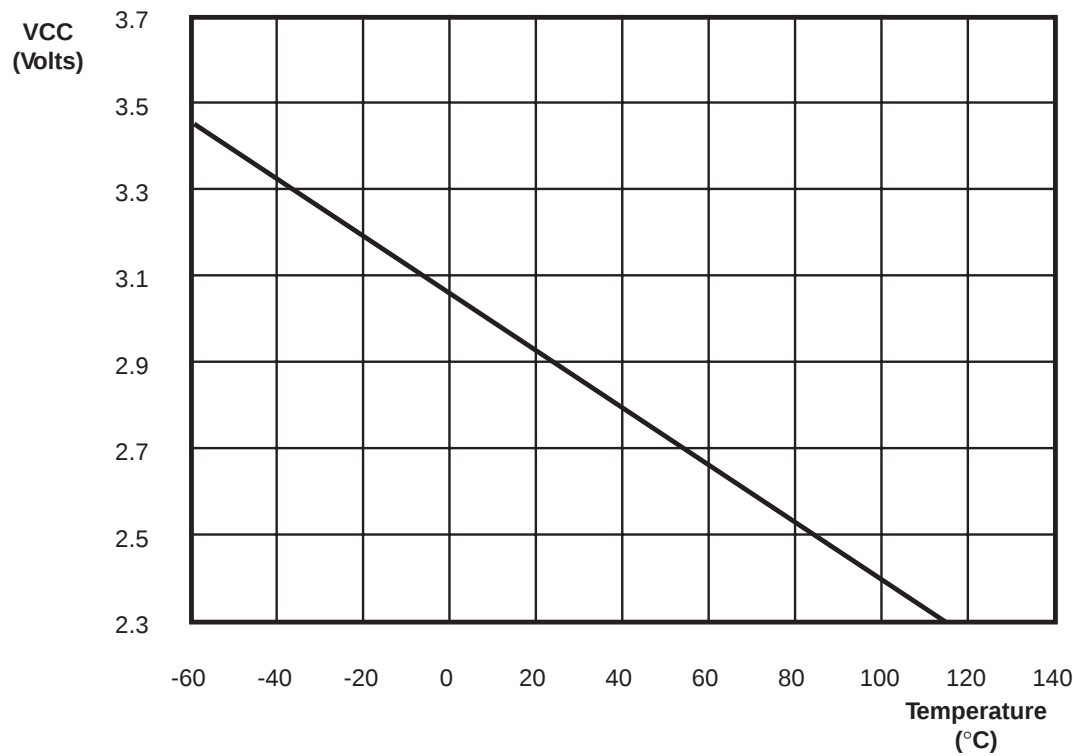


Figure 35. Typical Z86E40 V_{LV} Voltage vs. Temperature

FUNCTIONAL DESCRIPTION (Continued)

EPROM MODE

Table 14 shows the programming voltages of each programming mode. Table 15, and figures that follow show the programming timing of each programming mode. Figure 38 shows the circuit diagram of a Z86E40 programming adapter, which adapts from 2764A to Z86E40 and Figure 39 shows the Z86E30/E31 Programming Adapter Circuitry. Figure 40 shows the flowchart of an Intelligent Programming Algorithm, which is compatible with 2764A EPROM (Z86E40 is 4K EPROM, 2764A is 8K EPROM). Since the EPROM size of Z86E30/E31/E40 differs from 2764A, the programming address range has to be set from 0000H to 0FFFH for the Z86E30/E40 and 0000H to 07FFH for Z86E31. Otherwise, the upper portion of EPROM data will overwrite the lower portion of EPROM data. Figure 39 shows the adaptation from the 2764A to Z86E30/E31.

Note: EPROM Protect feature allows the LDC, LDCI, LDE, and LDEI instructions from internal program memory. A ROM lookup table can be used with this feature.

During programming, the V_{PP} input pin supplies the programming voltage and current to the EPROM. This pin is also used to latch which EPROM mode is to be used (R/W EPROM or R/W Option bits). The mode is set by placing the correct mode number on the least significant bits of the address and raising the EPM pin above V . After a setup time, the V_{PP} pin can then be raised or lowered. The latched EPROM mode will remain until the EPM pin is reduced below V_H .

Mode Name	Mode #	LSB Addr
EPROM R/W	0	0000
Option Bit R/W	3	0011

EPROM R/W mode allows the programming of the user mode program ROM.

Option Bit R/W allows the programming of the Z8 option bits. When the device is latched into Option Bit R/W mode, the address must then be changed to 63 decimals (000000111111 Binary). The Options are mapped into this address as follows:

Bit	Option
7	Unused
6	Unused
5	32 KHz XTAL Option
4	Permanent WDT
3	Auto Latch Disable
2	RC Oscillator Option
1	RAM Protect
0	ROM Protect

Table 14 gives the proper conditions for EPROM R/W operations, once the mode is latched.

FUNCTIONAL DESCRIPTION (Continued)

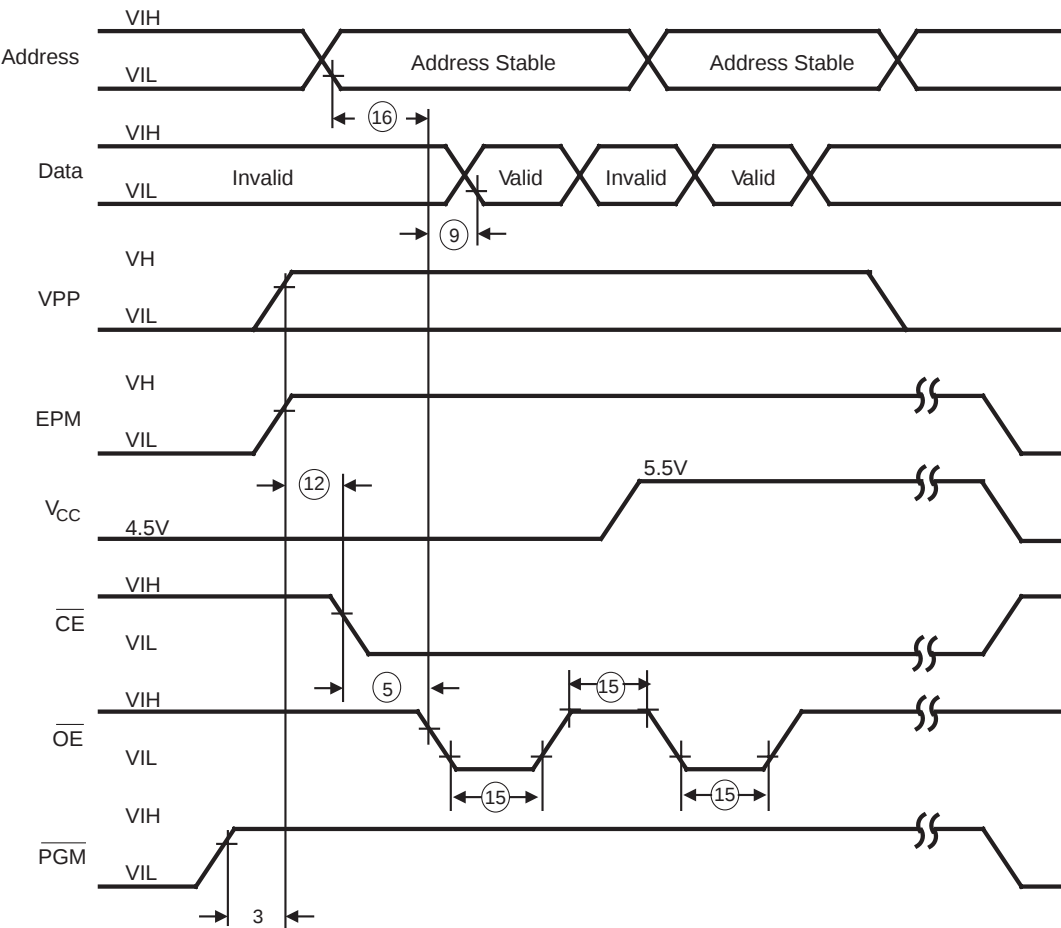


Figure 36. EPROM Read Mode Timing Diagram

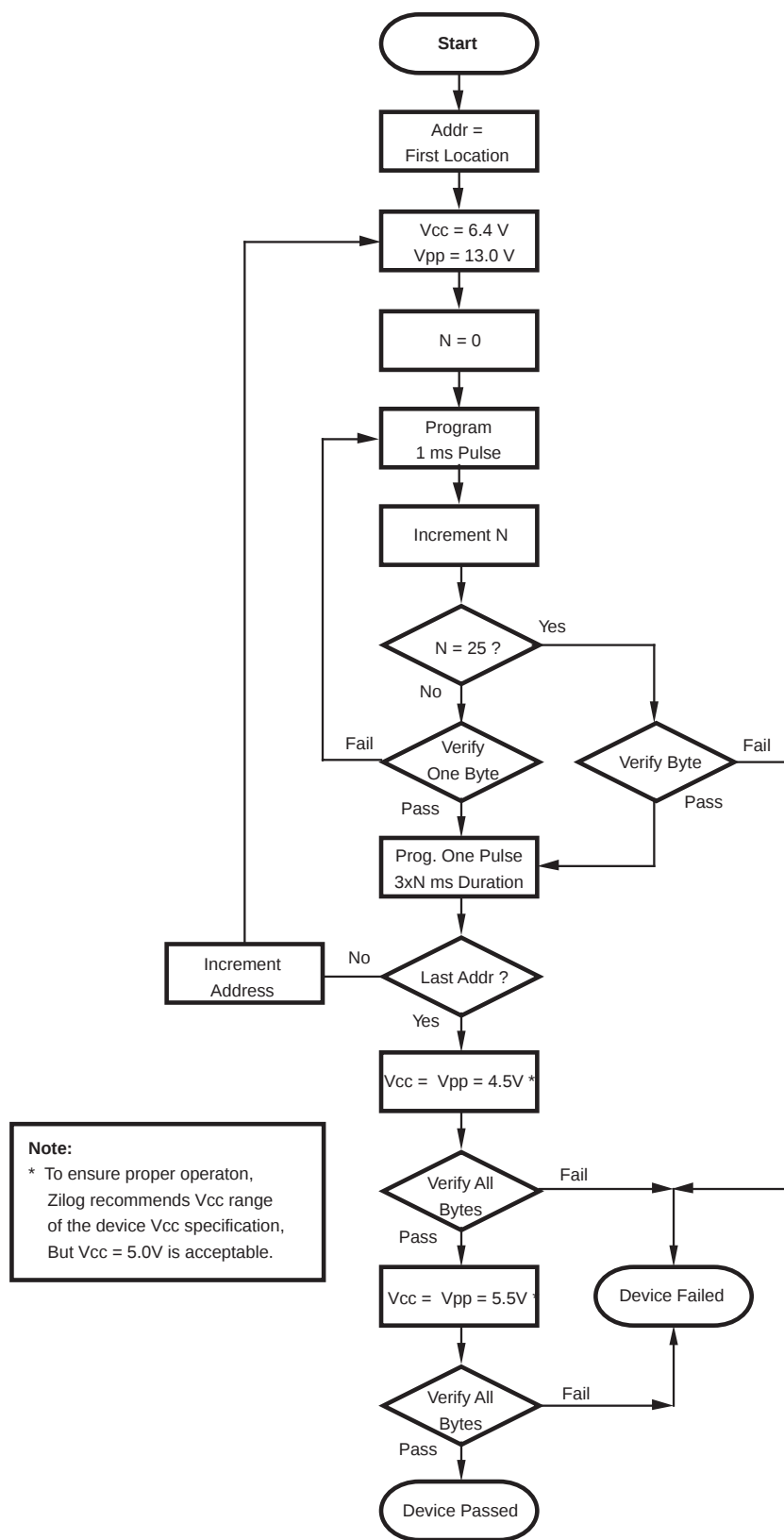


Figure 40. Z86E40 Programming Algorithm

EXPANDED REGISTER FILE CONTROL REGISTERS

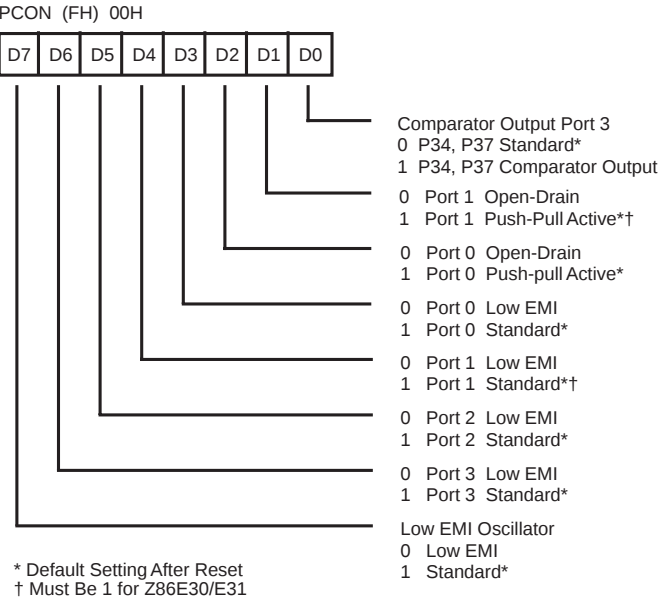


Figure 41. Port Configuration Register
Write Only

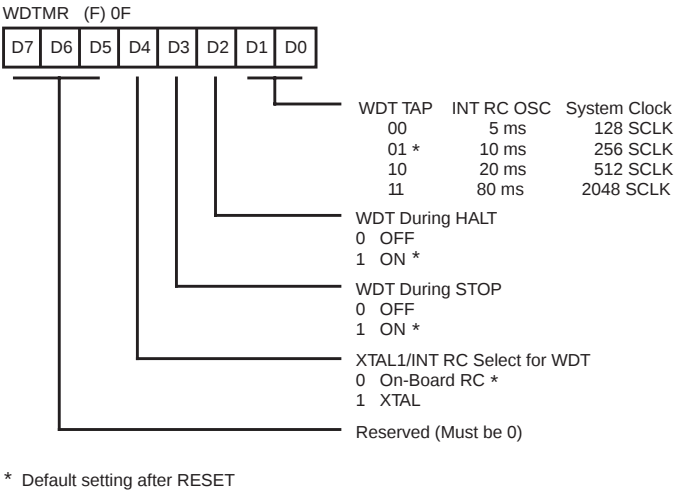


Figure 43. Watch-Dog Timer Mode Register
Write Only

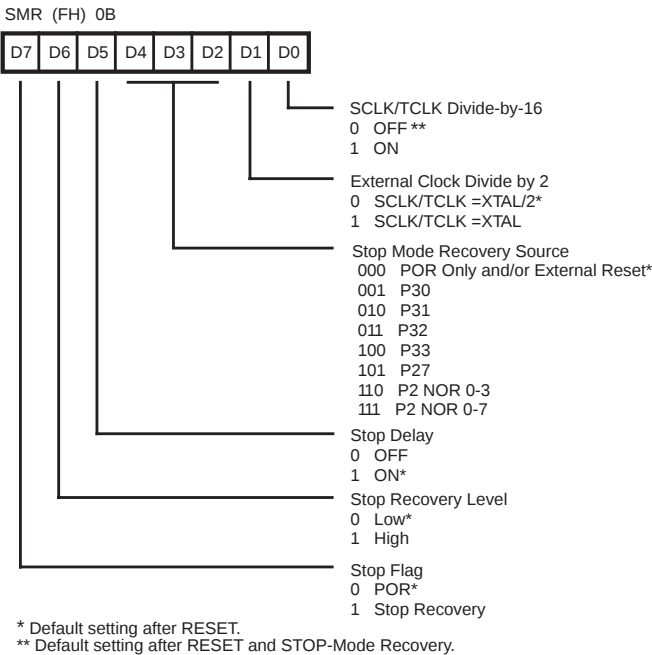


Figure 42. STOP-Mode Recovery Register
Write Only Except Bit D7, Which is Read Only

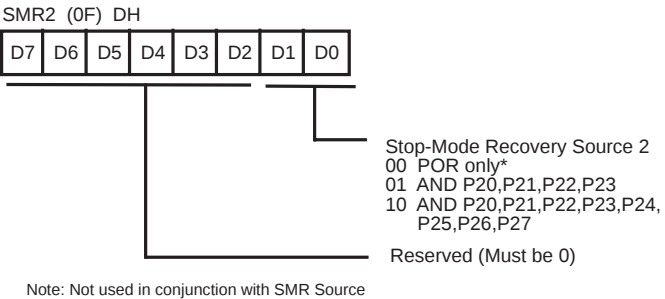


Figure 44. STOP-Mode Recovery Register 2
Write Only

Z8 CONTROL REGISTER DIAGRAMS (Continued)

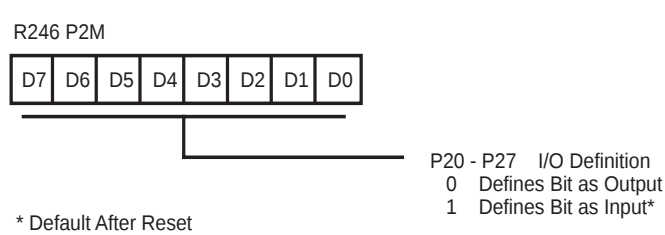


Figure 51. Port 2 Mode Register
F6H: Write Only

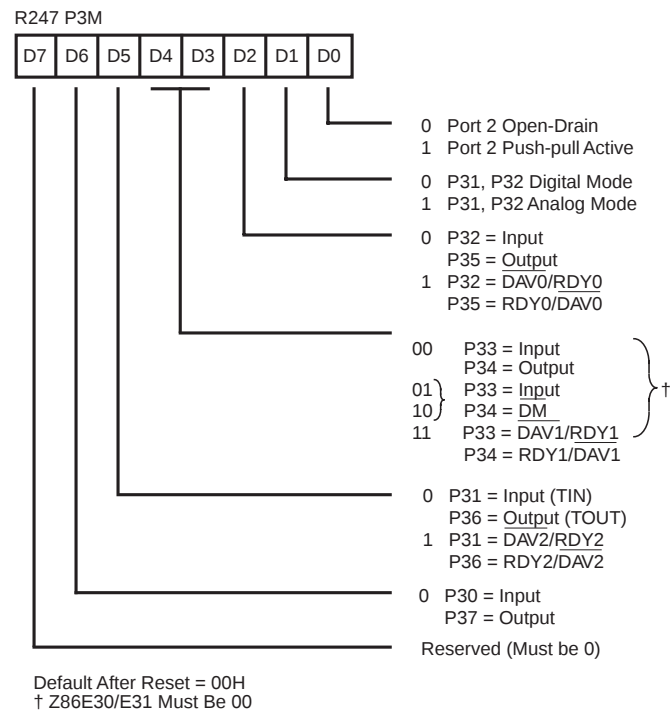


Figure 52. Port 3 Mode Register
F7H: Write Only

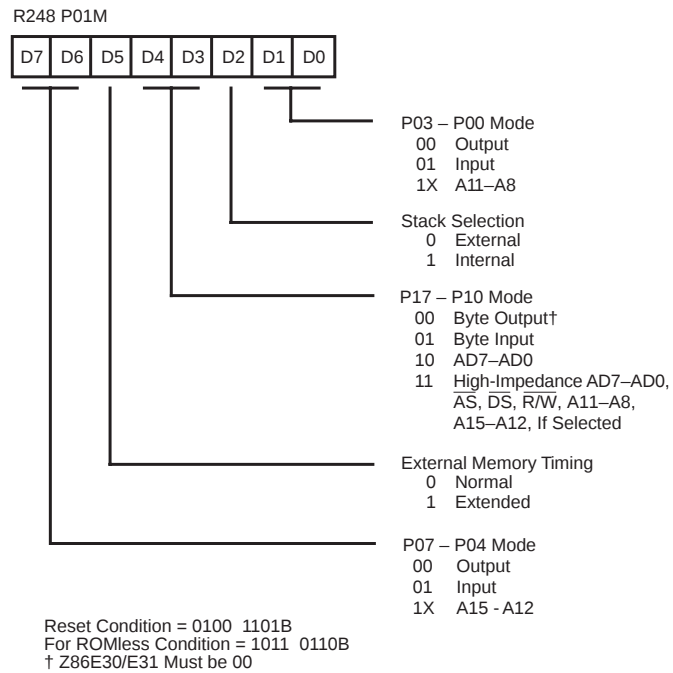


Figure 53. Port 0 and 1 Mode Register
F8H: Write Only
Z86E30/E31 Only

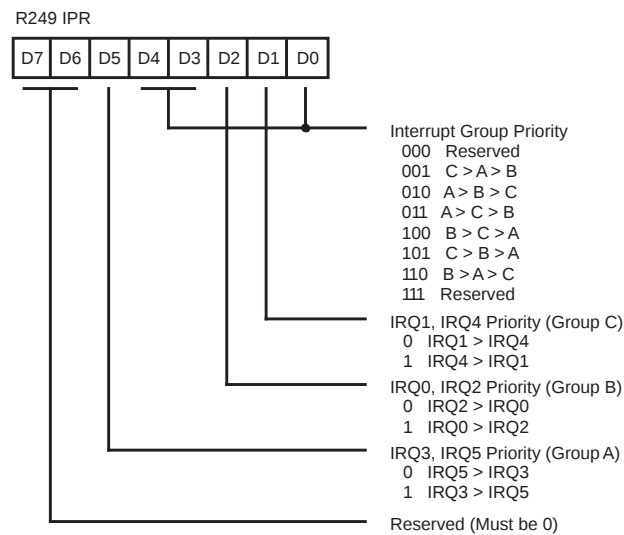


Figure 54. Interrupt Priority Register
F9H: Write Only

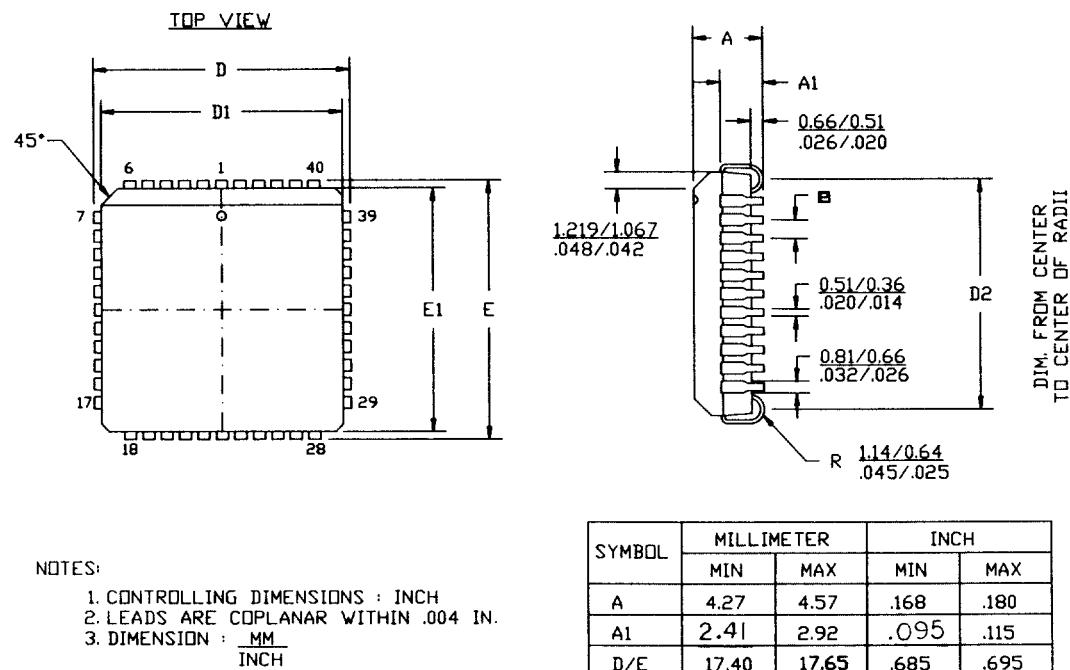


Figure 62. 44-Pin PLCC Package Diagram

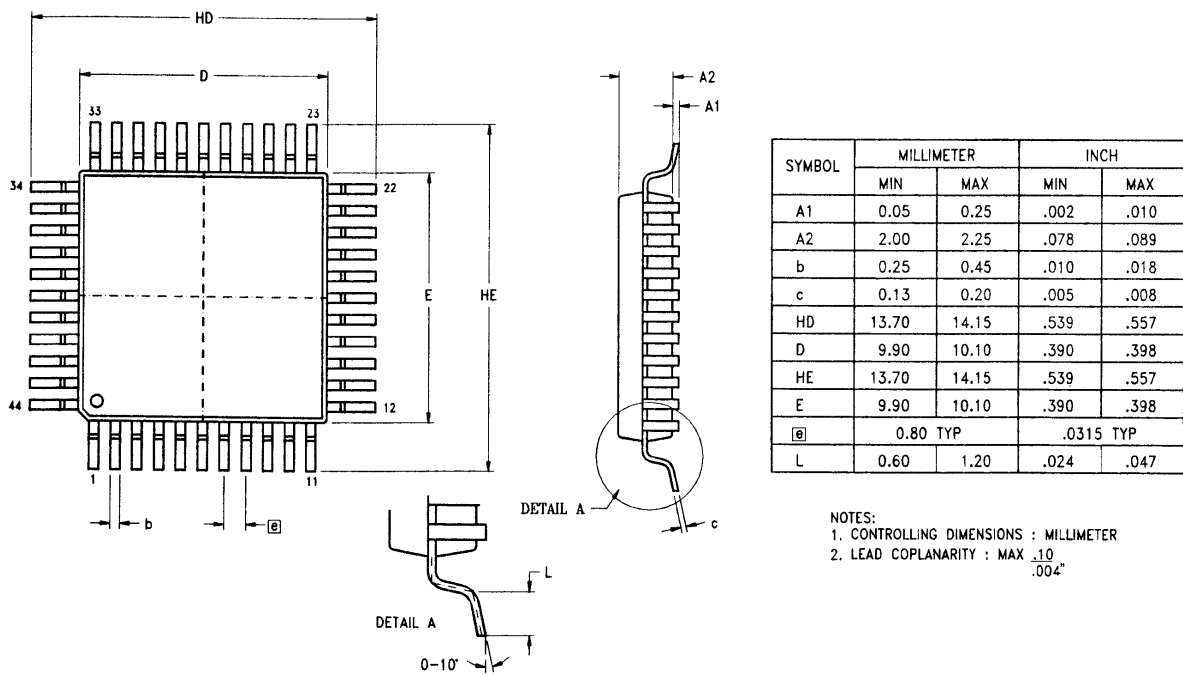


Figure 63. 44-Pin LQFP Package Diagram