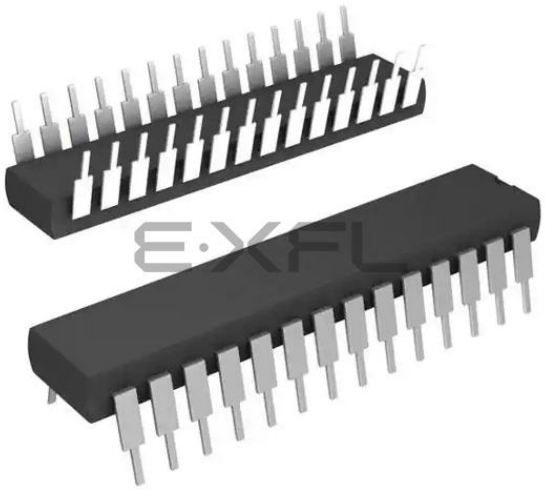

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	2KB (2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e3116pec

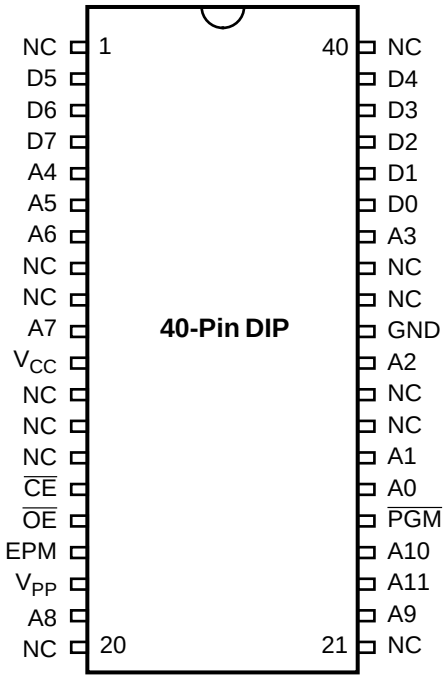


Figure 6. 40-Pin DIP Pin Configuration EPROM Mode

Table 4. 40-Pin DIP Package Pin Identification EPROM Mode

Pin #	Symbol	Function	Direction
1	NC	No Connection	
2–4	D5–D7	Data 5,6,7	In/Output
5–7	A4–A6	Address 4,5,6	Input
8–9	NC	No Connection	
10	A7	Address 7	Input
11	V_{CC}	Power Supply	
12–14	NC	No Connection	
15	$\overline{CE}$	Chip Select	Input
16	$\overline{OE}$	Output Enable	Input
17	EPM	EPROM Prog. Mode	Input
18	V_{PP}	Prog. Voltage	Input
19	A8	Address 8	Input
20–21	NC	No Connection	
22	A9	Address 9	Input
23	A11	Address 11	Input
24	A10	Address 10	Input
25	$\overline{PGM}$	Prog. Mode	Input
26–27	A0–A1	Address 0,1	Input
28–29	NC	No Connection	
30	A2	Address 2	Input
31	GND	Ground	
32–33	NC	No Connection	
34	A3	Address 3	Input
35–39	D0–D4	Data 0,1,2,3,4	In/Output
40	NC	No Connection	

PIN IDENTIFICATION (Continued)

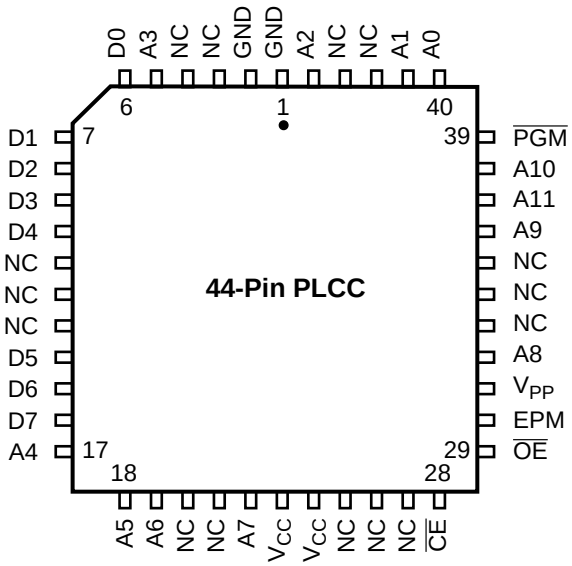


Figure 7. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Table 5. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Pin #	Symbol	Function	Direction
1–2	GND	Ground	
3–4	NC	No Connection	
5	A3	Address 3	Input
6–10	D0–D4	Data 0,1,2,3,4	In/Output
11–13	NC	No Connection	
14–16	D5–D7	Data 5,6,7	In/Output
17–19	A4–A6	Address 4,5,6	Input
20–21	NC	No Connection	
22	A7	Address 7	Input
23–24	V_{CC}	Power Supply	
25–27	NC	No Connection	
28	$\overline{CE}$	Chip Select	Input
29	$\overline{OE}$	Output Enable	Input
30	EPM	EPROM Prog. Mode	Input

Table 5. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Pin #	Symbol	Function	Direction
31	V_{PP}	Prog. Voltage	Input
32	A8	Address 8	Input
33–35	NC	No Connection	
36	A9	Address 9	Input
37	A11	Address 11	Input
38	A10	Address 10	Input
39	$\overline{PGM}$	Prog. Mode	Input
40–41	A0,A1	Address 0,1	Input
42–43	NC	No Connection	
44	A2	Address 2	Input

PIN IDENTIFICATION (Continued)

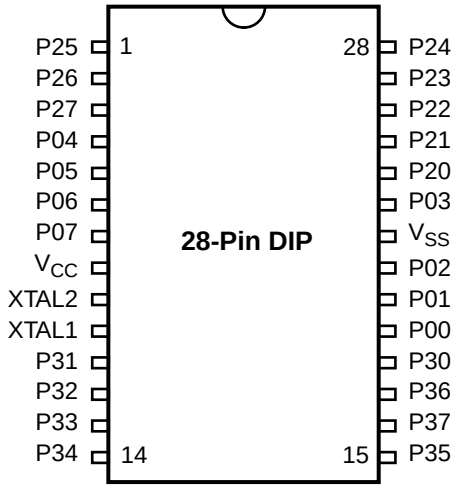


Figure 9. Standard Mode 28-Pin DIP/SOIC Pin Configuration

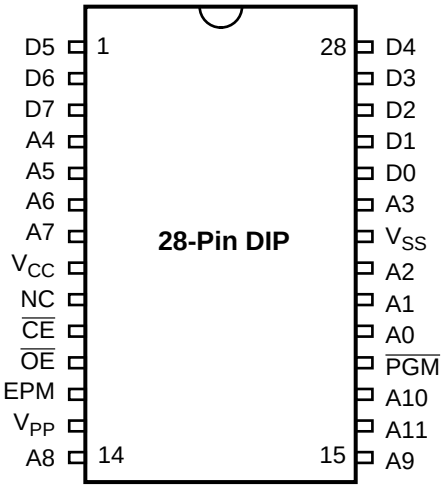


Figure 10. EPROM Programming Mode 28-Pin DIP/SOIC Pin Configuration

Table 7. 28-Pin DIP/SOIC/PLCC Pin Identification*

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Pins 5,6,	In/Output
4–7	P04–P07	Port 0, Pins 4,5,6,7	In/Output
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11–13	P31–P33	Port 3, Pins 1,2,3	Input
14–15	P34–P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19–21	P00–P02	Port 0, Pins 0,1,2	In/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24–28	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output

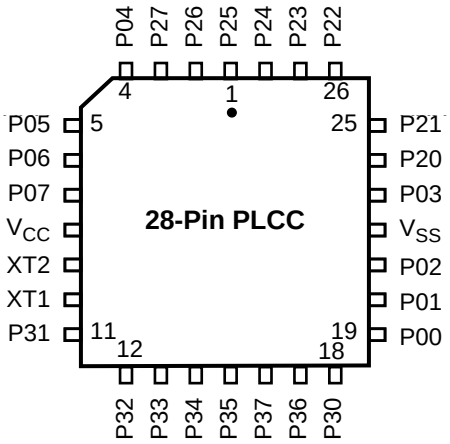


Figure 11. Standard Mode 28-Pin PLCC Pin Configuration

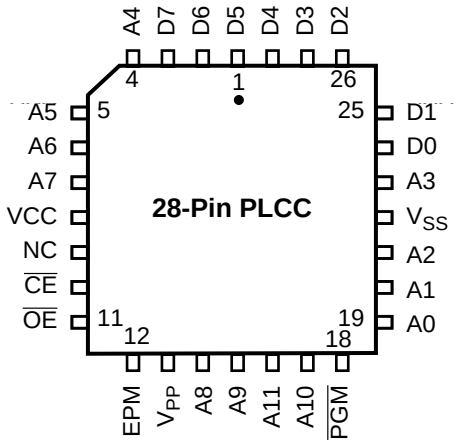


Figure 12. EPROM Programming Mode 28-Pin PLCC Pin Configuration

Table 8. 28-Pin EPROM Pin Identification

Pin #	Symbol	Function	Direction
1–3	D5–D7	Data 5,6,7	In/Output
4–7	A4–A7	Address 4,5,6,7	Input
8	V_{CC}	Power Supply	
9	NC	No connection	
10	$\overline{CE}$	Chip Select	Input
11	$\overline{OE}$	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V_{PP}	Prog. Voltage	Input
14–15	A8–A9	Address 8,9	Input
16	A11	Address 11	Input
17	A10	Address 10	Input
18	$\overline{PGM}$	Prog. Mode	Input
19–21	A0–A2	Address 0,1,2	Input
22	V_{SS}	Ground	
23	A3	Address 3	Input
24–28	D0–D4	Data 0,1,2,3,4	In/Output

Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
			T_A=–40 °C to +105 °C					
V_{CH}	Clock Input High Voltage	4.5V 5.5V	0.7 V_{CC} 0.7 V_{CC}	V_{CC}+0.3 V_{CC}+0.3	2.5 2.5	V V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V 5.5V	GND-0.3 GND-0.3	0.2 V_{CC} 0.2 V_{CC}	1.5 1.5	V V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V 5.5V	0.7 V_{CC} 0.7 V_{CC}	V_{CC}+0.3 V_{CC}+0.3	2.5 2.5	V V		
V_{IL}	Input Low Voltage	4.5V 5.5V	GND-0.3 GND-0.3	0.2 V_{CC} 0.2 V_{CC}	1.5 1.5	V V		
V_{OH}	Output High Voltage Low EMI Mode	4.5V 5.5V	V_{CC} -0.4 V_{CC} -0.4		4.8 4.8	V V	I_{OH} = – 0.5 mA I_{OH} = – 0.5 mA	8 8
V_{OH1}	Output High Voltage	4.5V 4.5V	V_{CC} -0.4 V_{CC} -0.4		4.8 4.8	V V	I_{OH} = -2.0 mA I_{OH} = -2.0 mA	8 8
V_{OL}	Output Low Voltage Low EMI Mode	4.5V 5.5V		0.4 0.4	0.2 0.2	V V	I_{OL} = 1.0 mA I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	4.5V 5.5V		0.4 0.4	0.1 0.1	V V	I_{OL} = + 4.0 mA I_{OL} = +4.0 mA	8 8
V_{OL2}	Output Low Voltage	4.5V 5.5V		1.2 1.2	0.5 0.5	V V	I_{OL} = + 12 mA I_{OL} = + 12 mA	8 8
V_{RH}	Reset Input High Voltage	3.5V 5.5V	.8 V_{CC} .8 V_{CC}	V_{CC} V_{CC}	1.7 2.1	V V		13 13
V_{OLR}	Reset Output Low Voltage	3.5V 5.5V		0.6 0.6	0.3 0.2	V V	I_{OL} = 1.0 mA I_{OL} = 1.0 mA	13 13
V_{OFFSET}	Comparator Input Offset Voltage	4.5V 5.5V		25 25	10 10	mV mV		
V_{ICR}	Input Common Mode Voltage Range	4.5V 5.5V	0 0	V_{CC}-1.5V V_{CC}-1.5V		V V		10 10
I_{IL}	Input Leakage	4.5V 5.5V	-1 -1	2 2	<1 <1	µA µA	V_{IN} = 0V, V_{CC} V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V 5.5V	-1 -1	2 2	<1 <1	µA µA	V_{IN} = 0V, V_{CC} V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	4.5V 5.5V	-18 -18	-180 -180	-112 -112	µA µA		
I_{CC}	Supply Current	4.5V 5.5V		25 25	20 20	mA mA	@ 16 MHz @ 16 MHz	4,5 4,5
I_{CC1}	Standby Current Halt Mode	4.5V 5.5V		8 8	3.7 3.7	mA mA	V_{IN} = 0V, V_{CC} @ 16 MHz V_{IN} = 0V, V_{CC} @ 16 MHz	4,5 4,5
I_{CC2}	Standby Current (Stop Mode)	4.5V 5.5V		10 10	2 3	µA µA	V_{IN} = 0V, V_{CC} V_{IN} = 0V, V_{CC}	6,11,14 6,11,14
I_{ALL}	Auto Latch Low Current	4.5V 5.5V	1.4 1.4	20 20	4.7 4.7	µA µA	0V < V_{IN} < V_{CC} 0V < V_{IN} < V_{CC}	9 9

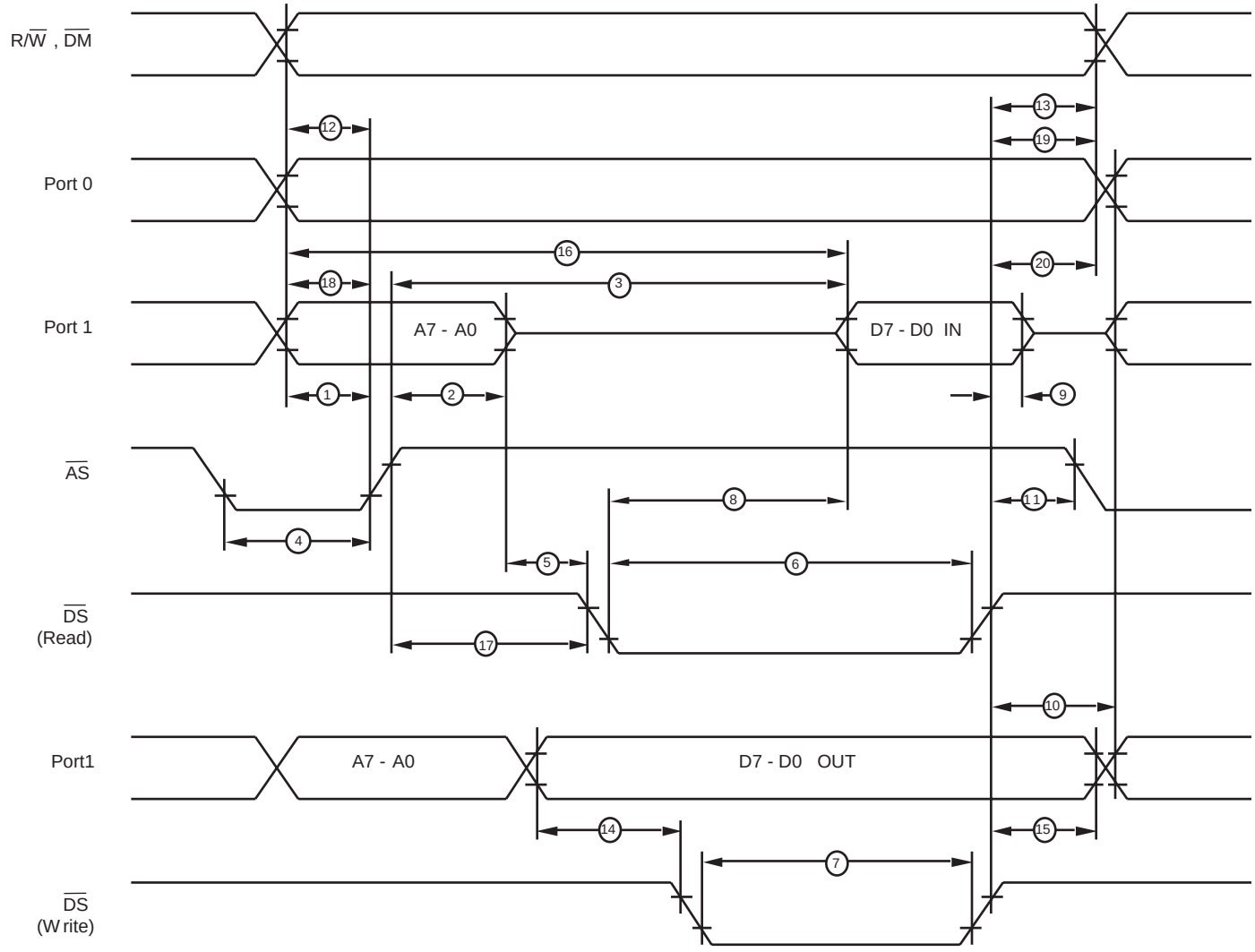


Figure 14. External I/O or Memory Read/Write Timing
Z86E40 Only

			T_A = -40°C to 105°C 16 MHz Note [3]				
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	4.5V 5.5V	25 25		ns ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	4.5V 5.5V	35 35		ns ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	4.5V 5.5V		180 180	ns ns	1,2
4	TwAS	$\overline{AS}$ Low Width	4.5V 5.5V	40 40		ns ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	4.5V 5.5V	0 0		ns ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	4.5V 5.5V	135 135		ns ns	1,2
7	TwDSW	$\overline{DS}$ (Write) Low Width	4.5V 5.5V	80 80		ns ns	1,2
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid	4.5V 5.5V		75 75	ns ns	1,2
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	4.5V 5.5V	0 0		ns ns	2
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	4.5V 5.5V	50 50		ns ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	4.5V 5.5V	35 35		ns ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	4.5V 5.5V	25 25		ns ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	4.5V 5.5V	35 35		ns ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	4.5V 5.5V	55 55	25 25	ns ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	4.5V 5.5V	35 35		ns ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	4.5V 5.5V		230 230	ns ns	1,2
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	4.5V 5.5V	45 45		ns ns	2
18	TdDM(AS)	/DM Valid to $\overline{AS}$ Fall Delay	4.5V 5.5V	30 30		ns ns	2
20	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	4.5V 5.5V	35 35		ns ns	

Notes:

1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

Additional Timing Table (Divide-By-One Mode)

				T_A = 0 °C to +70 °C		T_A = -40 °C to +105 °C			
				4 MHz		4 MHz			
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.5V	250	DC	250	DC	ns	1,7,8
			5.5V	250	DC	250	DC	ns	1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		25		25	ns	1,7,8
			5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	3.5V	100		100		ns	1,7,8
			5.5V	100		100		ns	1,7,8
4	TwTinL	Timer Input Low Width	3.5V	100		100		ns	1,7,8
			5.5V	70		70		ns	1,7,8
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC			1,7,8
			5.5V	5TpC		5TpC			1,7,8
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC			1,7,8
			5.5V	8TpC		8TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns	1,7,8
			5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low Time	3.5V	100		100		ns	1,2,7,8
			5.5V	70		70		ns	1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC			1,3,7,8
			5.5V	5TpC		5TpC			1,3,7,8
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC			1,2,7,8
			5.5V	5TpC		5TpC			1,2,7,8
10	Twsm	STOP Mode Recovery Width Spec	3.5V	12		12		ns	4,8
			5.5V	12		12		ns	4,8
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC		4,8,9
			5.5V		5TpC				

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31–P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 1, POR STOP Mode Delay is on.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V and the V_{CC} voltage specification of 3.5V guarantees 3.5V only.
7. SMR D1 = 0.
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

PIN FUNCTIONS

EPROM Programming Mode

D7–D0 Data Bus. The data can be read from or written to external memory through the data bus.

A11–A0 Address Bus. During programming, the EPROM address is written to the address bus.

V_{CC} Power Supply. This pin must supply 5V during the EPROM read mode and 6V during other modes.

$\overline{CE}$ Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

$\overline{OE}$ Output Enable (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM EPROM Program Mode. This pin controls the different EPROM Program Mode by applying different voltages.

V_{PP} Program Voltage. This pin supplies the program voltage.

$\overline{PGM}$ Program Mode (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if excessive noise surges above V_{CC} occur on pins XTAL1 and $\overline{RESET}$.

In addition, processor operation of Z8 OTP devices may be affected by excessive noise surges on the V_{PP}, $\overline{CE}$, $\overline{EPM}$, $\overline{OE}$ pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{CC}
- Adding a capacitor to the affected pin

Standard Mode

XTAL Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network, or external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network to the on-chip oscillator output.

R/$\overline{W}$ Read/Write (output, write Low). The R/$\overline{W}$ signal is Low when the CCP is writing to the external program or data memory (Z86E40 only).

$\overline{RESET}$ Reset (input, active Low). Reset will initialize the MCU. Reset is accomplished either through Power-On, Watch-Dog Timer reset, STOP-Mode Recovery, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin low for the POR time. Any devices driving the reset line must be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. After the POR time, $\overline{RESET}$ is a Schmitt-triggered input.

To avoid asynchronous and noisy reset problems, the Z86E40 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. During the reset cycle, $\overline{DS}$ is held active Low while $\overline{AS}$ cycles at a rate of TpC/2. Program execution begins at location 000CH, 5–10 TpC cycles after $\overline{RESET}$ is released. For Power-On Reset, the reset output time is 5 ms. The Z86E40 does not reset WDTMR, SMR, P2M, and P3M registers on a STOP-Mode Recovery operation.

$\overline{ROMless}$ (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90/C89 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC}, the device functions normally as a Z8 ROM version).

Note: When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC}.

Port 0 (P07–P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble programmed. Either nibble output that can be globally programmed as push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can be placed under handshake control. In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. In ROMless mode, after a hardware reset, Port 0 is configured as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode. In ROM mode, Port 0 is defined as input after reset.

Port 0 can be set in the High-Impedance Mode if selected as an address output state, along with Port 1 and the control signals $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$ (Figure 18).

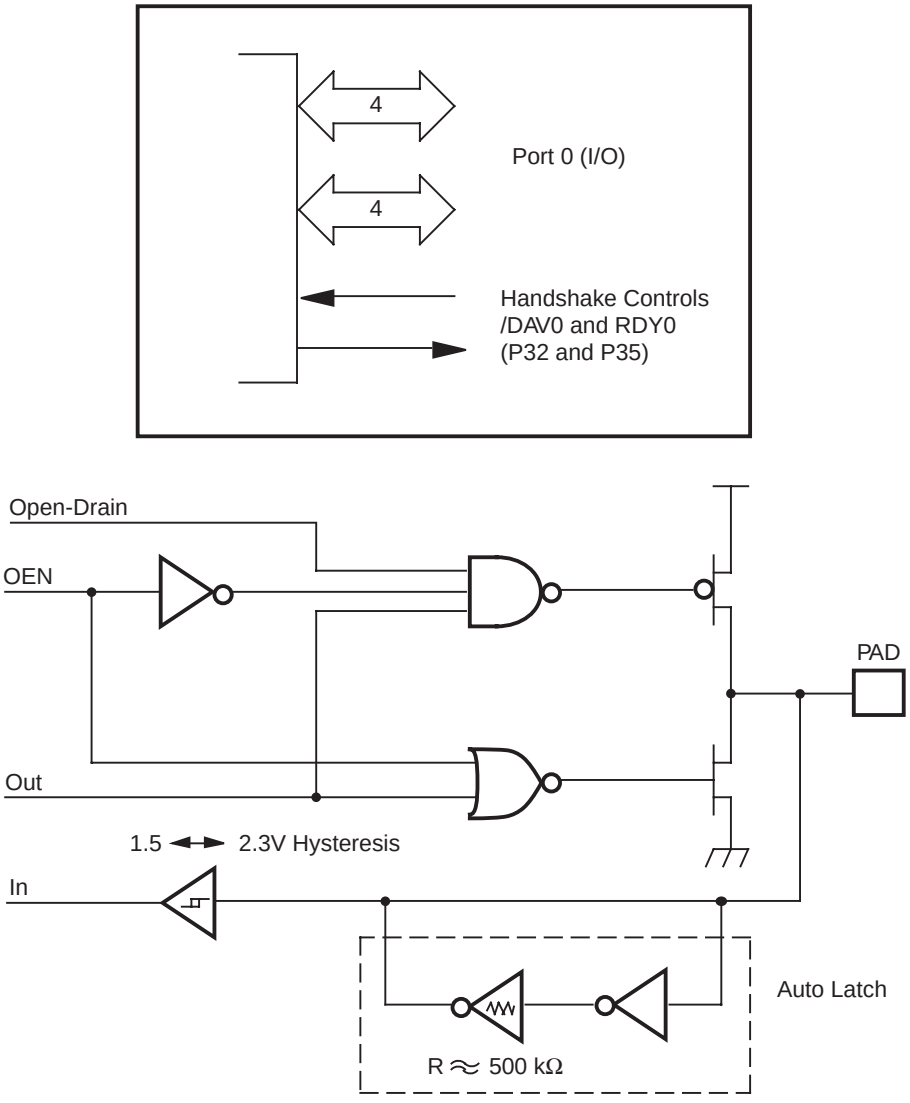


Figure 18. Port 0 Configuration

Port 2 (P27–P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control.

In Handshake Mode, Port 3 lines P31 and P36 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2 (Figure 20).

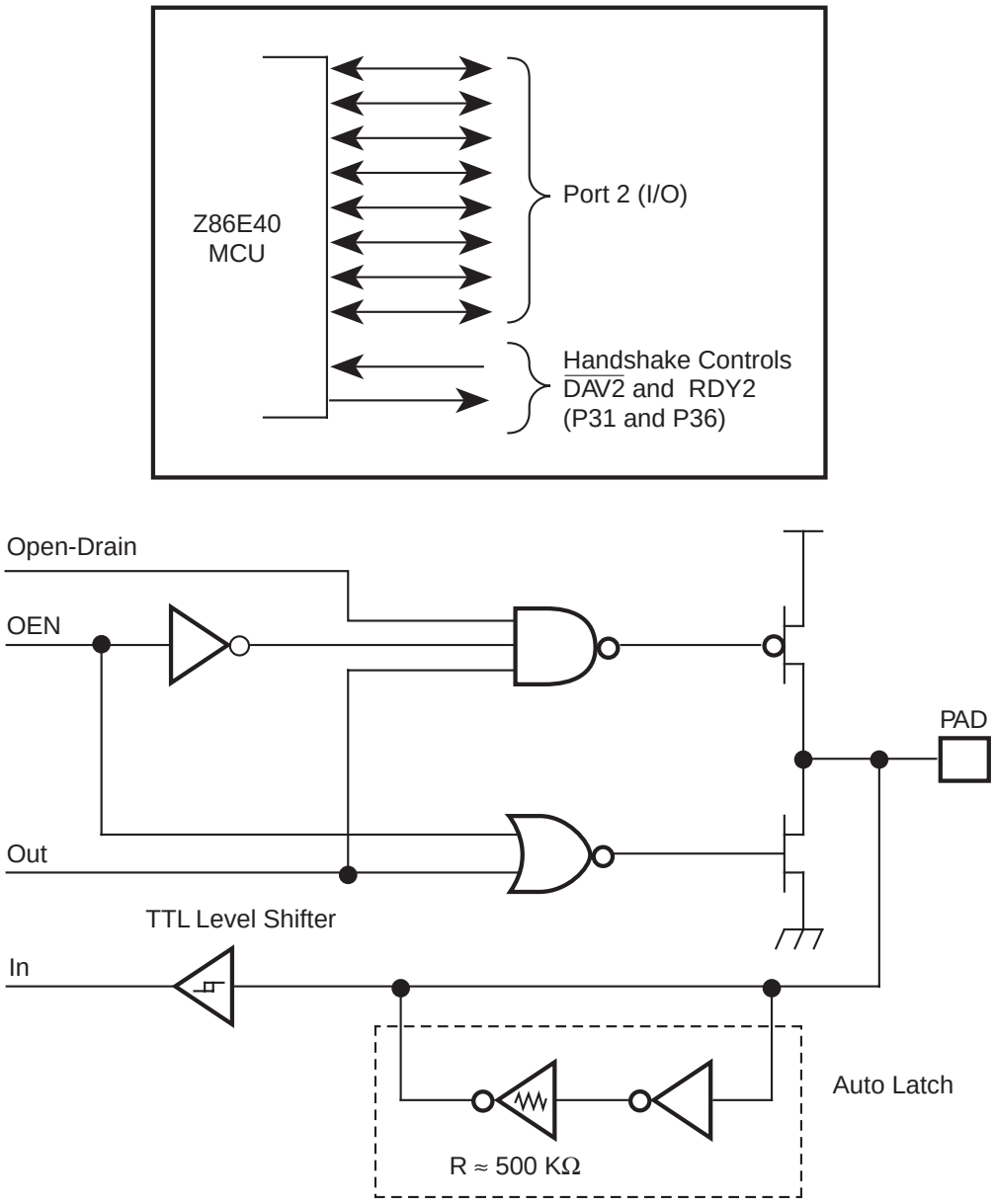


Figure 20. Port 2 Configuration

FUNCTIONAL DESCRIPTION (Continued)

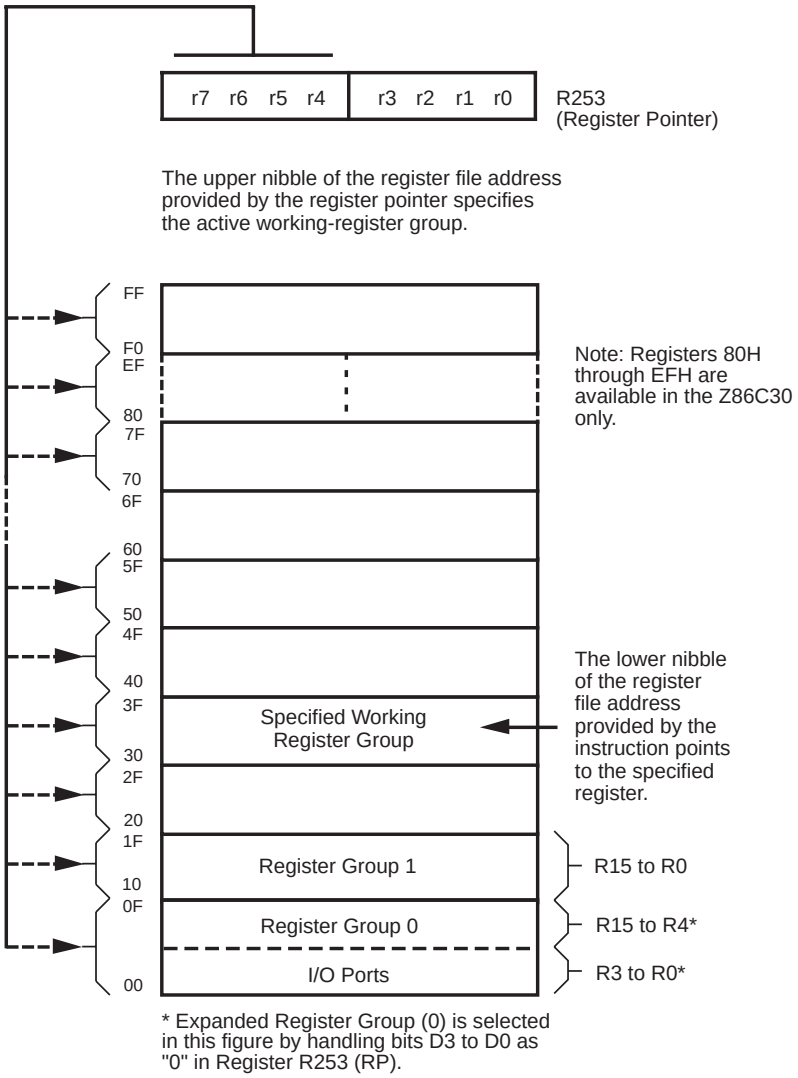


Figure 25. Register Pointer

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The MCU has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 28). The six sources are divided as follows: four sources are claimed by Port 3 lines P33–P30) and two in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 10).

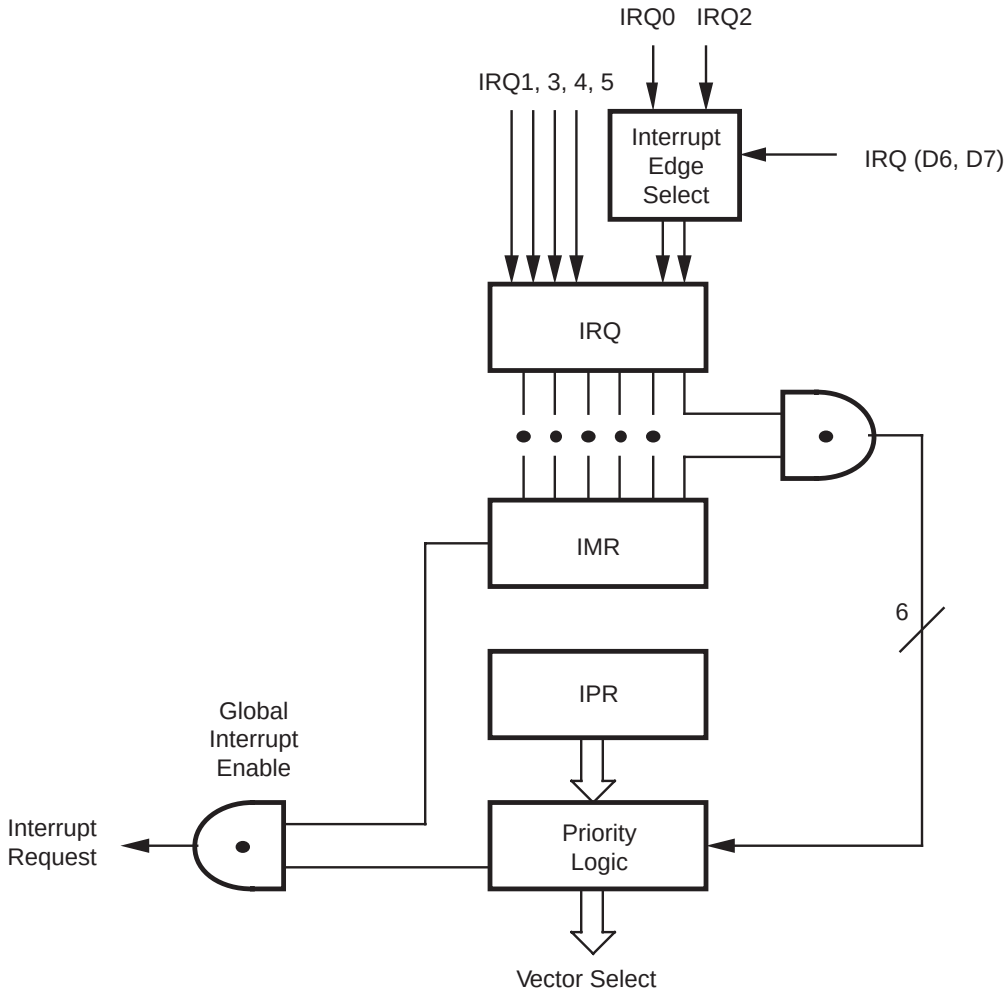


Figure 28. Interrupt Block Diagram

Table 10. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	$\overline{DAV0}$, IRQ0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	$\overline{DAV2}$, IRQ2, T_{IN}	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Falling Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	TI	10, 11	Internal

FUNCTIONAL DESCRIPTION (Continued)

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status
2. Stop-Mode Recovery (if D5 of SMR=0)
3. WDT time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP mode Register (SMR) determines whether the POR timer is bypassed after STOP-Mode Recovery (typical for an external clock and RC/LC oscillators with fast start up times).

HALT. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (Opcode=FFH) immediately before the appropriate sleep instruction, that is:

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP Mode
                or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. STOP Mode is terminated by one of the following resets: either by WDT time-out, POR, a Stop-Mode Recovery Source, which is defined by the SMR register or external reset. This causes the processor to restart the application program at address 000CH.

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2 and 3, and low EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00 (Figure 30).

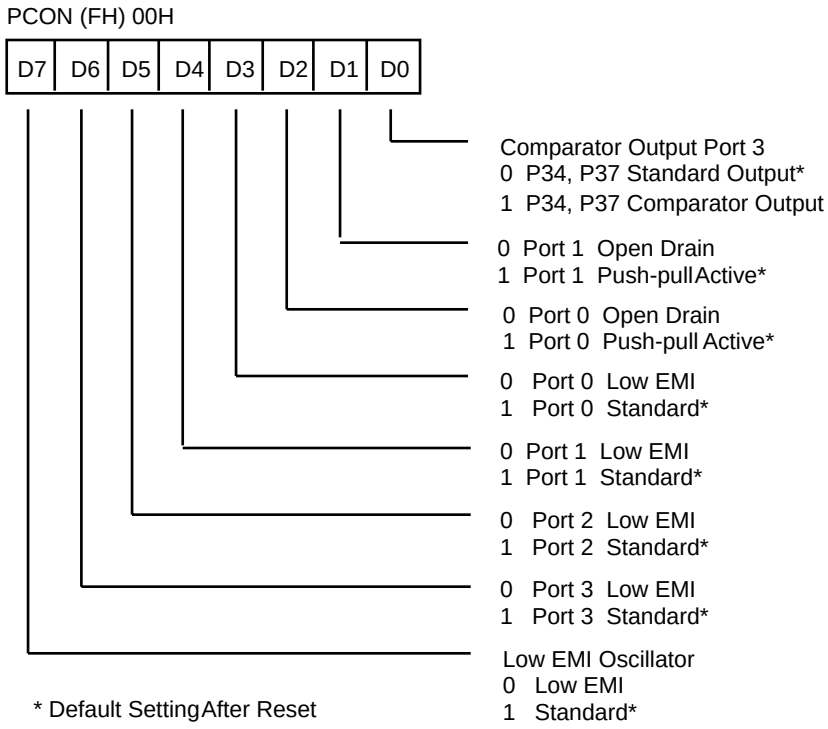


Figure 30. Port Configuration Register (PCON) (Write Only)

FUNCTIONAL DESCRIPTION (Continued)

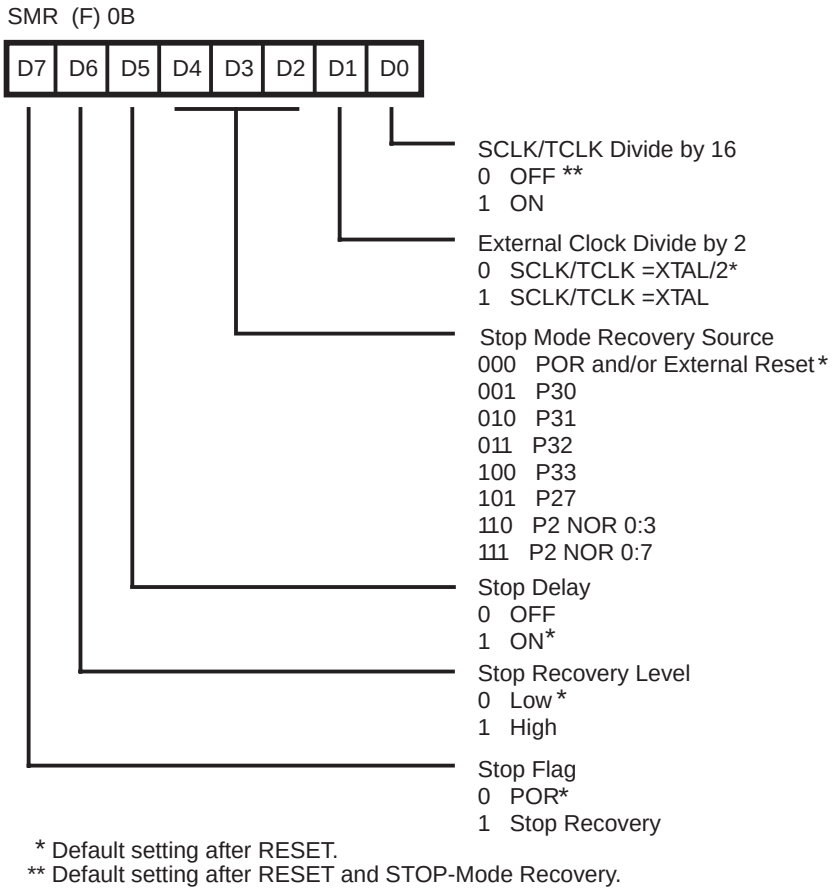


Figure 31. STOP-Mode Recovery Register (Write-Only Except Bit D7, Which is Read-Only)

EXPANDED REGISTER FILE CONTROL REGISTERS

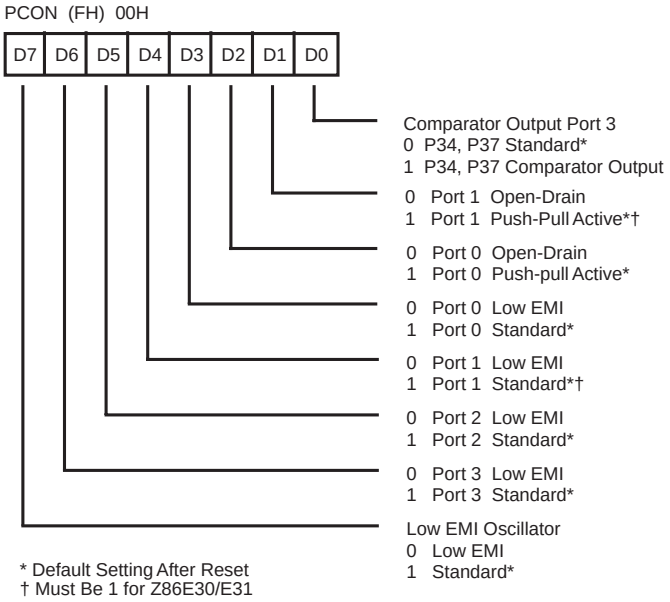


Figure 41. Port Configuration Register Write Only

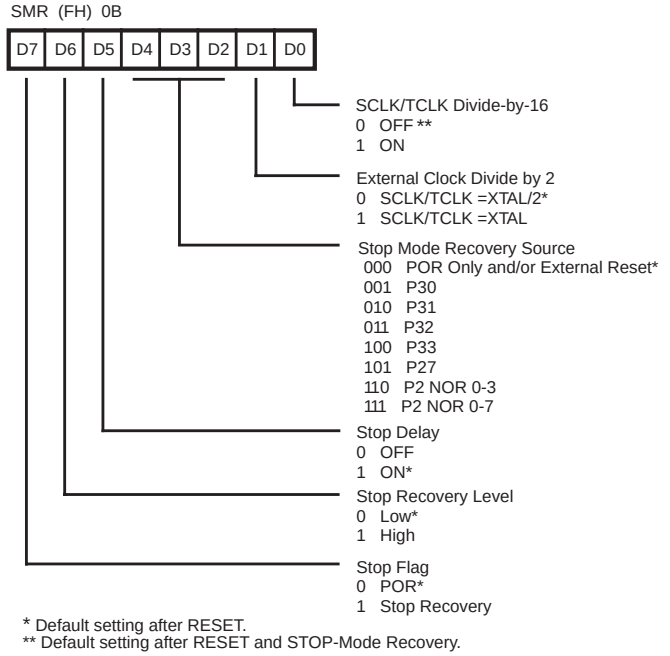


Figure 42. STOP-Mode Recovery Register Write Only Except Bit D7, Which is Read Only

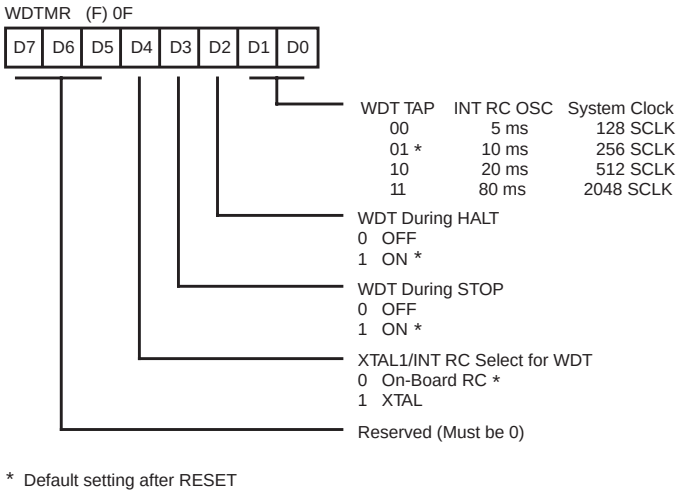


Figure 43. Watch-Dog Timer Mode Register Write Only

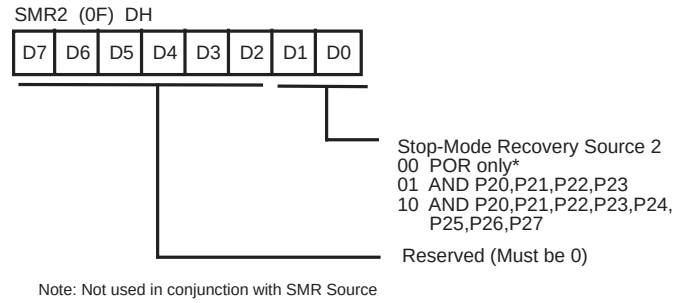


Figure 44. STOP-Mode Recovery Register 2 Write Only

Z8 CONTROL REGISTER DIAGRAMS

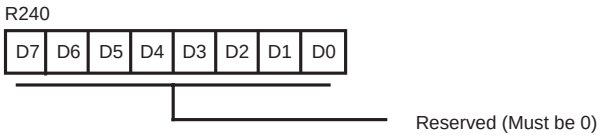


Figure 45. Reserved

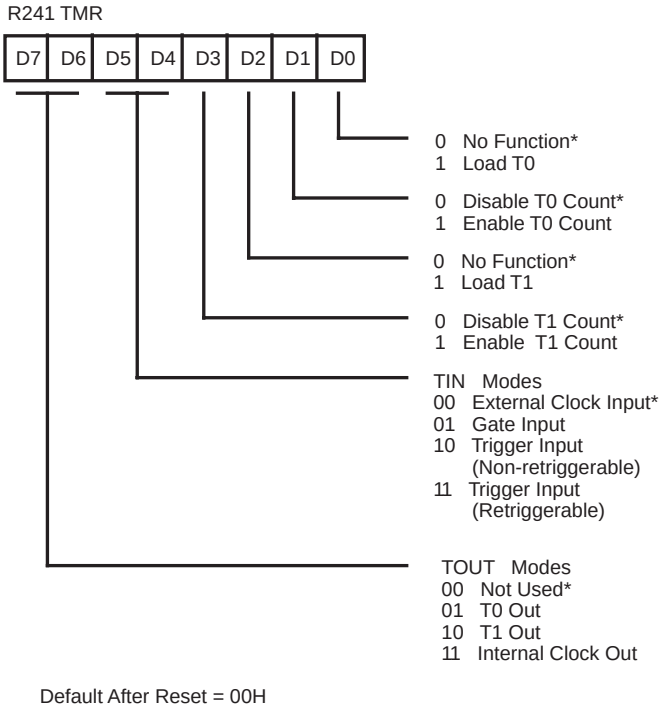


Figure 46. Timer Mode Register
F1H: Read/Write

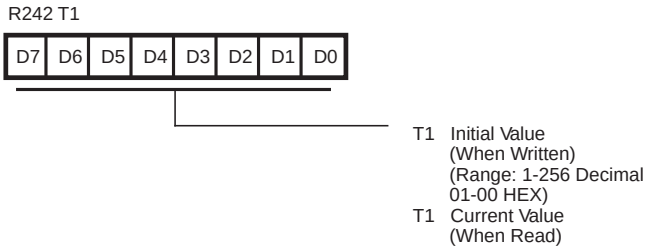


Figure 47. Counter/Timer 1 Register
F2H: Read/Write

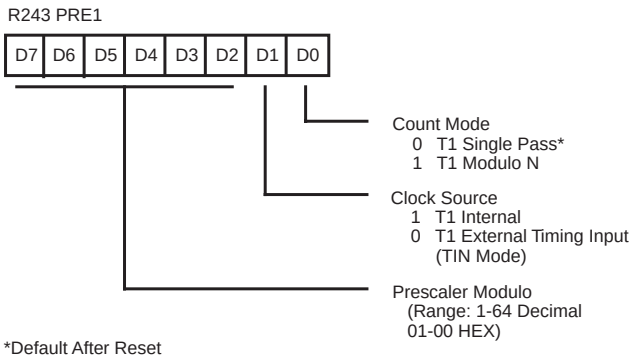


Figure 48. Prescaler 1 Register
F3H: Write Only

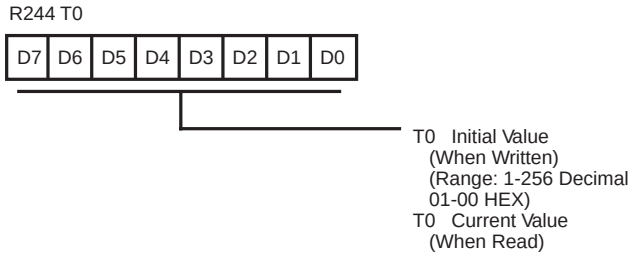


Figure 49. Counter/Timer 0 Register
F4H; Read/Write

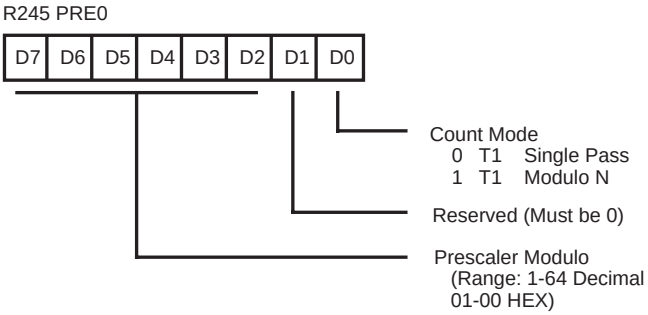


Figure 50. Prescaler 0 Register
F5H: Write Only

Z8 CONTROL REGISTER DIAGRAMS (Continued)

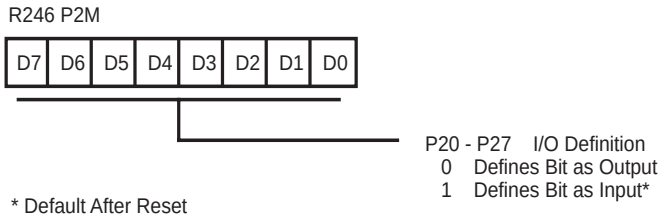


Figure 51. Port 2 Mode Register
F6H: Write Only

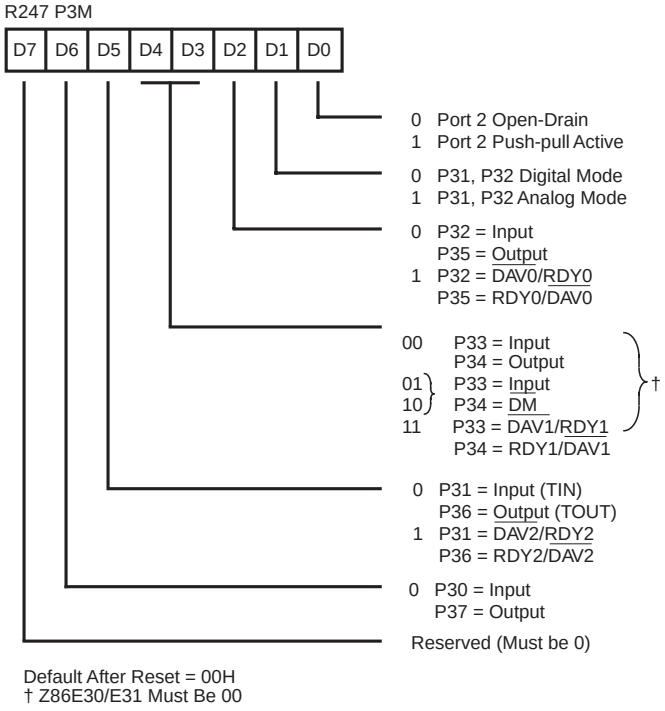


Figure 52. Port 3 Mode Register
F7H: Write Only

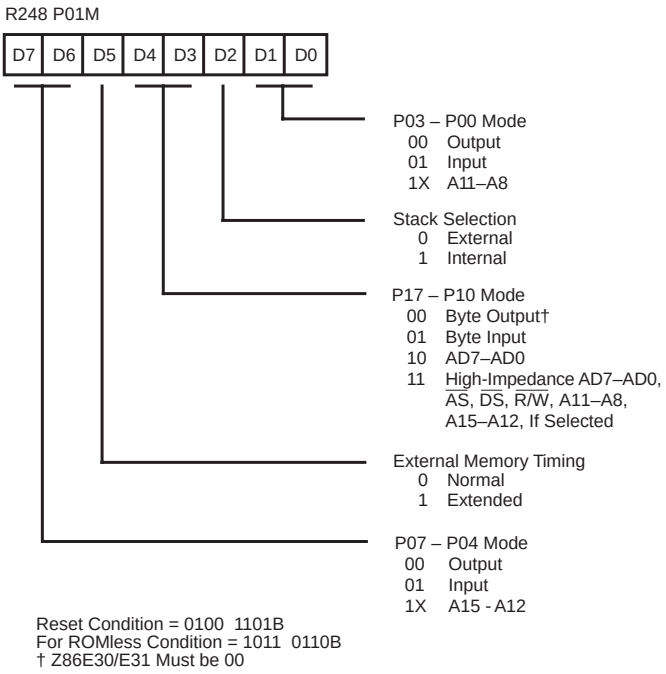


Figure 53. Port 0 and 1 Mode Register
F8H: Write Only
Z86E30/E31 Only

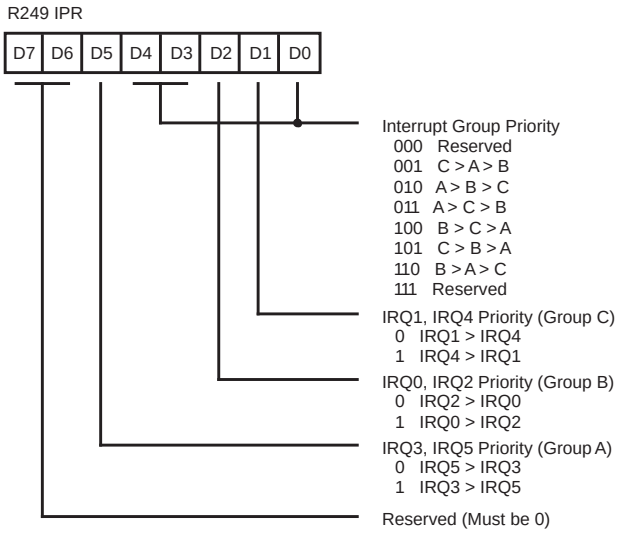
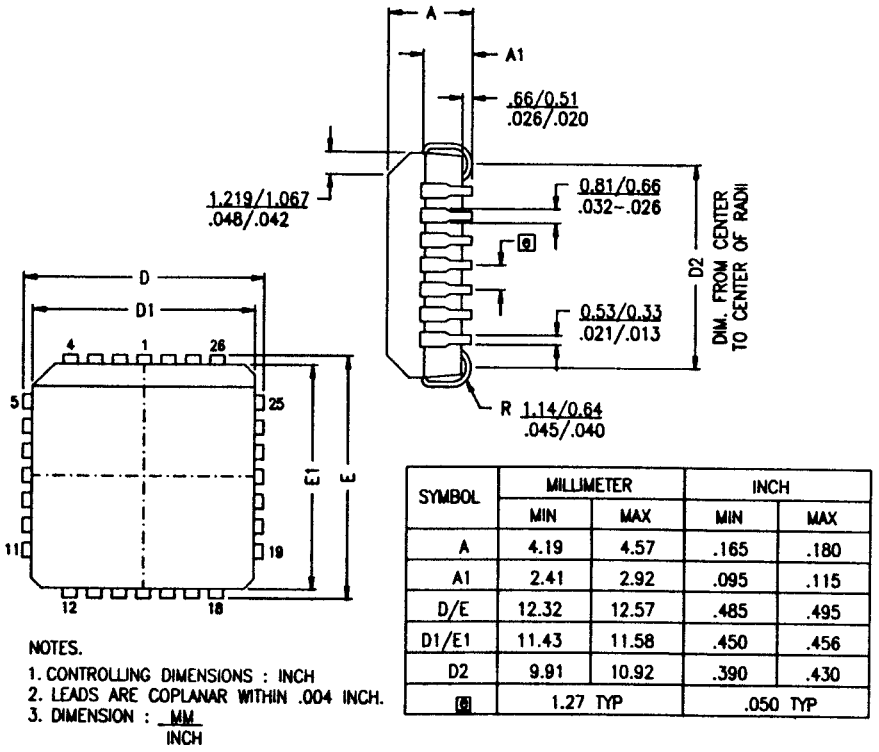


Figure 54. Interrupt Priority Register
F9H: Write Only



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.19	4.57	.165	.180
A1	2.41	2.92	.095	.115
D/E	12.32	12.57	.485	.495
D1/E1	11.43	11.58	.450	.456
D2	9.91	10.92	.390	.430
e	1.27 TYP		.050 TYP	

Figure 66. 28-Pin PLCC Package Diagram

ORDERING INFORMATION

Z86E40 (16 MHz)

40-Pin DIP	44-Pin PLCC	44-Pin LQFP
Z86E4016PSC	Z86E4016VSC	Z86E4016FSC
Z86E4016PEC	Z86E4016VEC	Z86E4016FEC

Z86E30 (16 MHz)

28-Pin DIP	28-Pin SOIC	28-Pin PLCC
Z86E3016PSC	Z86E3016SSC	Z86E3016VSC
Z96E3016PEC	Z86E3016SEC	Z86E3016VEC

Z86E31 (16 MHz)

28-Pin DIP	28-Pin SOIC	28-Pin PLCC
Z86E3116PSC	Z86E3116SSC	Z86E3116VSC
Z86E3116PEC	Z86E3116SEC	Z86E3116VEC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package

P = Plastic DIP

V = Plastic Leaded Chip Carrier

F = Plastic Quad Flat Pack

S = SOIC (Small Outline Integrated Circuit)

Temperature

S = 0 °C to +70 °C
E = -40 °C to +105 °C

Speed

16 = 16 MHz

Environmental

C= Plastic Standard

E = Hermetic Standard

Example:

Z 86E40 16 P S C is a Z86E40, 16 MHz, DIP, 0°C to +70°C, Plastic Standard Flow