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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	2KB (2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e3116pscr53lr

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

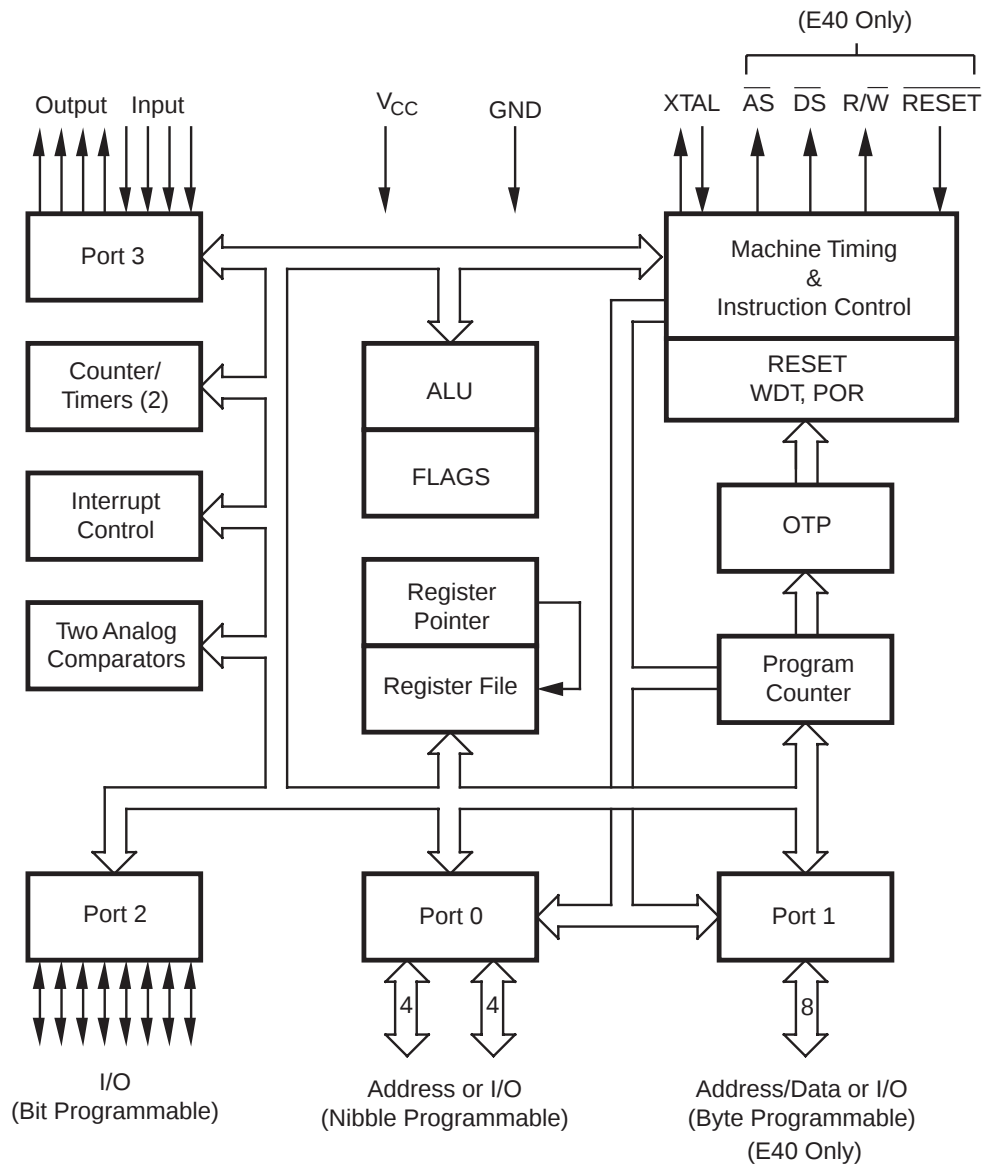


Figure 1. Z86E30/E31/E40 Functional Block Diagram

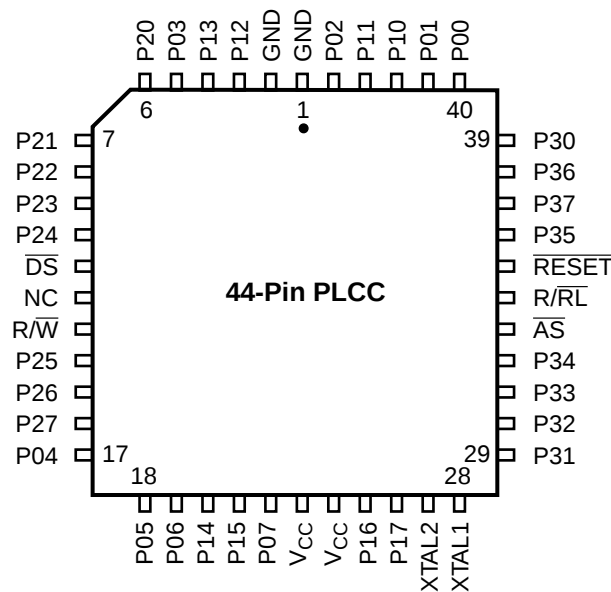


Figure 4. 44-Pin PLCC Pin Configuration
Standard Mode

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1–2	GND	Ground	
3–4	P12–P13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6–10	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output
11	DS	Data Strobe	Output
12	NC	No Connection	
13	R/W	Read/Write	Output
14–16	P25–P27	Port 2, Pins 5,6,7	In/Output
17–19	P04–P06	Port 0, Pins 4,5,6	In/Output
20–21	P14–P15	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23–24	VCC	Power Supply	
25–26	P16–P17	Port 1, Pins 6,7	In/Output
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29–31	P31–P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
33	AS	Address Strobe	Output
34	R/RL	ROM/ROMless select	Input
35	RESET	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40–41	P00–P01	Port 0, Pins 0,1	In/Output
42–43	P10–P11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

PIN IDENTIFICATION (Continued)

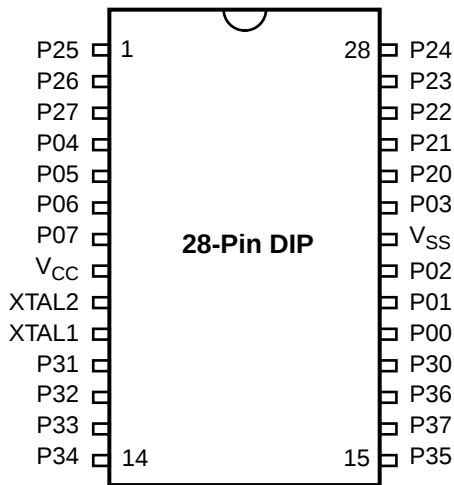


Figure 9. Standard Mode
28-Pin DIP/SOIC Pin Configuration

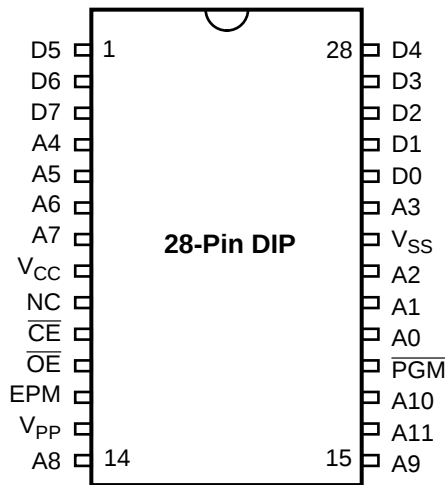


Figure 10. EPROM Programming Mode
28-Pin DIP/SOIC Pin Configuration

Table 7. 28-Pin DIP/SOIC/PLCC
Pin Identification*

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Pins 5,6,	In/Output
4–7	P04–P07	Port 0, Pins 4,5,6,7	In/Output
8	VCC	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11–13	P31–P33	Port 3, Pins 1,2,3	Input
14–15	P34–P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19–21	P00–P02	Port 0, Pins 0,1,2	In/Output
22	VSS	Ground	
23	P03	Port 0, Pin 3	In/Output
24–28	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output

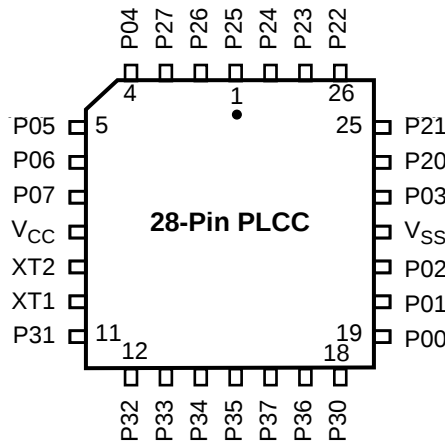
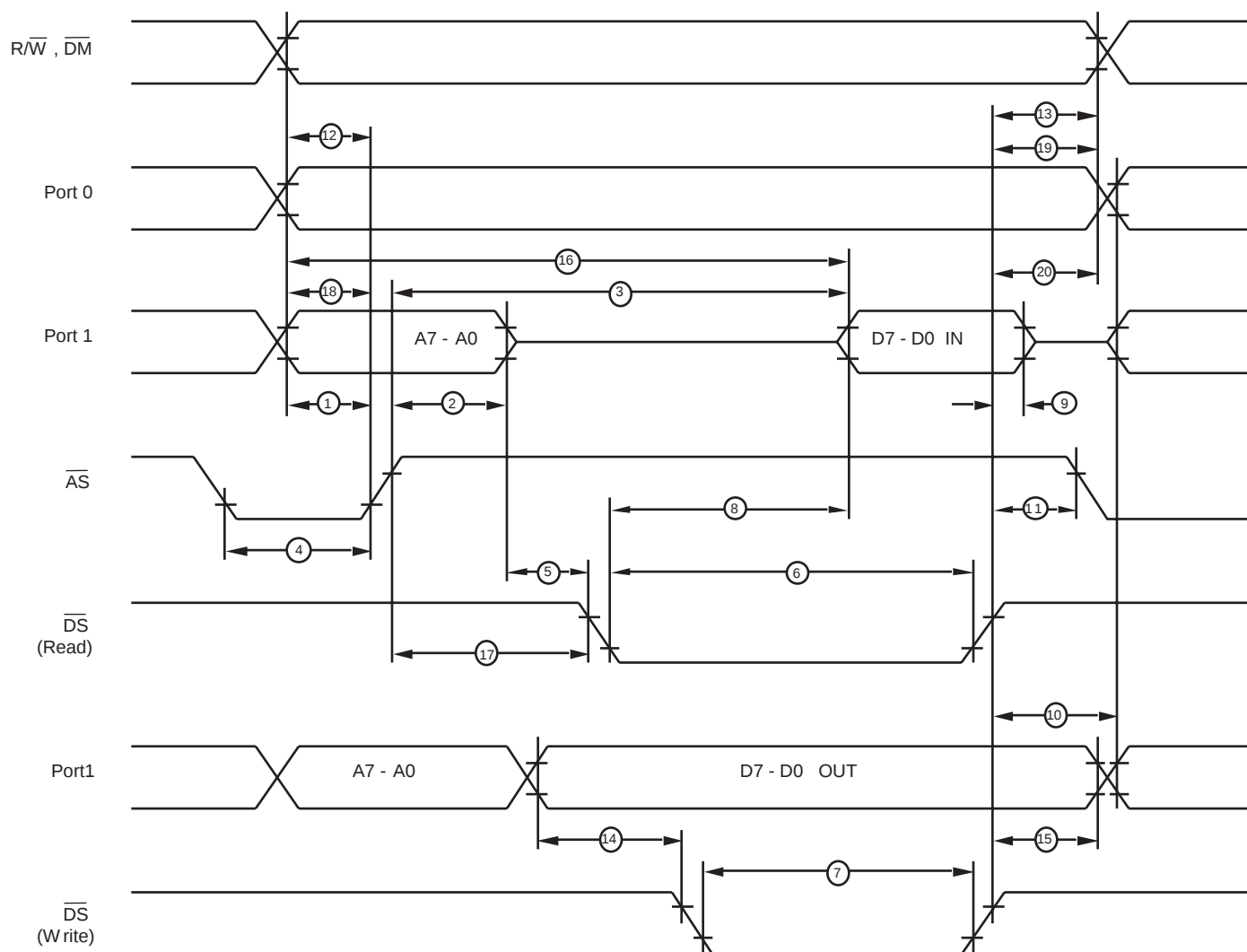


Figure 11. Standard Mode
28-Pin PLCC Pin Configuration



**Figure 14. External I/O or Memory Read/Write Timing
Z86E40 Only**

Additional Timing Table (Divide-By-One Mode)

				$T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$		$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$			
				4 MHz		4 MHz			
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.5V 5.5V	250 250	DC DC	250 250	DC DC	ns ns	1,7,8 1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V 5.5V		25 25		25 25	ns ns	1,7,8 1,7,8
3	TwC	Input Clock Width	3.5V 5.5V	100 100		100 100		ns ns	1,7,8 1,7,8
4	TwTinL	Timer Input Low Width	3.5V 5.5V	100 70		100 70		ns ns	1,7,8 1,7,8
5	TwTinH	Timer Input High Width	3.5V 5.5V	5TpC 5TpC		5TpC 5TpC			1,7,8 1,7,8
6	TpTin	Timer Input Period	3.5V 5.5V	8TpC 8TpC		8TpC 8TpC			1,7,8 1,7,8
7	TrTin, Tftin	Timer Input Rise & Fall Timer	3.5V 5.5V		100 100		100 100	ns ns	1,7,8 1,7,8
8A	TwIL	Int. Request Low Time	3.5V 5.5V	100 70		100 70		ns ns	1,2,7,8 1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V 5.5V	5TpC 5TpC		5TpC 5TpC			1,3,7,8 1,3,7,8
9	TwIH	Int. Request Input High Time	3.5V 5.5V	5TpC 5TpC		5TpC 5TpC			1,2,7,8 1,2,7,8
10	Twsm	STOP Mode Recovery Width Spec	3.5V 5.5V	12 12		12 12		ns ns	4,8 4,8
11	Tost	Oscillator Startup Time	3.5V 5.5V		5TpC 5TpC		5TpC		4,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31–P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 1, POR STOP Mode Delay is on.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 5.5V guarantees 5.0V $\pm$ 0.5V and the V_{CC} voltage specification of 3.5V guarantees 3.5V only.
7. SMR D1 = 0.
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

Port 2 (P27–P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can

be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control.

In Handshake Mode, Port 3 lines P31 and P36 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2 (Figure 20).

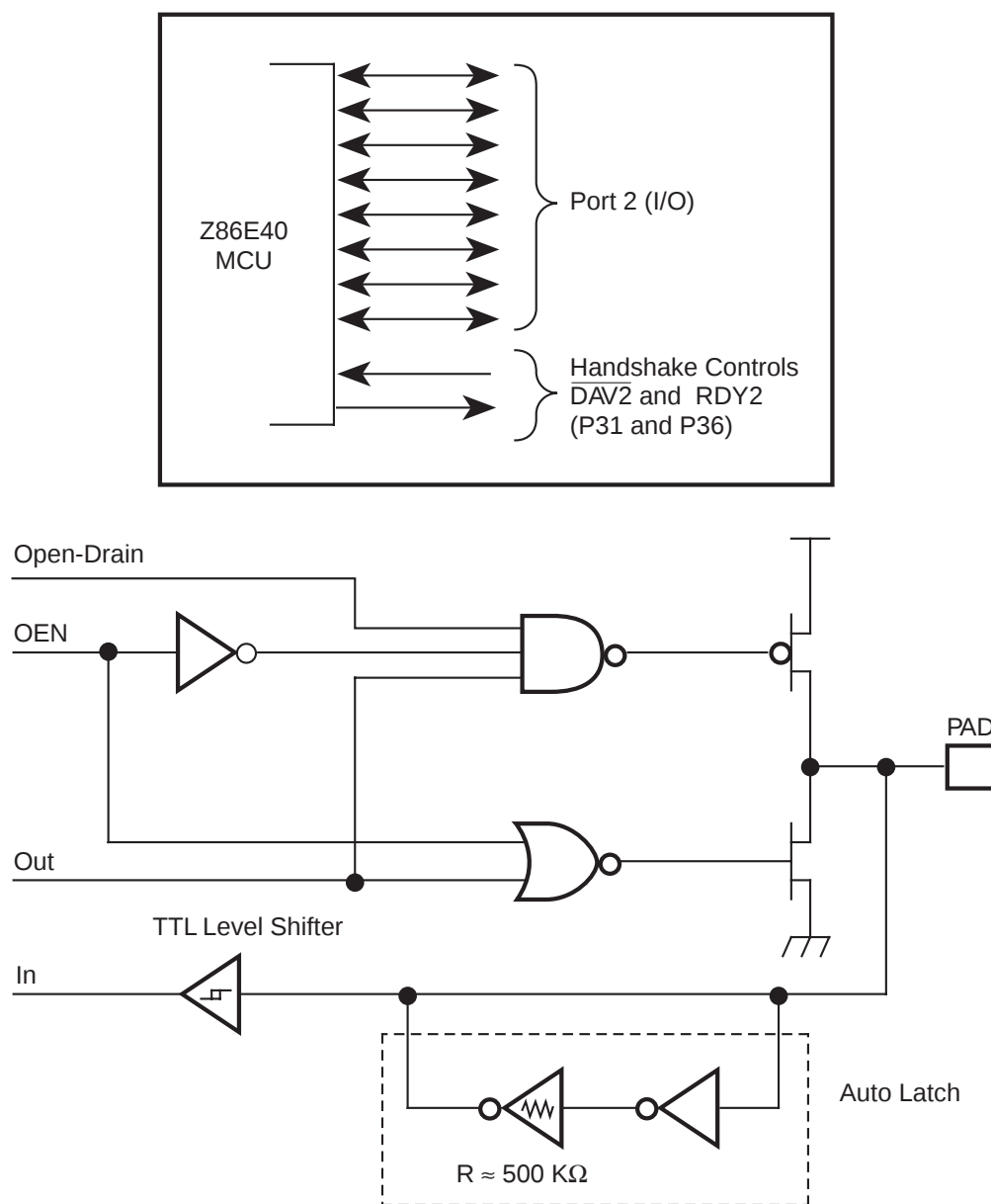


Figure 20. Port 2 Configuration

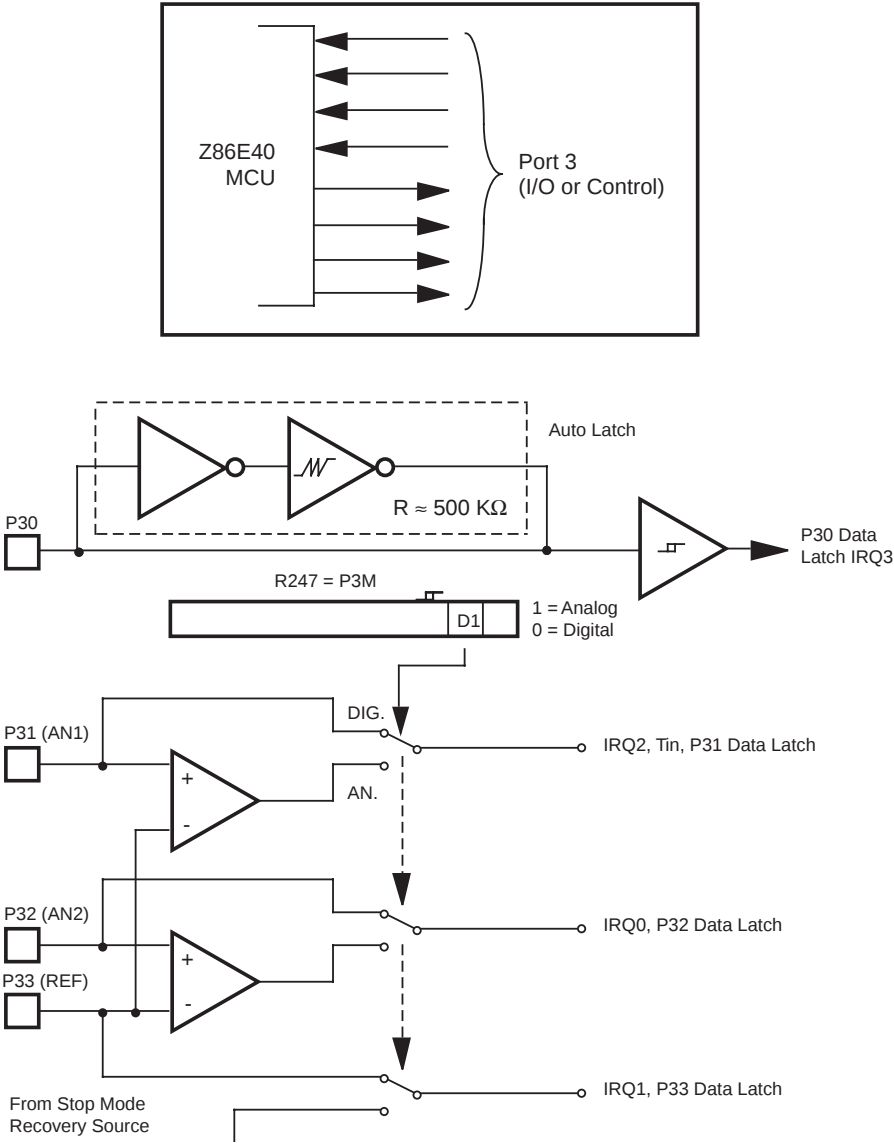


Figure 21. Port 3 Configuration

Table 9. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Interrupt	P0 HS	P1 HS	P2 HS	Ext
P30	IN			IRQ3				
P31	IN	T _{IN}	AN1	IRQ2		D/R		
P32	IN		AN2	IRQ0	D/R			
P33	IN		REF	IRQ1		D/R		
P34	OUT		AN1-Out			R/D		/DM
P35	OUT				R/D			
P36	OUT	T _{OUT}				R/D		
P37	OUT		An2-Out					

FUNCTIONAL DESCRIPTION

The MCU incorporates the following special functions to enhance the standard Z8 architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of three ways:

- 1. Power-On Reset
- 2. Watch-Dog Timer
- 3. STOP-Mode Recovery Source

Note: Having the Auto Power-On Reset circuitry built-in, the MCU does not need to be connected to an external power-on reset circuit. The reset time is 5 ms (typical). The MCU does not reinitialize WDTMR, SMR, P2M, and P3M registers to their reset values on a STOP-Mode Recovery operation.

Note: The device V_{CC} must rise up to the operating V_{CC} specification before the TPOR expires.

Program Memory. The MCU can address up to 4 KB of Internal Program Memory (Figure 22). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 12 (000CH) to address 4095 (0FFFH) consists of program-mable EPROM. After reset, the program counter points at the address 000CH, which is the starting address of the user program.

In ROMless mode, the Z86E40 can address up to 64 KB of External Program Memory. The ROM/ROMless option is only available on the 44-pin devices.

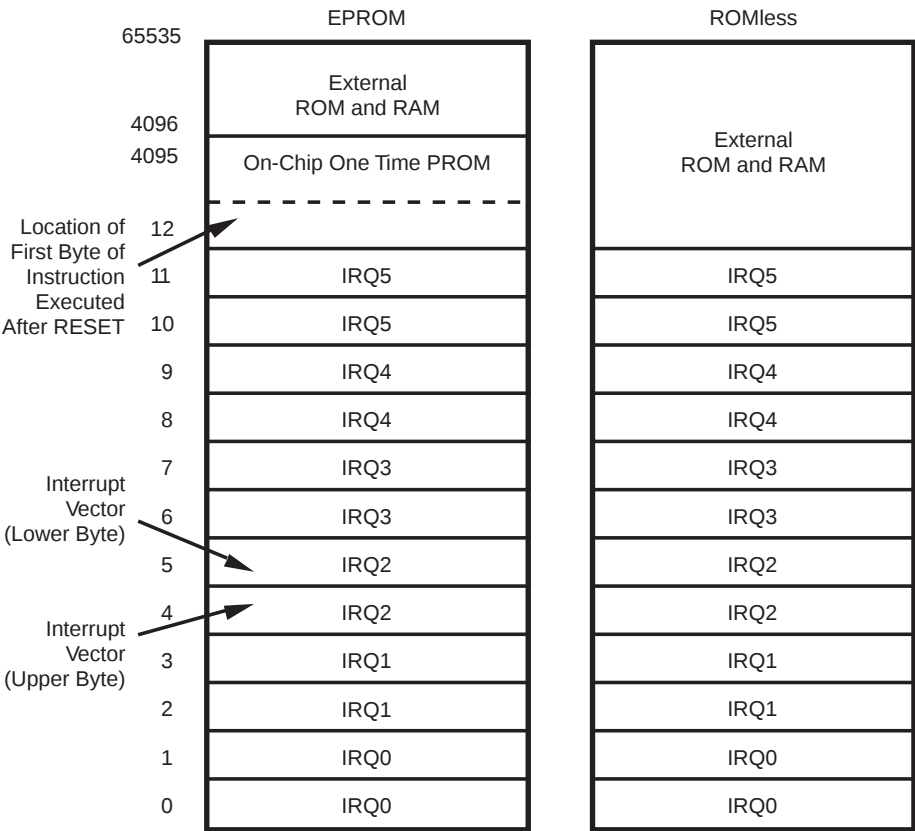


Figure 22. Program Memory Map (ROMless Z86E40 Only)

EPROM Protect. When in ROM Protect Mode, and executing out of External Program Memory, instructions LDC, LDCI, LDE, and LDEI cannot read Internal Program Memory.

When in ROM Protect Mode and executing out of Internal Program Memory, instructions LDC, LDCI, LDE, and LDEI can read Internal Program Memory.

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The MCU has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 28). The six sources are divided as follows: four sources are claimed by Port 3 lines P33–P30) and two

in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 10).

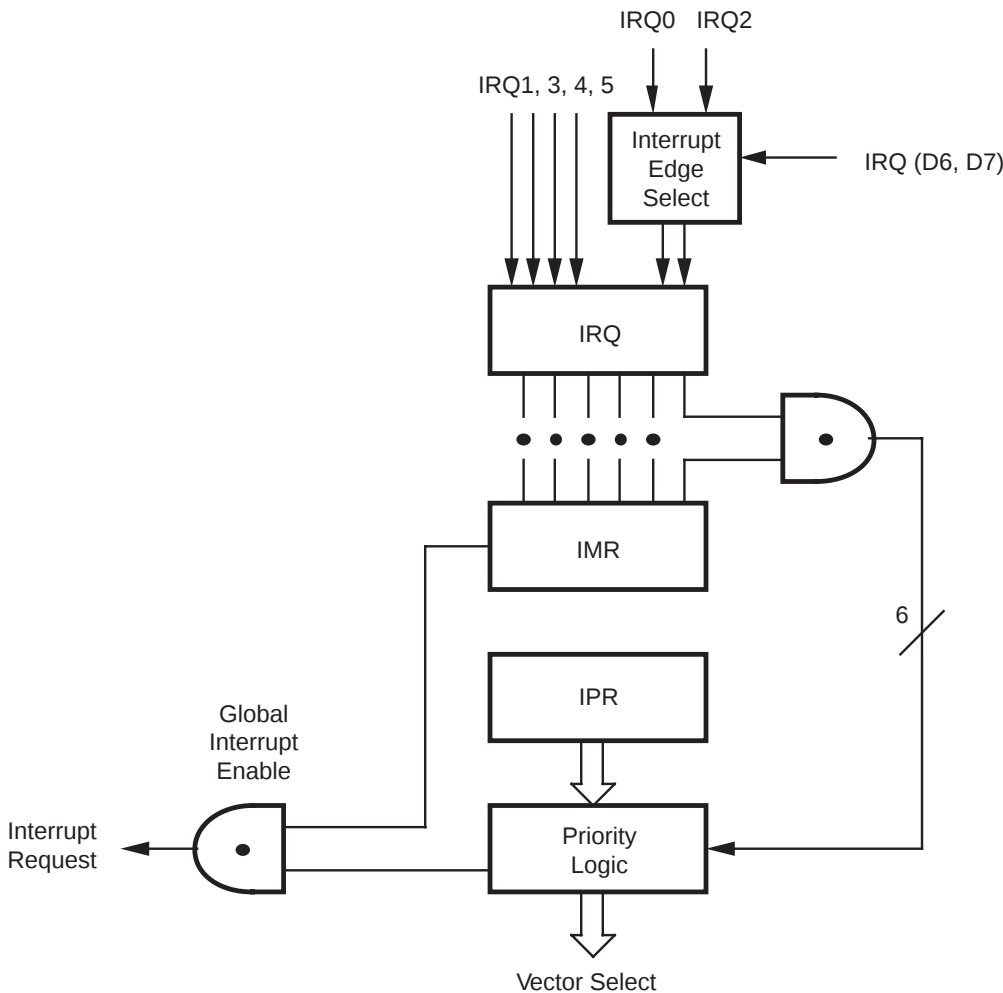


Figure 28. Interrupt Block Diagram

Table 10. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	DAV0, IRQ0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	DAV2, IRQ2, T _{IN}	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Falling Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register (IPR). An interrupt machine cycle is activated when an interrupt request is granted. Thus, disabling all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in bits D7 and D6 of the IRQ Register (R250). The configuration is shown in Table 11.

Table 11. IRQ Register Configuration

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 KHz to 16 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to device pin Ground. The RC oscillator option can be selected in the programming mode. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Figure 29).

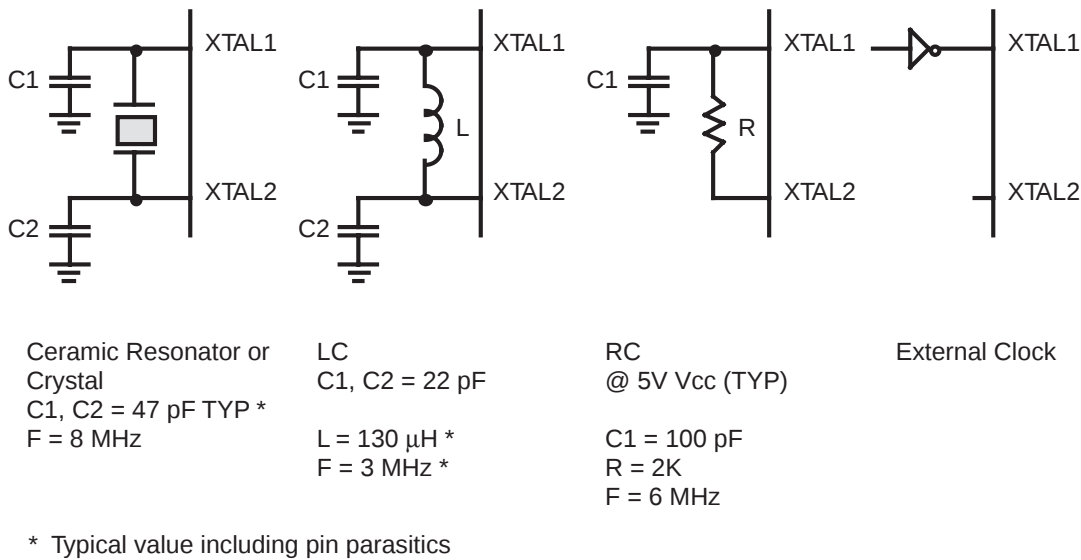


Figure 29. Oscillator Configuration

Comparator Output Port 3 (D0). Bit 0 controls the comparator output in Port 3. A “1” in this location brings the comparator outputs to P34 and P37, and a “0” releases the Port to its standard I/O configuration. The default value is 0.

Port 1 Open-Drain (D1). Port 1 can be configured as an open-drain by resetting this bit (D1=0) or configured as push-pull active by setting this bit (D1=1). The default value is 1.

Port 0 Open-Drain (D2). Port 0 can be configured as an open-drain by resetting this bit (D2=0) or configured as push-pull active by setting this bit (D2=1). The default value is 1.

Low EMI Port 0 (D3). Port 0 can be configured as a Low EMI Port by resetting this bit (D3=0) or configured as a Standard Port by setting this bit (D3=1). The default value is 1.

Low EMI Port 1 (D4). Port 1 can be configured as a Low EMI Port by resetting this bit (D4=0) or configured as a Standard Port by setting this bit (D4=1). The default value is 1. **Note:** The emulator does not support Port 1 low EMI mode and must be set D4 = 1.

Low EMI Port 2 (D5). Port 2 can be configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting this bit (D5=1). The default value is 1.

Low EMI Port 3 (D6). Port 3 can be configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting this bit (D6=1). The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A “1” in this location configures the oscillator with standard drive. While a “0” configures the oscillator with low noise drive, however, it does not affect the relationship of SCLK and XTAL. The low EMI mode will reduce the drive of the oscillator (OSC). The default value is 1. **Note:** 4 MHz is the maximum external clock frequency when running in the low EMI oscillator mode.

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 31). All bits are Write Only except bit 7 which is a Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power-on cycle. Bit 6 controls whether a low or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the Stop-Mode Recovery Source. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

FUNCTIONAL DESCRIPTION (Continued)

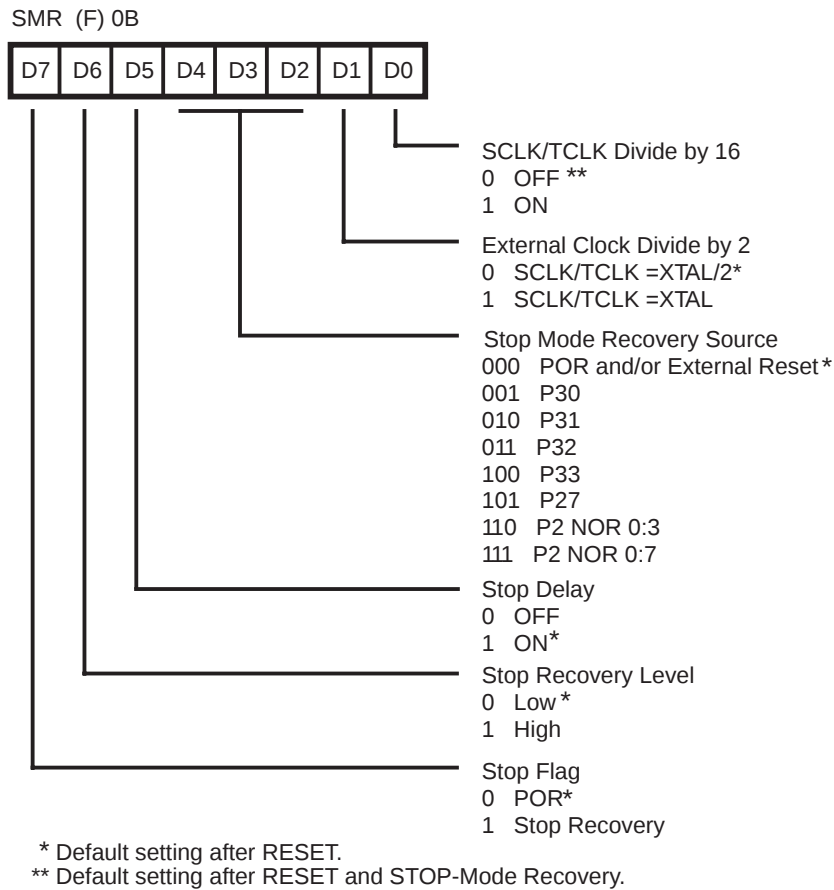


Figure 31. STOP-Mode Recovery Register
(Write-Only Except Bit D7, Which is Read-Only)

Table 14. EPROM Programming Table

Programming Modes	V _{PP}	EPM	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	ADDR	DATA	V _{CC} *
EPROM READ1	X	V _H	V _{IL}	V _{IL}	V _{IH}	ADDR	Out	4.5V†
EPROM READ2	X	V _H	V _{IL}	V _{IL}	V _{IH}	ADDR	Out	5.5V†
PROGRAM	V _H	V _H	V _{IL}	V _{IH}	V _{IL}	ADDR	In	6.4V
PROGRAM VERIFY	V _H	V _H	V _{IL}	V _{IL}	V _{IH}	ADDR	Out	6.0V
OPTION BIT PGM	V _H	V _H	V _{IL}	V _{IH}	V _{IL}	63	IN	6.4V
OPTION BIT READ	X	V _H	V _{IL}	V _{IL}	V _{IH}	63	OUT	6.0V

Notes:V_H = 13.0 V ± 0.1 VV_{IH} = As per specific Z8 DC specificationV_{IL} = As per specific Z8 DC specificationX=Not used, but must be set to V_H, V_{IH}, or V_{IL} level.NU = Not used, but must be set to either V_{IH} or V_{IL} level.I_{PP} during programming = 40 mA maximum.I_{CC} during programming, verify, or read = 40 mA maximum.*V_{CC} has a tolerance of ±0.25V.

† Zilog recommends an EPROM read at V_{CC} = 4.5 V and 5.5 V to ensure proper device operations during the V_{CC} after programming, but V_{CC} = 5.0 V is acceptable.

Table 15. EPROM Programming Timing

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		μs
2	Data Setup Time	2		μs
3	V _{PP} Setup	2		μs
4	V _{CC} Setup Time	2		μs
5	Chip Enable Setup Time	2		μs
6	Program Pulse Width	0.95	1.05	ms
7	Data Hold Time	2		μs
8	$\overline{OE}$ Setup Time	2		μs
9	Data Access Time	200		ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width/Option Program Pulse Width	2.85		ms
12	EPM Setup Time	2		μs
13	$\overline{PGM}$ Setup Time	2		μs
14	Address to $\overline{OE}$ Setup Time	2		μs
15	$\overline{OE}$ Width	250		ns
16	Address to $\overline{OE}$ Low	125		ns

FUNCTIONAL DESCRIPTION (Continued)

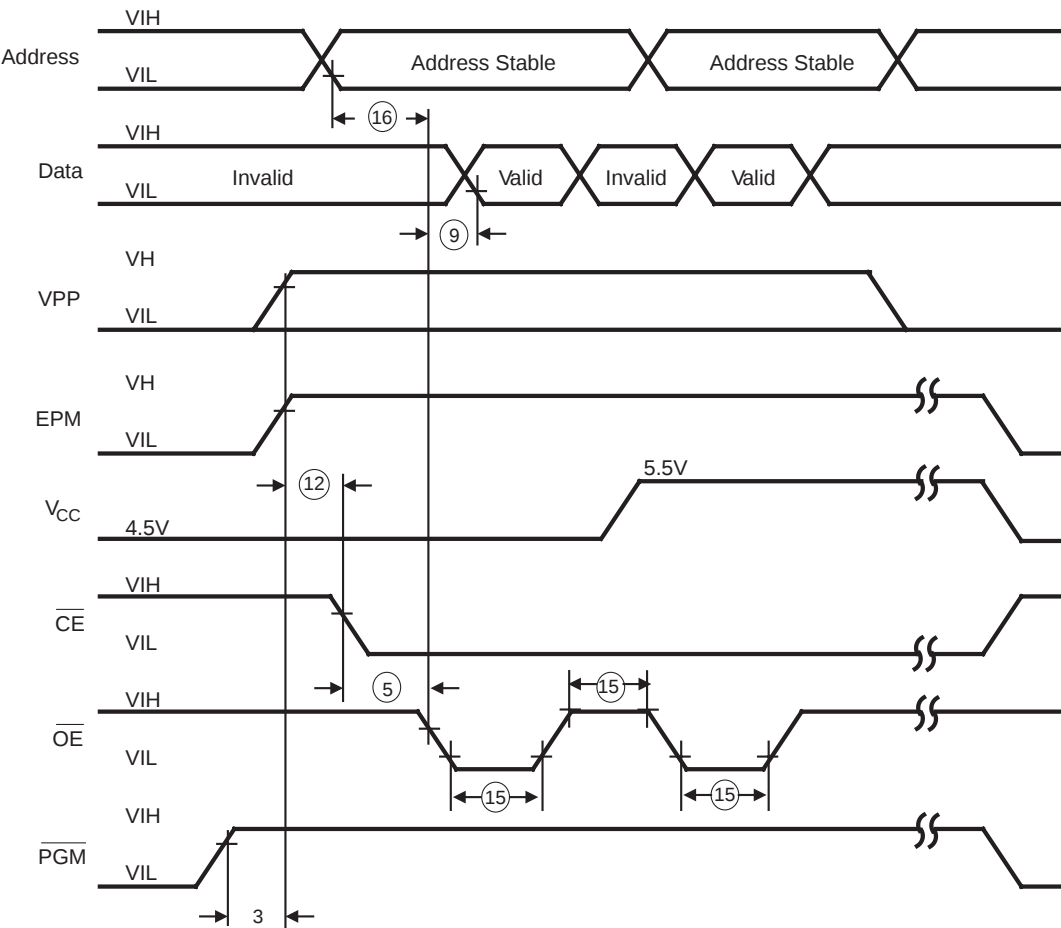


Figure 36. EPROM Read Mode Timing Diagram

Z86E40 TIMING DIAGRAMS

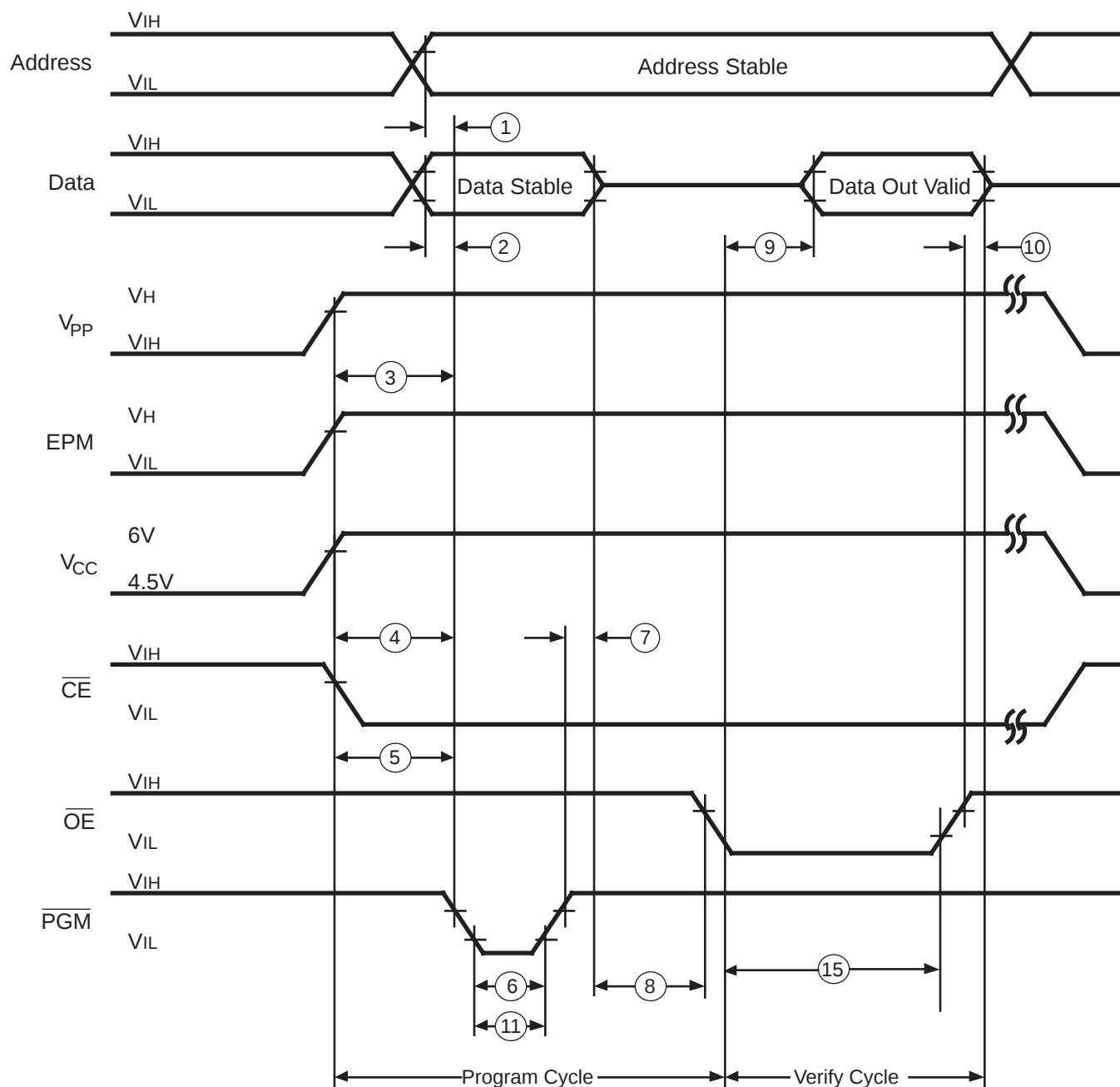


Figure 37. Timing Diagram of EPROM Program and Verify Modes

DS97Z8X0502

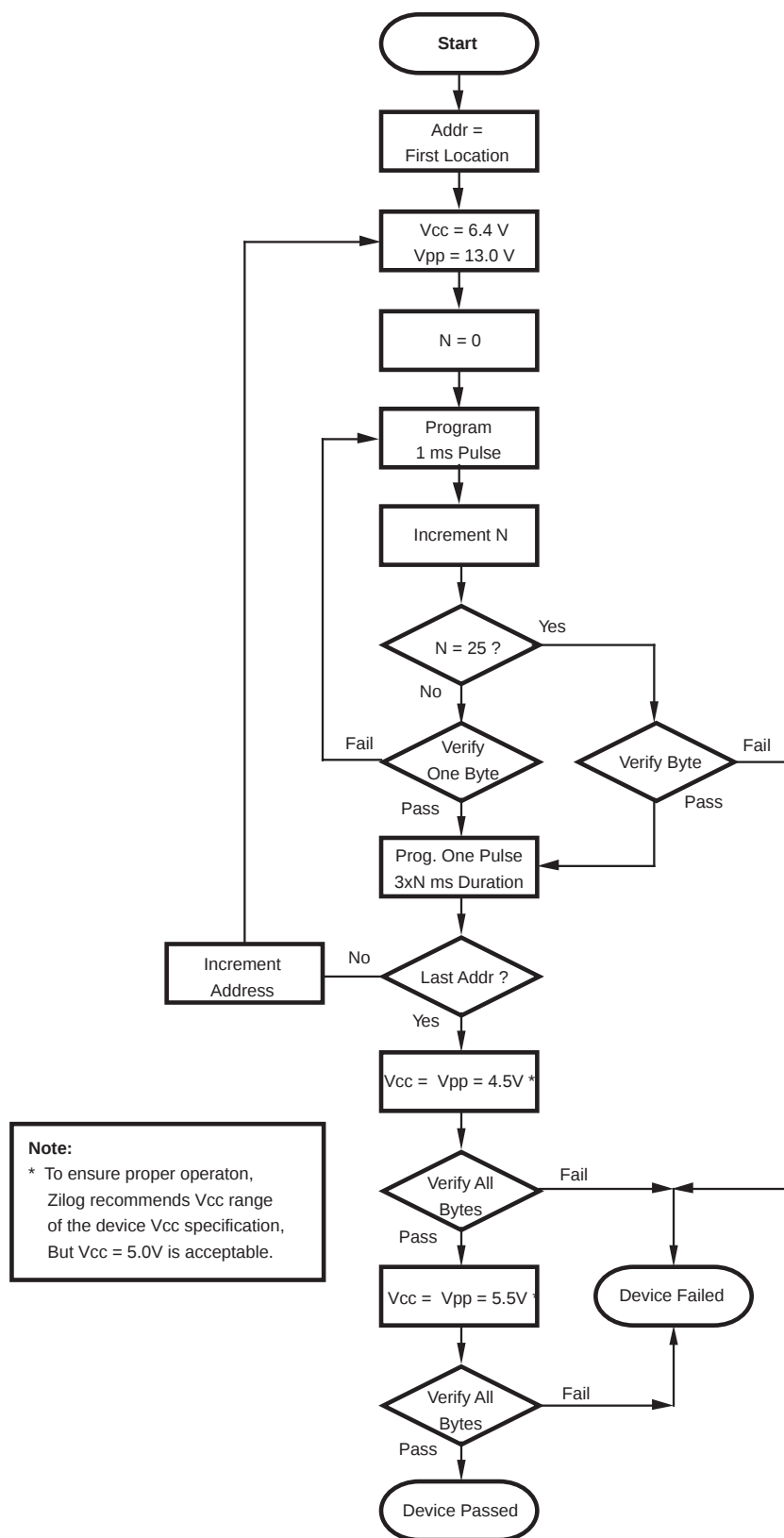


Figure 40. Z86E40 Programming Algorithm

Z8 CONTROL REGISTER DIAGRAMS

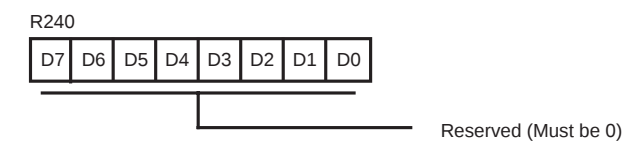
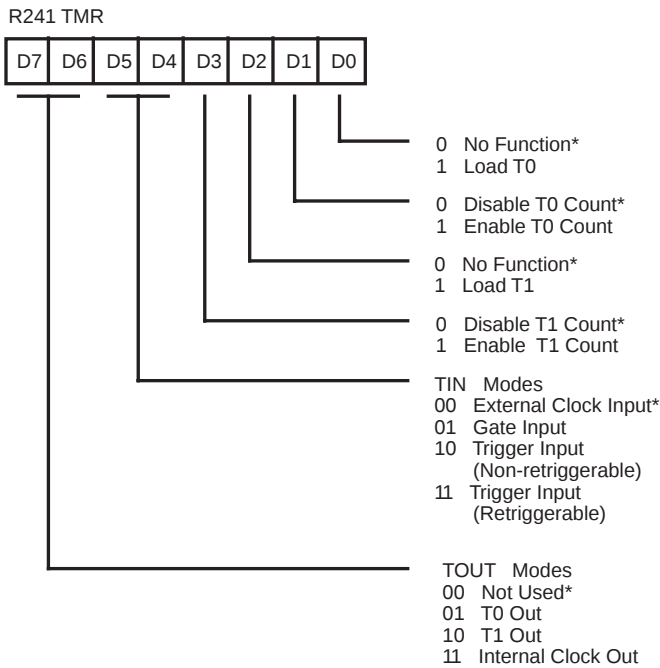


Figure 45. Reserved



Default After Reset = 00H

Figure 46. Timer Mode Register
F1H: Read/Write

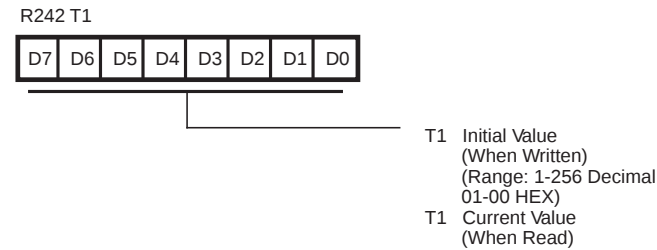


Figure 47. Counter/Timer 1 Register
F2H: Read/Write

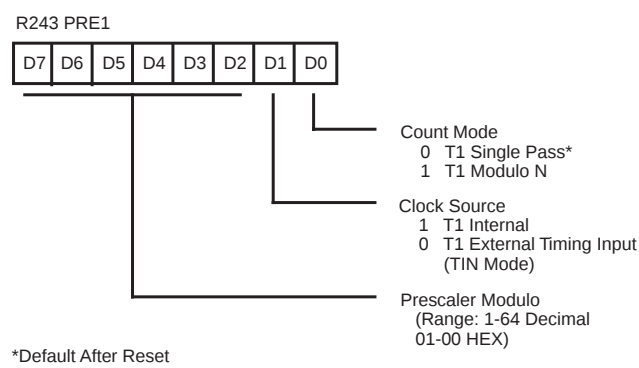


Figure 48. Prescaler 1 Register
F3H: Write Only

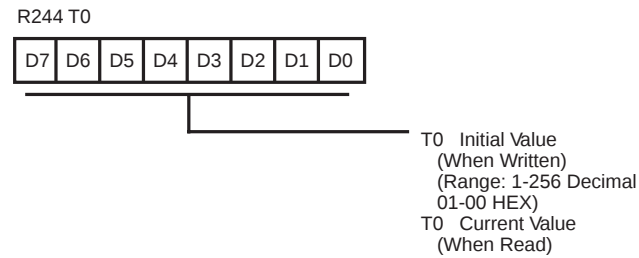


Figure 49. Counter/Timer 0 Register
F4H: Read/Write

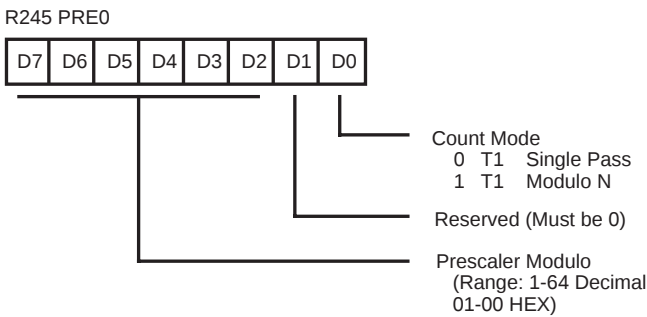


Figure 50. Prescaler 0 Register
F5H: Write Only

Z8 CONTROL REGISTER DIAGRAMS (Continued)

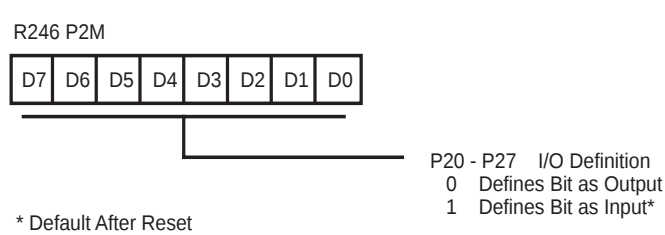


Figure 51. Port 2 Mode Register
F6H: Write Only

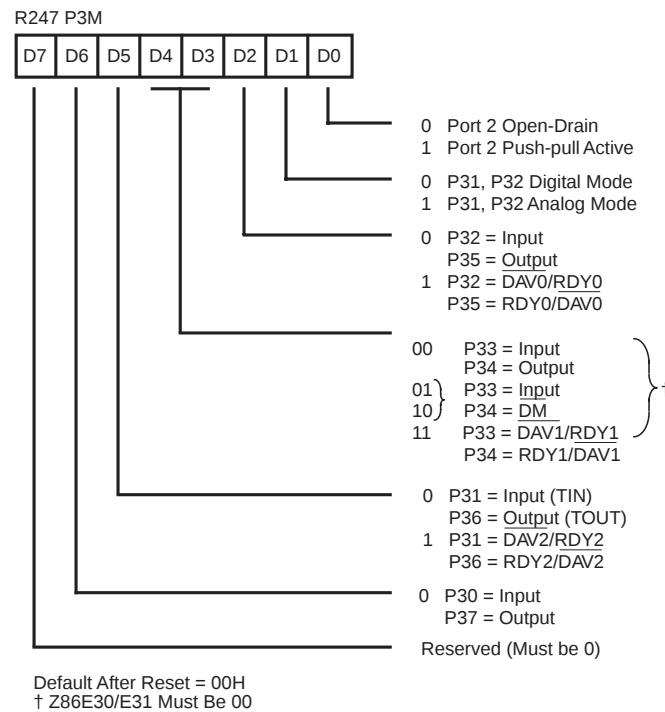


Figure 52. Port 3 Mode Register
F7H: Write Only

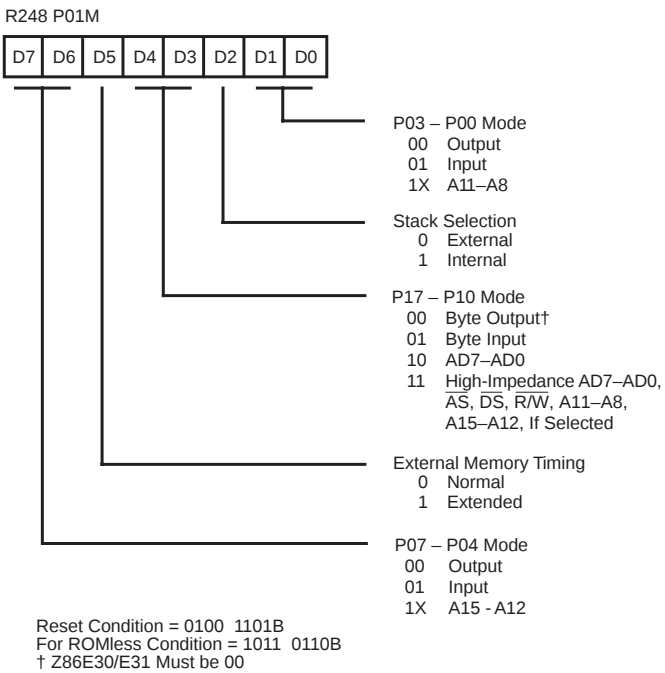


Figure 53. Port 0 and 1 Mode Register
F8H: Write Only
Z86E30/E31 Only

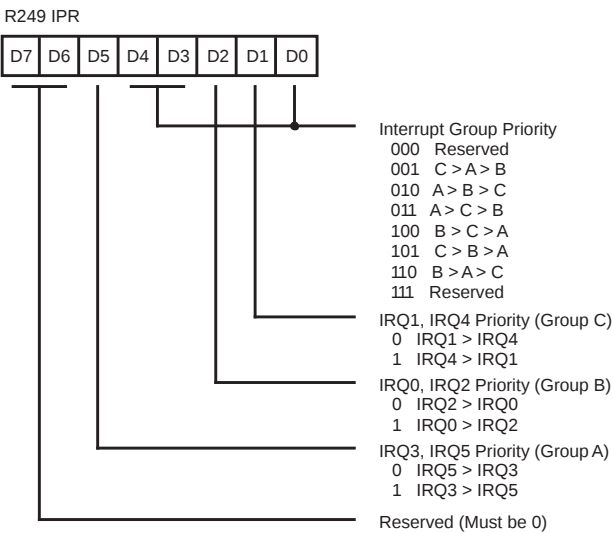


Figure 54. Interrupt Priority Register
F9H: Write Only

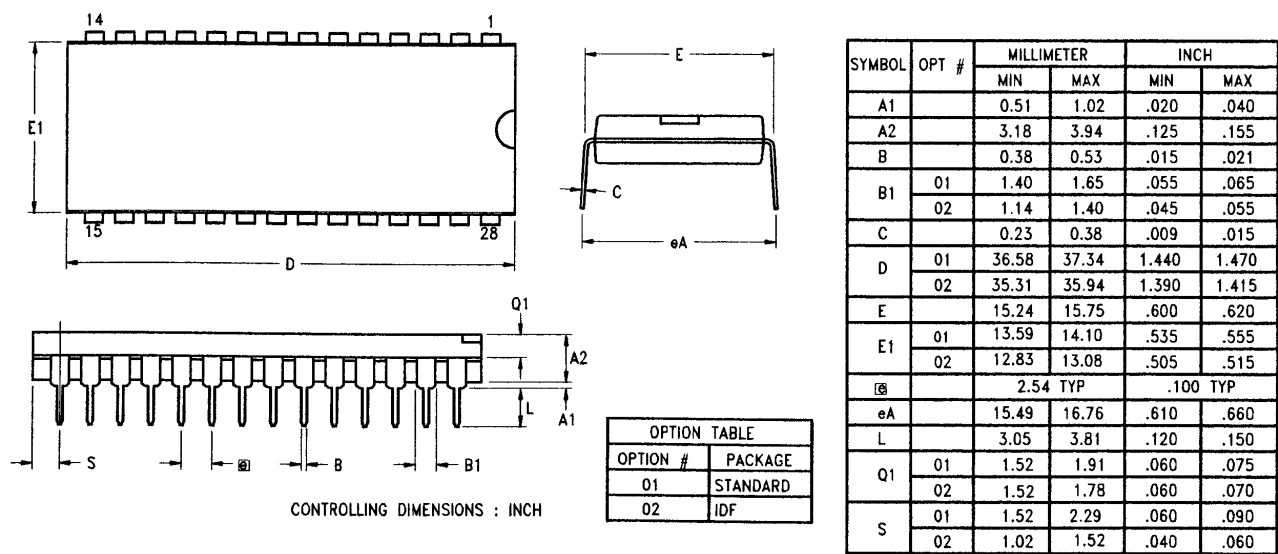


Figure 64. 28-Pin DIP Package Diagram

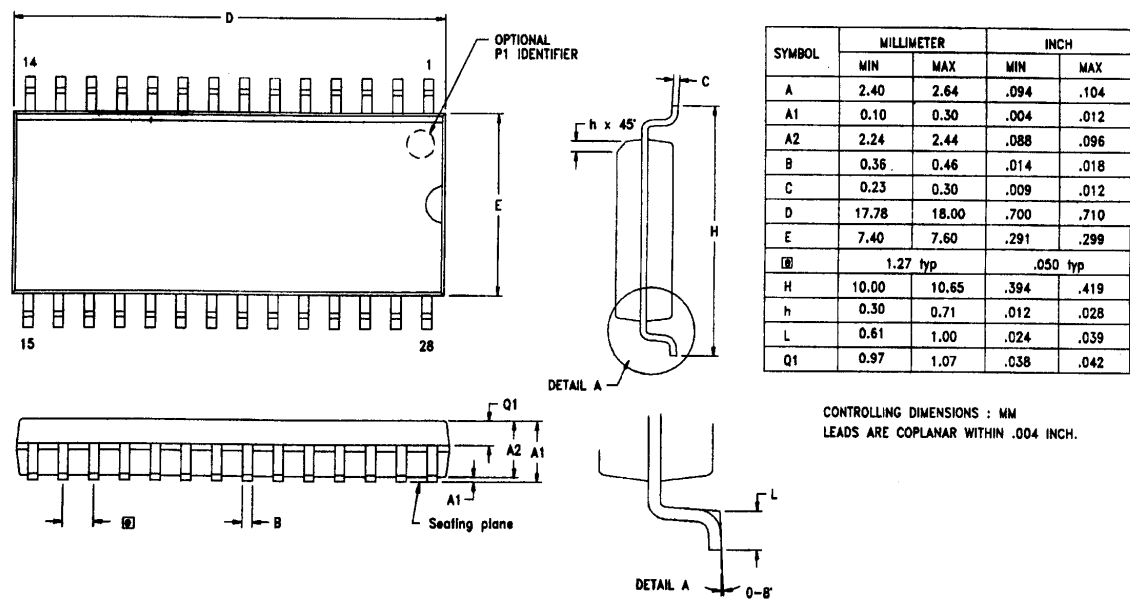


Figure 65. 28-Pin SOIC Package Diagram