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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	2KB (2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e3116ssc00tr

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

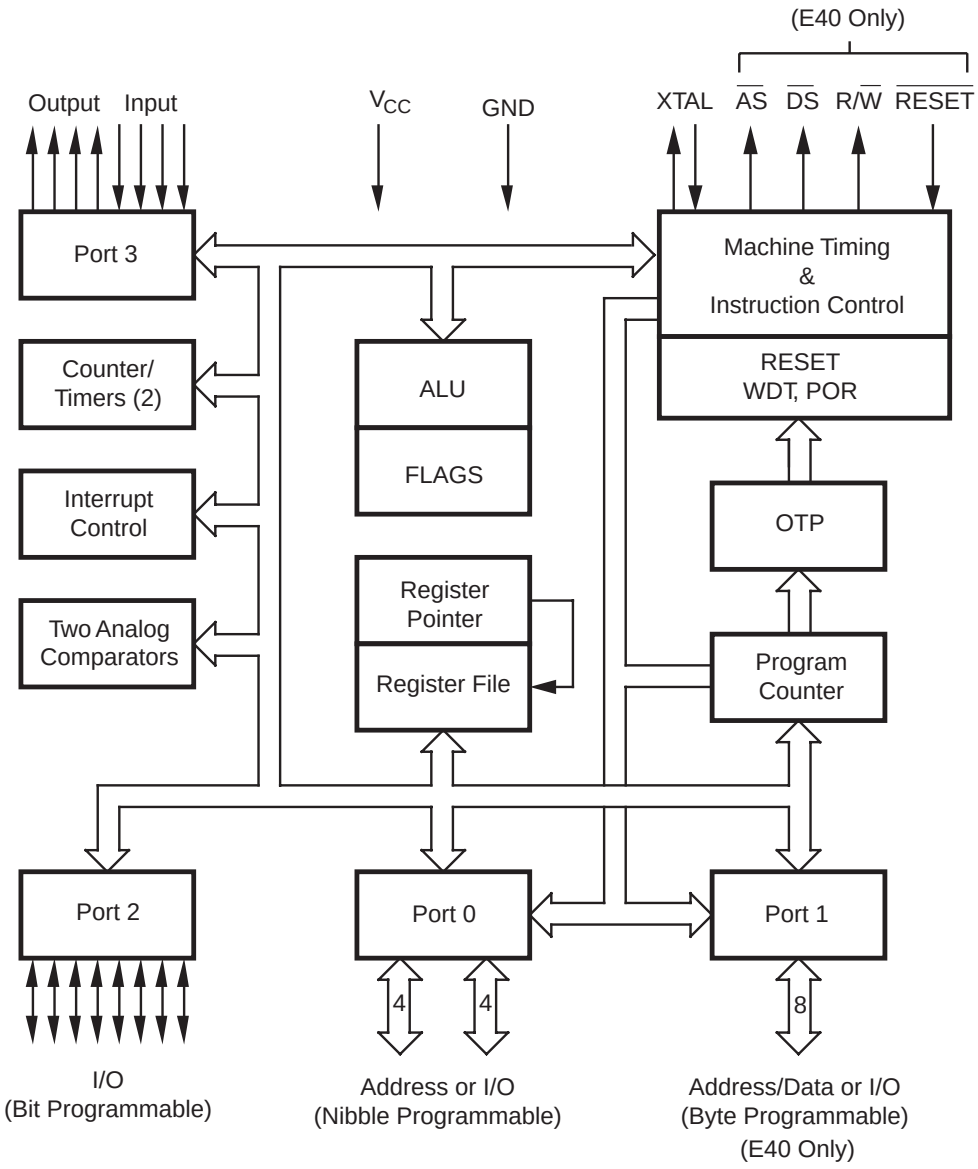


Figure 1. Z86E30/E31/E40 Functional Block Diagram

PIN IDENTIFICATION

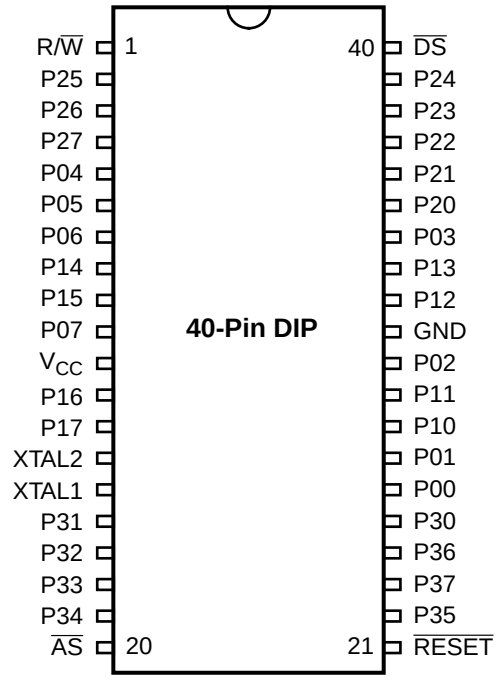


Figure 3. 40-Pin DIP Pin Configuration Standard Mode

Table 1. 40-Pin DIP Pin Identification Standard Mode

Pin #	Symbol	Function	Direction
1	R/$\overline{W}$	Read/Write	Output
2–4	P25–P27	Port 2, Pins 5,6,7	In/Output
5–7	P04–P06	Port 0, Pins 4,5,6	In/Output
8–9	P14–P15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V_{CC}	Power Supply	
12–13	P16–P17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal Oscillator	Output
15	XTAL1	Crystal Oscillator	Input
16–18	P31–P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	$\overline{AS}$	Address Strobe	Output
21	$\overline{RESET}$	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26–27	P00–P01	Port 0, Pins 0,1	In/Output
28–29	P10–P11	Port 1, Pins 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground	
32–33	P12–P13	Port 1, Pins 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35–39	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output
40	$\overline{DS}$	Data Strobe	Output

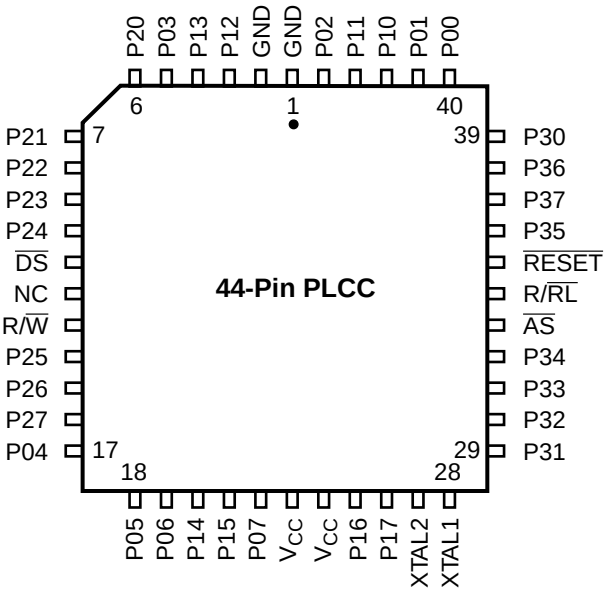


Figure 4. 44-Pin PLCC Pin Configuration
Standard Mode

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1–2	GND	Ground	
3–4	P12–P13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6–10	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output
11	$\overline{DS}$	Data Strobe	Output
12	NC	No Connection	
13	R/$\overline{W}$	Read/Write	Output
14–16	P25–P27	Port 2, Pins 5,6,7	In/Output
17–19	P04–P06	Port 0, Pins 4,5,6	In/Output
20–21	P14–P15	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23–24	V_{CC}	Power Supply	
25–26	P16–P17	Port 1, Pins 6,7	In/Output
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29–31	P31–P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
33	$\overline{AS}$	Address Strobe	Output
34	R/$\overline{RL}$	ROM/ROMless select	Input
35	$\overline{RESET}$	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40–41	P00–P01	Port 0, Pins 0,1	In/Output
42–43	P10–P11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

PIN IDENTIFICATION (Continued)

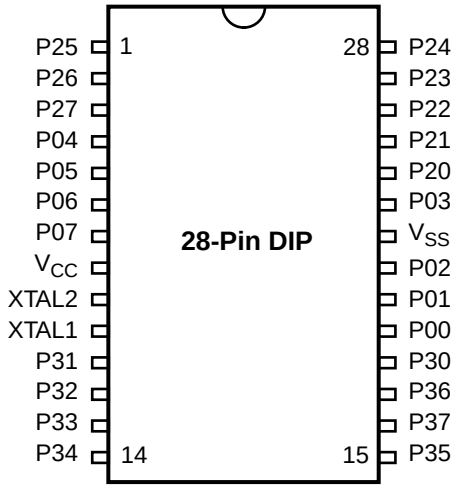


Figure 9. Standard Mode 28-Pin DIP/SOIC Pin Configuration

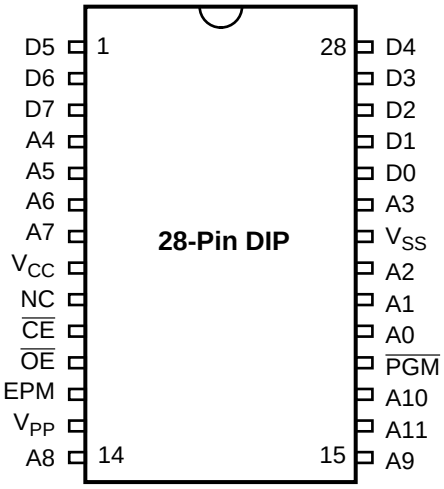


Figure 10. EPROM Programming Mode 28-Pin DIP/SOIC Pin Configuration

Table 7. 28-Pin DIP/SOIC/PLCC Pin Identification*

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Pins 5,6,	In/Output
4–7	P04–P07	Port 0, Pins 4,5,6,7	In/Output
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11–13	P31–P33	Port 3, Pins 1,2,3	Input
14–15	P34–P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19–21	P00–P02	Port 0, Pins 0,1,2	In/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24–28	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output

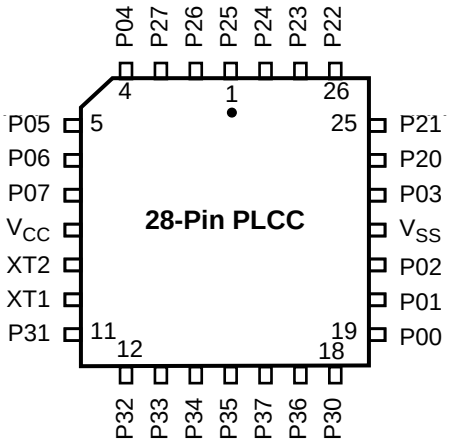


Figure 11. Standard Mode 28-Pin PLCC Pin Configuration

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

			T_A= 0 °C to +70 °C					
Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V 5.5V	0.7 V_{CC} 0.7 V_{CC}	V_{CC}+0.3 V_{CC}+0.3	1.8 2.5	V V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V 4.5V	GND -0.3 GND -0.3	0.2 V_{CC} 0.2 V_{CC}	0.9 1.5	V V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V 5.5V	0.7 V_{CC} 0.7 V_{CC}	V_{CC}+0.3 V_{CC}+0.3	2.5 2.5	V V		
V_{IL}	Input Low Voltage	3.5V 5.5V	GND -0.3 GND -0.3	0.2 V_{CC} 0.2 V_{CC}	1.5 1.5	V V		
V_{OH}	Output High Voltage Low EMI Mode	3.5V 5.5V	V_{CC} -0.4 V_{CC} -0.4		3.3 4.8	V V	I_{OH} = – 0.5 mA	
V_{OH1}	Output High Voltage	3.5V 5.5V	V_{CC} -0.4 V_{CC} -0.4		3.3 4.8	V V	I_{OH} = -2.0 mA I_{OH} = -2.0 mA	
V_{OL}	Output Low Voltage Low EMI Mode	3.5V 4.5V		0.4 0.4	0.2 0.2	V V	I_{OL} = 1.0 mA I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	3.5V 4.5V		0.4 0.4	0.1 0.1	V V	I_{OL} = + 4.0 mA I_{OL} = + 4.0 mA	8 8
V_{OL2}	Output Low Voltage	3.5V 4.5V		1.2 1.2	0.5 0.5	V V	I_{OL} = + 12 mA I_{OL} = + 12 mA	8 8
V_{RH}	Reset Input High Voltage	3.5V 5.5V	.8 V_{CC} .8 V_{CC}	V_{CC} V_{CC}	1.7 2.1	V V		
V_{RL}	Reset Input Low Voltage	3.5V 5.5V	GND -0.3 GND -0.3	0.2 V_{CC} 0.2 V_{CC}	1.3 1.7	V V		13
V_{OLR}	Reset Output Low Voltage	3.5V 5.5V		0.6 0.6	0.3 0.2	V V	I_{OL} = 1.0 mA I_{OL} = 1.0 mA	
V_{OFFSET}	Comparator Input Offset Voltage	3.5V 4.5V		25 25	10 10	mV mV		
V_{ICR}	Input Common Mode Voltage Range	3.5V 5.5V	0 0	V_{CC} -1.0V V_{CC} -1.0V		V V		10 10
I_{IL}	Input Leakage	3.5V 4.5V	-1 -1	2 2	0.032 0.032	µA µA	V_{IN} = 0V, V_{CC} V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V 4.5V	-1 -1	2 2	0.032 0.032	µA µA	V_{IN} = 0V, V_{CC} V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.5V 4.5V	-20 -20	-130 -180	-65 -112	µA µA		

Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
			T_A=–40 °C to +105 °C					
V_{CH}	Clock Input High Voltage	4.5V 5.5V	0.7 V_{CC} 0.7 V_{CC}	V_{CC}+0.3 V_{CC}+0.3	2.5 2.5	V V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V 5.5V	GND-0.3 GND-0.3	0.2 V_{CC} 0.2 V_{CC}	1.5 1.5	V V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V 5.5V	0.7 V_{CC} 0.7 V_{CC}	V_{CC}+0.3 V_{CC}+0.3	2.5 2.5	V V		
V_{IL}	Input Low Voltage	4.5V 5.5V	GND-0.3 GND-0.3	0.2 V_{CC} 0.2 V_{CC}	1.5 1.5	V V		
V_{OH}	Output High Voltage Low EMI Mode	4.5V 5.5V	V_{CC} -0.4 V_{CC} -0.4		4.8 4.8	V V	I_{OH} = – 0.5 mA I_{OH} = – 0.5 mA	8 8
V_{OH1}	Output High Voltage	4.5V 4.5V	V_{CC} -0.4 V_{CC} -0.4		4.8 4.8	V V	I_{OH} = -2.0 mA I_{OH} = -2.0 mA	8 8
V_{OL}	Output Low Voltage Low EMI Mode	4.5V 5.5V		0.4 0.4	0.2 0.2	V V	I_{OL} = 1.0 mA I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	4.5V 5.5V		0.4 0.4	0.1 0.1	V V	I_{OL} = + 4.0 mA I_{OL} = +4.0 mA	8 8
V_{OL2}	Output Low Voltage	4.5V 5.5V		1.2 1.2	0.5 0.5	V V	I_{OL} = + 12 mA I_{OL} = + 12 mA	8 8
V_{RH}	Reset Input High Voltage	3.5V 5.5V	.8 V_{CC} .8 V_{CC}	V_{CC} V_{CC}	1.7 2.1	V V		13 13
V_{OLR}	Reset Output Low Voltage	3.5V 5.5V		0.6 0.6	0.3 0.2	V V	I_{OL} = 1.0 mA I_{OL} = 1.0 mA	13 13
V_{OFFSET}	Comparator Input Offset Voltage	4.5V 5.5V		25 25	10 10	mV mV		
V_{ICR}	Input Common Mode Voltage Range	4.5V 5.5V	0 0	V_{CC}-1.5V V_{CC}-1.5V		V V		10 10
I_{IL}	Input Leakage	4.5V 5.5V	-1 -1	2 2	<1 <1	µA µA	V_{IN} = 0V, V_{CC} V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V 5.5V	-1 -1	2 2	<1 <1	µA µA	V_{IN} = 0V, V_{CC} V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	4.5V 5.5V	-18 -18	-180 -180	-112 -112	µA µA		
I_{CC}	Supply Current	4.5V 5.5V		25 25	20 20	mA mA	@ 16 MHz @ 16 MHz	4,5 4,5
I_{CC1}	Standby Current Halt Mode	4.5V 5.5V		8 8	3.7 3.7	mA mA	V_{IN} = 0V, V_{CC} @ 16 MHz V_{IN} = 0V, V_{CC} @ 16 MHz	4,5 4,5
I_{CC2}	Standby Current (Stop Mode)	4.5V 5.5V		10 10	2 3	µA µA	V_{IN} = 0V, V_{CC} V_{IN} = 0V, V_{CC}	6,11,14 6,11,14
I_{ALL}	Auto Latch Low Current	4.5V 5.5V	1.4 1.4	20 20	4.7 4.7	µA µA	0V < V_{IN} < V_{CC} 0V < V_{IN} < V_{CC}	9 9

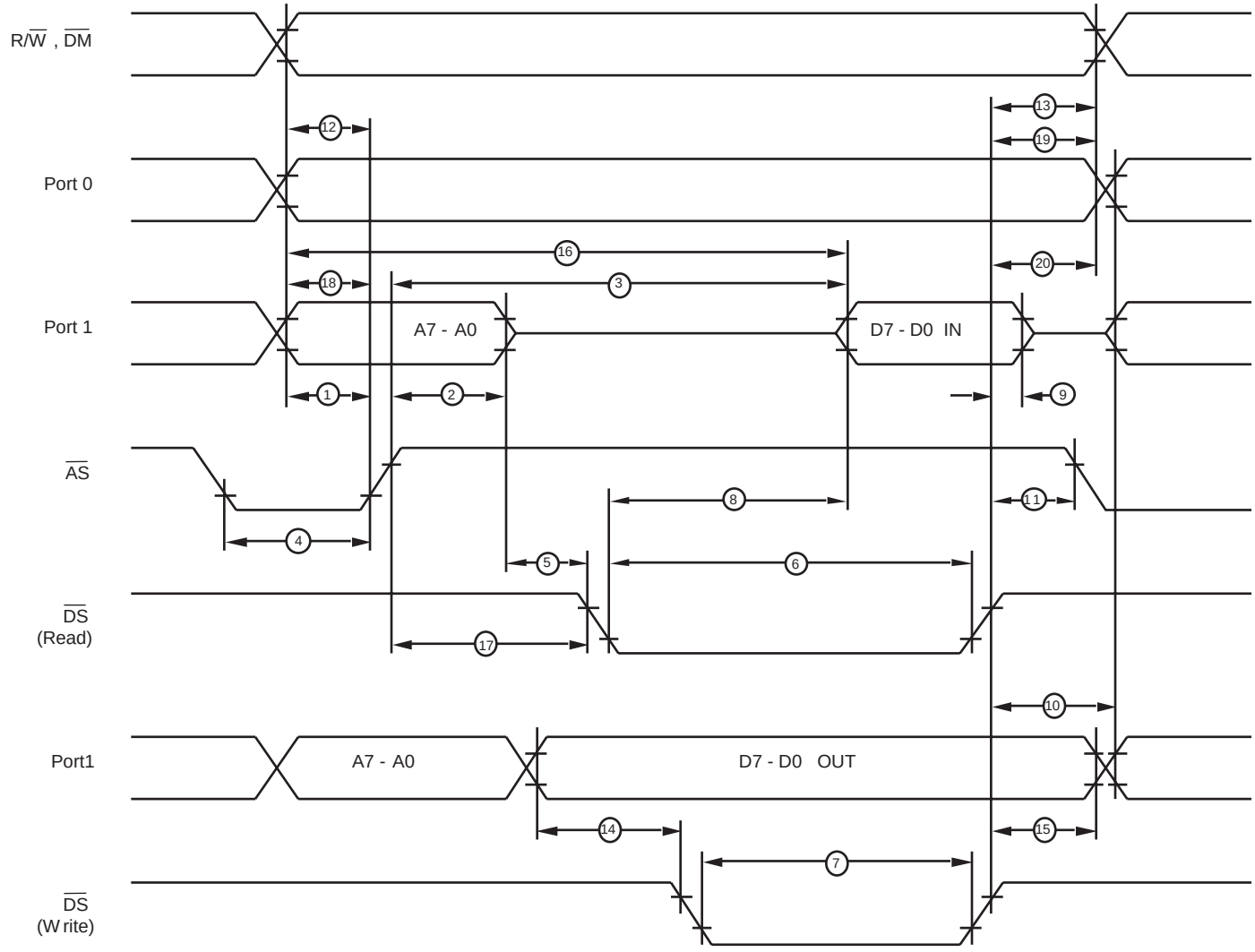


Figure 14. External I/O or Memory Read/Write Timing
Z86E40 Only

DC ELECTRICAL CHARACTERISTICS (Continued)

				T_A = 0°C to 70°C 16 MHz			
No	Symbol	Parameter	Note [3] V_{CC}	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	3.5V 5.5V	25 25		ns ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	3.5V 5.5V	35 35		ns ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	3.5V 5.5V		180 180	ns ns	1,2
4	TwAS	$\overline{AS}$ Low Width	3.5V 5.5V	40 40		ns ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	3.5V 5.5V	0 0		ns ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	3.5V 5.5V	135 135		ns ns	1,2
7	TwDSW	$\overline{DS}$ (Write) Low Width	3.5V 5.5V	80 80		ns ns	1,2
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid	3.5V 5.5V		75 75	ns ns	1,2
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	3.5V 5.5V	0 0		ns ns	2
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	3.5V 5.5V	50 50		ns ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	3.5V 5.5V	35 35		ns ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	3.5V 5.5V	25 25		ns ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	3.5V 5.5V	35 35		ns ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	3.5V 5.5V	55 55	25 25	ns ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	3.5V 5.5V	35 35		ns ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.5V 5.5V		230 230	ns ns	1,2
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	3.5V 5.5V	45 45		ns ns	2
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Fall Delay	3.5V 5.5V	30 30		ns ns	2
20	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	3.5V 5.5V	35 35		ns ns	

Notes:

1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR D1 = 0, D0 = 0.

Additional Timing Table (Divide-By-One Mode)

				T_A = 0 °C to +70 °C		T_A = -40 °C to +105 °C			
				4 MHz		4 MHz			
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.5V	250	DC	250	DC	ns	1,7,8
			5.5V	250	DC	250	DC	ns	1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		25		25	ns	1,7,8
			5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	3.5V	100		100		ns	1,7,8
			5.5V	100		100		ns	1,7,8
4	TwTinL	Timer Input Low Width	3.5V	100		100		ns	1,7,8
			5.5V	70		70		ns	1,7,8
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC			1,7,8
			5.5V	5TpC		5TpC			1,7,8
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC			1,7,8
			5.5V	8TpC		8TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns	1,7,8
			5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low Time	3.5V	100		100		ns	1,2,7,8
			5.5V	70		70		ns	1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC			1,3,7,8
			5.5V	5TpC		5TpC			1,3,7,8
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC			1,2,7,8
			5.5V	5TpC		5TpC			1,2,7,8
10	Twsm	STOP Mode Recovery Width Spec	3.5V	12		12		ns	4,8
			5.5V	12		12		ns	4,8
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC		4,8,9
			5.5V		5TpC				

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31–P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 1, POR STOP Mode Delay is on.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V and the V_{CC} voltage specification of 3.5V guarantees 3.5V only.
7. SMR D1 = 0.
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

PIN FUNCTIONS (Continued)

Port 1 (P17–P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7–A0) and Data (D7–D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and /DAV1 (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (Figure 19).

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z86E40 to share common resources in multiprocessor and DMA applications.

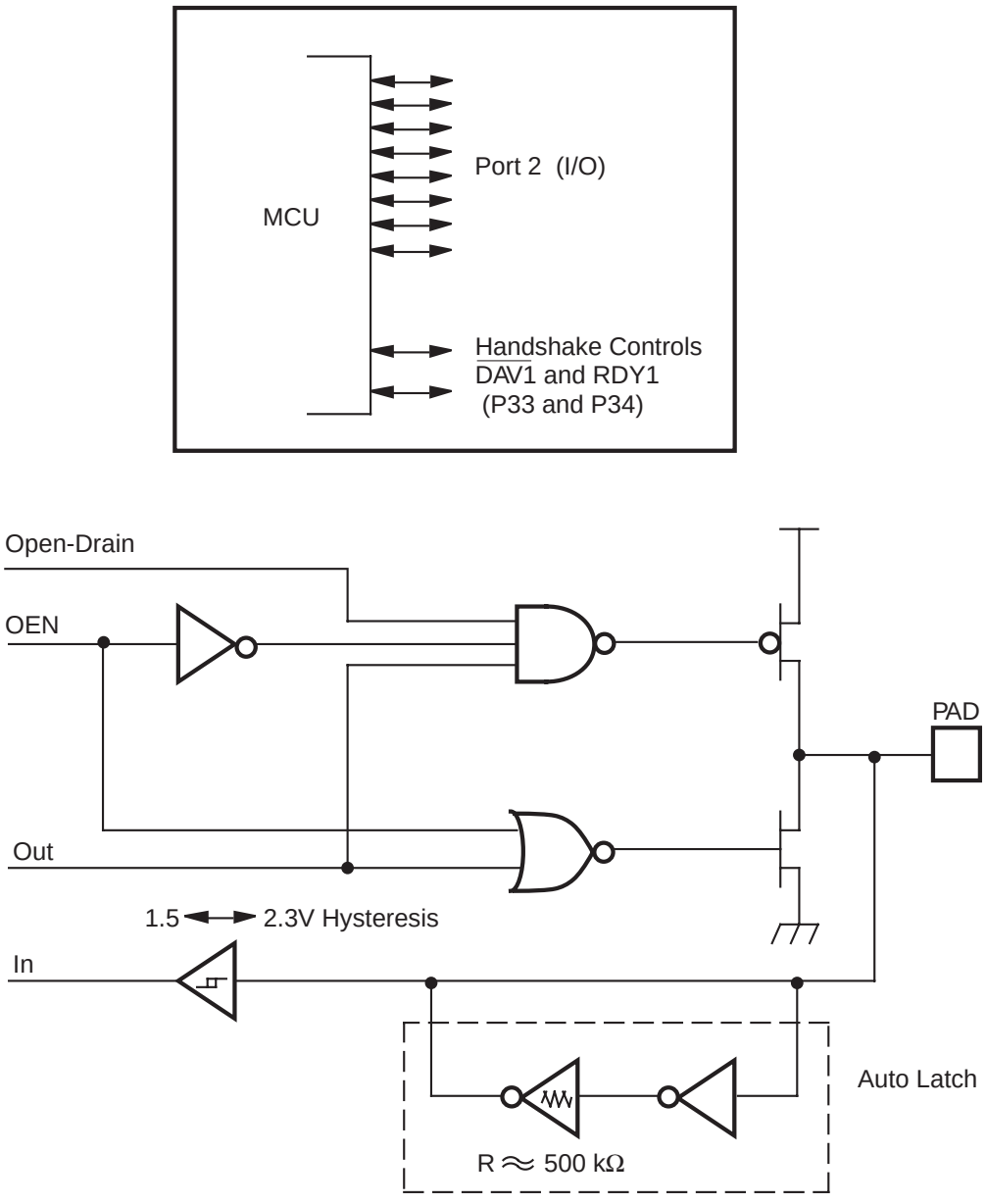


Figure 19. Port 1 Configuration (Z86E40 Only)

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register (IPR). An interrupt machine cycle is activated when an interrupt request is granted. Thus, disabling all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in bits D7 and D6 of the IRQ Register (R250). The configuration is shown in Table 11.

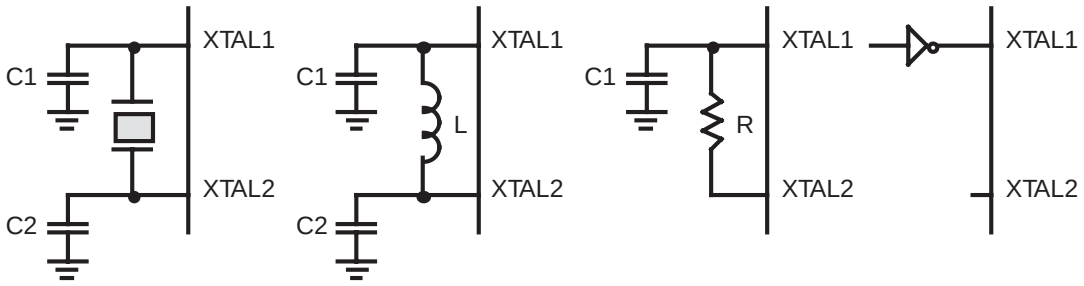
Table 11. IRQ Register Configuration

IRQ		Interrupt Edge	
D7	**D6**	**P31**	**P32**
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 KHz to 16 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to device pin Ground. The RC oscillator option can be selected in the programming mode. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Figure 29).



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
F = 8 MHz

LC
C1, C2 = 22 pF

L = 130 µH *
F = 3 MHz *

RC
@ 5V Vcc (TYP)

C1 = 100 pF
R = 2K
F = 6 MHz

External Clock

* Typical value including pin parasitics

Figure 29. Oscillator Configuration

SCLK/TCLK Divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (i.e., D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake up source of the STOP-Mode Recovery (Figure 32). Table 12 shows the SMR source selected with the setting of D2 to D4. P33–P31 cannot be used to wake up from STOP mode when programmed as analog inputs. When the STOP-Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: If the Port2 pin is configured as an output, this output level will be read by the SMR circuitry.

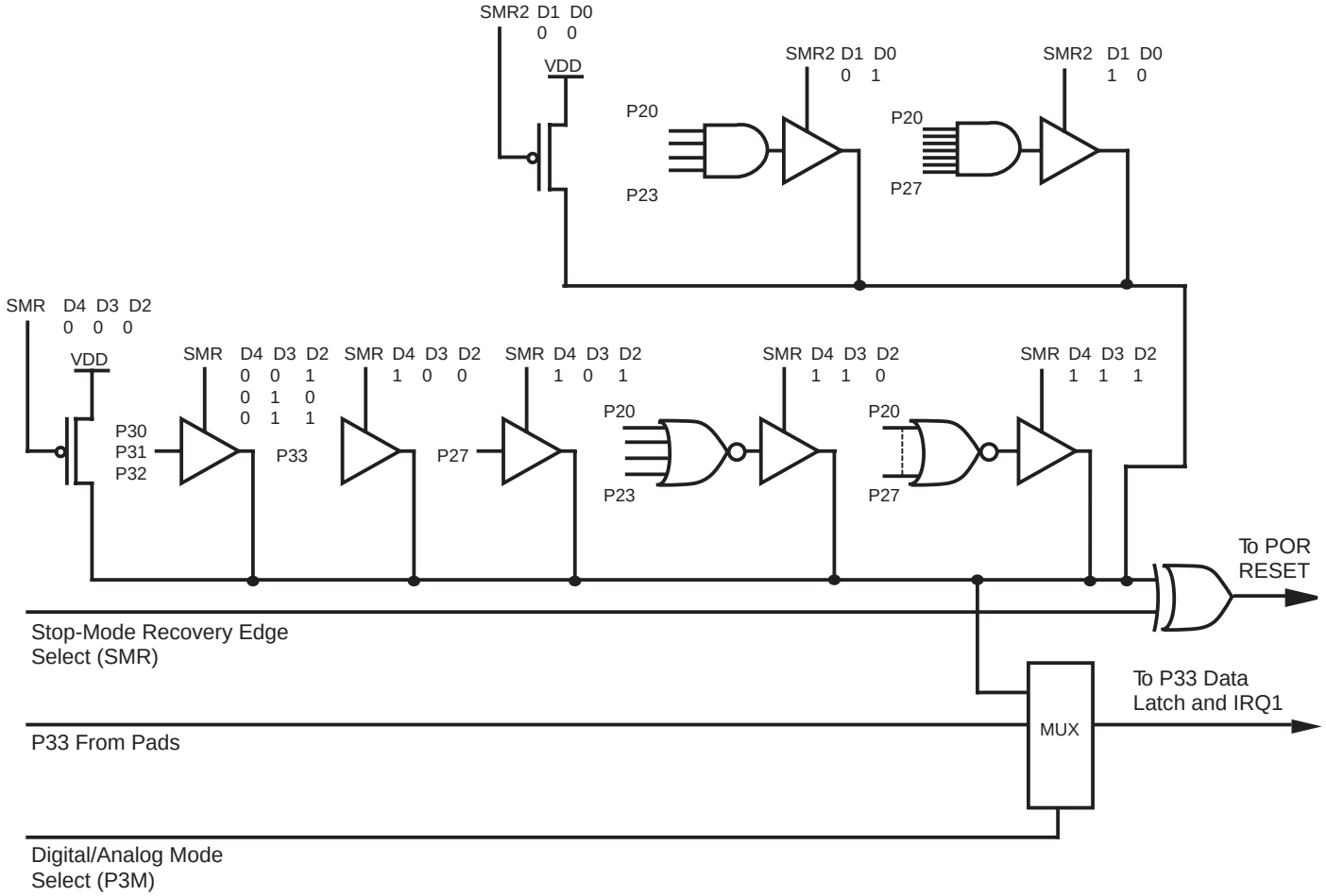


Figure 32. Stop-Mode Recovery Source

FUNCTIONAL DESCRIPTION (Continued)

Table 12. Stop-Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0–3
1	1	1	Logical NOR of Port 2 bits 0–7

Stop-Mode Recovery Delay Select (D5). The 5 ms RESET delay after Stop-Mode Recovery is disabled by programming this bit to a zero. A “1” in this bit will cause a 5 ms RESET delay after Stop-Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the Stop-Mode Recovery source needs to be kept active for at least 5TpC.

Stop-Mode Recovery Level Select (D6). A “1” in this bit defines that a high level on any one of the recovery sources wakes the MCU from STOP Mode. A 0 defines low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A “0” in this bit indicates that the device has been reset by POR (cold). A “1” in this bit indicates the device was awakened by a SMR source (warm).

Stop-Mode Recovery Register 2 (SMR2). This register contains additional Stop-Mode Recovery sources. When the Stop-Mode Recovery sources are selected in this register then SMR Register. Bits D2, D3, and D4 must be 0.

SMR:10		Operation
D1	**D0**	**Description of Action**
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is disabled after Power-On Reset and initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT is driven either by an on-board RC oscillator or an external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register.

Note: Execution of the WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags.

WDT Time-Out Period (D0 and D1). Bits 0 and 1 control a tap circuit that determines the time-out periods that can be obtained (Table 13). The default value of D0 and D1 are 1 and 0, respectively.

Table 13. Time-out Period of WDT

D1	D0	Time-out of the Internal RC OSC	Time-out of the System Clock
0	0	5 ms	128 SCLK
0	1	10 ms*	256 SCLK*
1	0	20 ms	512 SCLK
1	1	80 ms	2048 SCLK

Notes:
*The default setting is 10 ms.

WDT During HALT Mode (D2). This bit determines whether or not the WDT is active during HALT Mode. A “1” indicates that the WDT is active during HALT. A “0” disables the WDT in HALT Mode. The default value is “1”.

WDT During STOP Mode (D3). This bit determines whether or not the WDT is active during STOP mode. A “1” indicates active during STOP. A “0” disables the WDT during STOP Mode. This is applicable only when the WDT clock source is the internal RC oscillator.

Clock Source For WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1, and the WDT is stopped in STOP Mode. The default configuration of this bit is 0, which selects the RC oscillator.

Permanent WDT. When this feature is enabled, the WDT is enabled after reset and will operate in Run and Halt Mode. The control bits in the WDTMR do not affect the WDT operation. If the clock source of the WDT is the internal RC oscillator, then the WDT will run in STOP mode. If the clock source of the WDT is the XTAL1 pin, then the WDT will not run in STOP mode.

Note: WDT time-out in STOP Mode will not reset SMR,SMR2,PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers.

WDTMR Register Accessibility. The WDTMR register is accessible only during the **first 60** internal system clock

Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{LV} (Figure 35).

Note: V_{CC} must be in the allowed operating range prior to the minimum Power-On Reset time-out (T_{POR}).

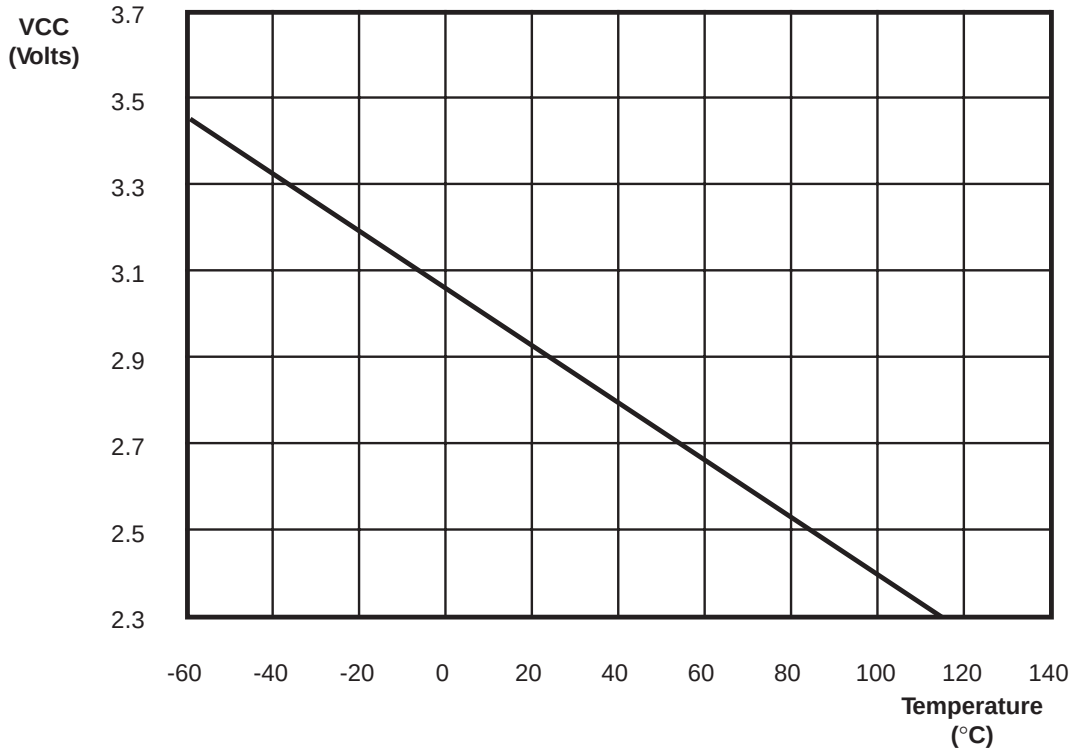


Figure 35. Typical Z86E40 V_{LV} Voltage vs. Temperature

Table 14. EPROM Programming Table

Programming Modes	V_{PP}	EPM	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	ADDR	DATA	V_{CC}*
EPROM READ1	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	4.5V†
EPROM READ2	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.5V†
PROGRAM	V_H	V_H	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.4V
PROGRAM VERIFY	V_H	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.0V
OPTION BIT PGM	V_H	V_H	V_{IL}	V_{IH}	V_{IL}	63	IN	6.4V
OPTION BIT READ	X	V_H	V_{IL}	V_{IL}	V_{IH}	63	OUT	6.0V

Notes:
V_H = 13.0 V ± 0.1 V
V_{IH} = As per specific Z8 DC specification
VIL= As per specific Z8 DC specification
X=Not used, but must be set to V_H, V_{IH}, or V_{IL} level.
NU = Not used, but must be set to either V_{IH} or V_{IL} level.
I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum.
*V_{CC} has a tolerance of ±0.25V.
† Zilog recommends an EPROM read at V_{CC} = 4.5 V and 5.5 V to ensure proper device operations during the V_{CC} after programming, but V_{CC} = 5.0 V is acceptable.

Table 15. EPROM Programming Timing

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95	1.05	ms
7	Data Hold Time	2		µs
8	$\overline{OE}$ Setup Time	2		µs
9	Data Access Time	200		ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width/Option Program Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	$\overline{PGM}$ Setup Time	2		µs
14	Address to $\overline{OE}$ Setup Time	2		µs
15	$\overline{OE}$ Width	250		ns
16	Address to $\overline{OE}$ Low	125		ns

Z86E40 TIMING DIAGRAMS (Continued)

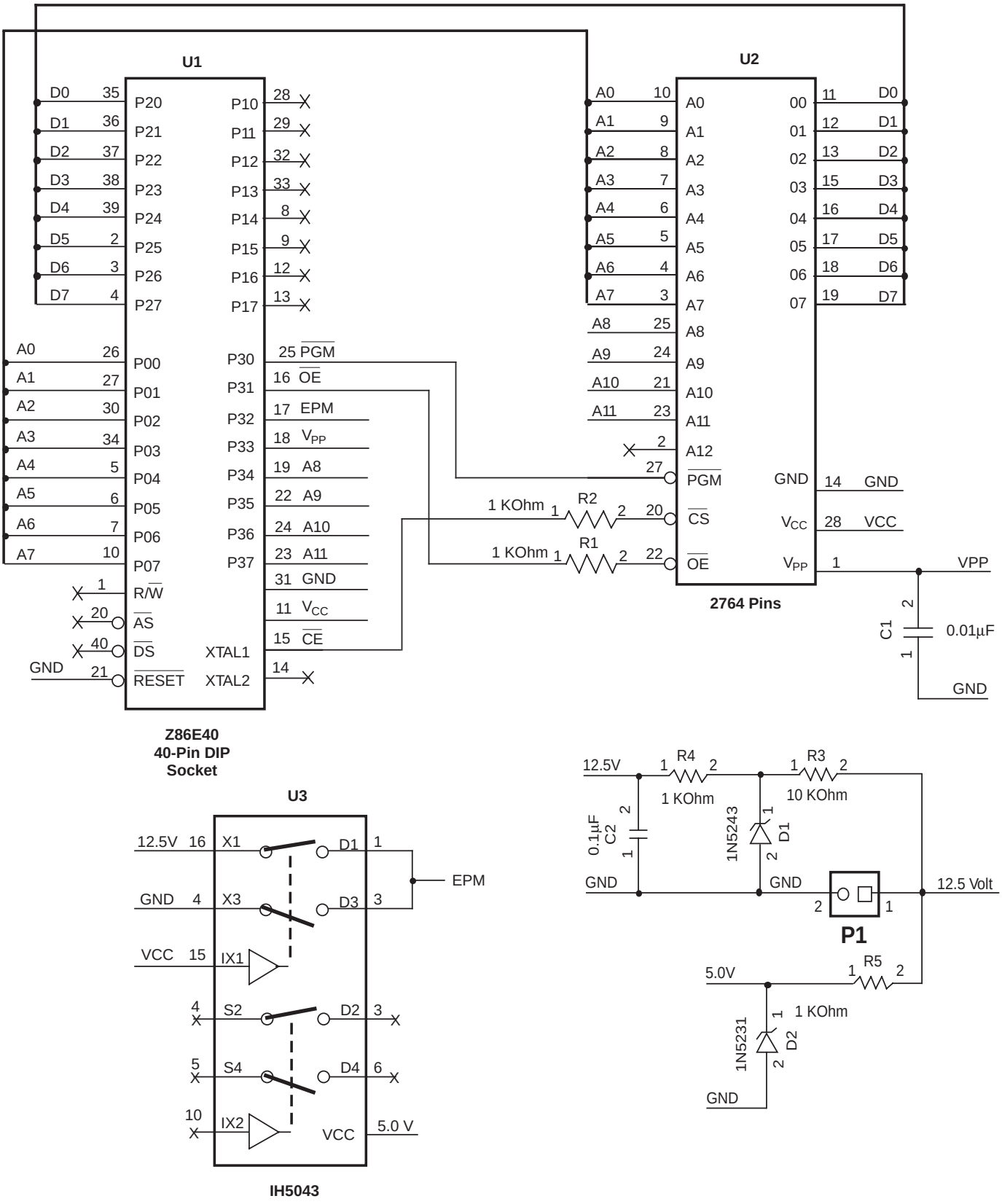


Figure 38. Z86E40 Z8 OTP Programming Adapter
For use with Standard EPROM Programmers

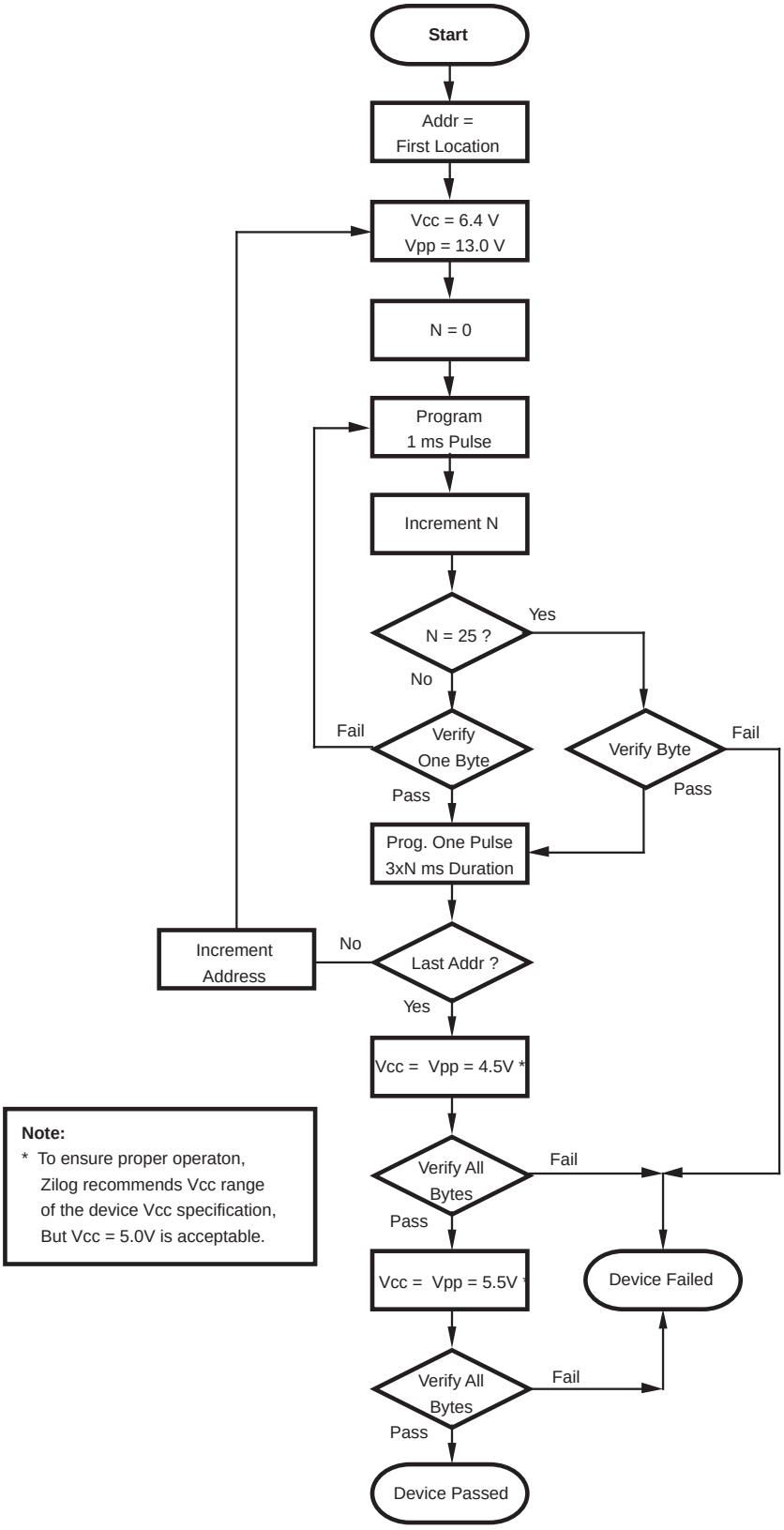


Figure 40. Z86E40 Programming Algorithm

Z8 CONTROL REGISTER DIAGRAMS

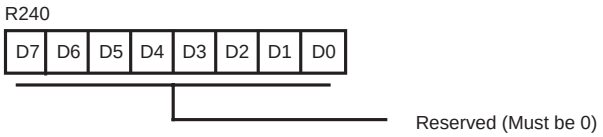


Figure 45. Reserved

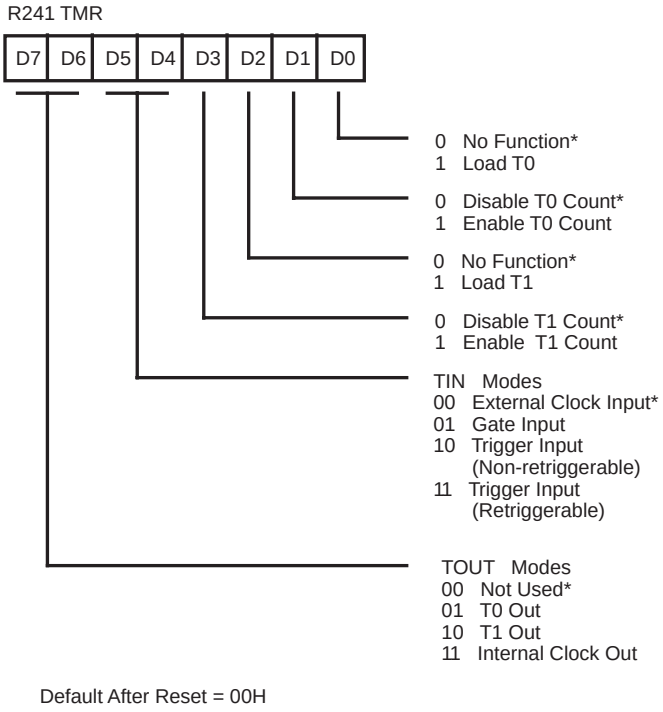


Figure 46. Timer Mode Register
F1H: Read/Write

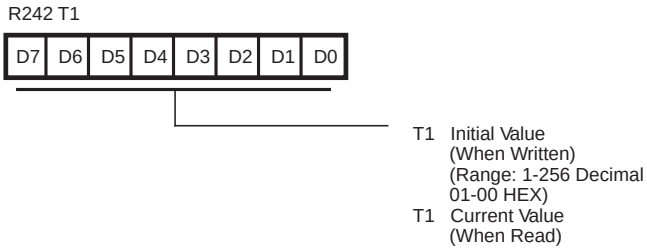


Figure 47. Counter/Timer 1 Register
F2H: Read/Write

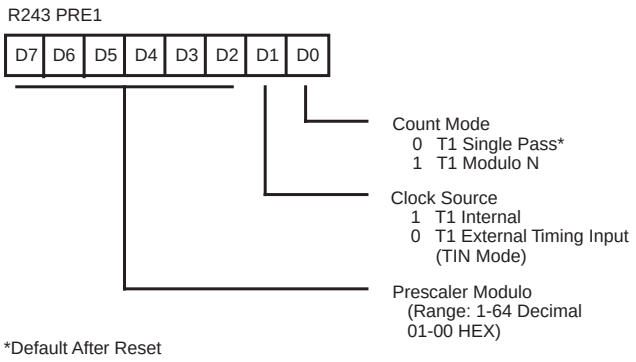


Figure 48. Prescaler 1 Register
F3H: Write Only

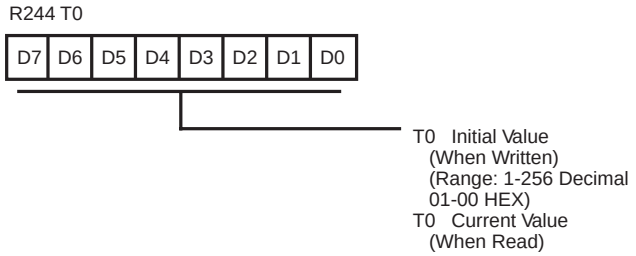


Figure 49. Counter/Timer 0 Register
F4H; Read/Write

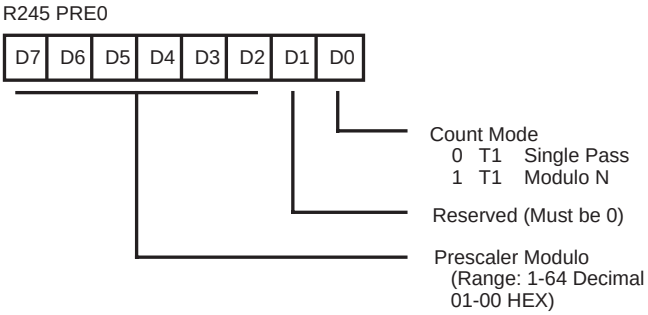
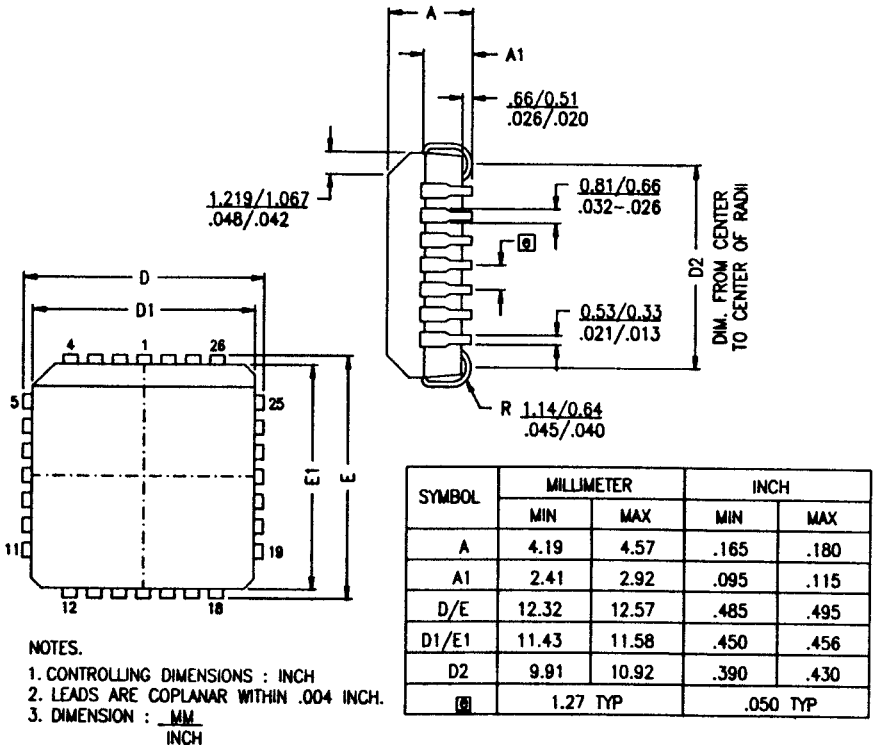


Figure 50. Prescaler 0 Register
F5H: Write Only



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.19	4.57	.165	.180
A1	2.41	2.92	.095	.115
D/E	12.32	12.57	.485	.495
D1/E1	11.43	11.58	.450	.456
D2	9.91	10.92	.390	.430
e	1.27 TYP		.050 TYP	

Figure 66. 28-Pin PLCC Package Diagram

Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.