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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	2KB (2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e3116vec

PIN IDENTIFICATION (Continued)

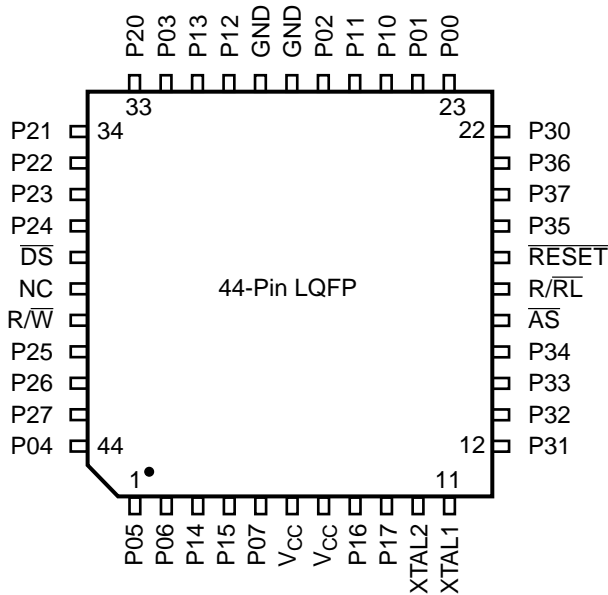


Figure 5. 44-Pin LQFP Pin Configuration
Standard Mode

Table 3. 44-Pin LQFP Pin Identification

Pin #	Symbol	Function	Direction
1–2	P05–P06	Port 0, Pins 5,6	In/Output
3–4	P14–P15	Port 1, Pins 4,5	In/Output
5	P07	Port 0, Pin 7	In/Output
6–7	V _{CC}	Power Supply	
8–9	P16–P17	Port 1, Pins 6,7	In/Output
10	XTAL2	Crystal Oscillator	Output
11	XTAL1	Crystal Oscillator	Input
12–14	P31–P33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	AS	Address Strobe	Output
17	R/RL	ROM/ROMless select	Input
18	RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23–24	P00–P01	Port 0, Pin 0,1	In/Output
25–26	P10–P11	Port 1, Pins 0,1	In/Output

Table 3. 44-Pin LQFP Pin Identification

Pin #	Symbol	Function	Direction
27	P02	Port 0, Pin 2	In/Output
28–29	GND	Ground	
30–31	P12–P13	Port 1, Pins 2,3	In/Output
32	P03	Port 0, Pin 3	In/Output
33–37	P20–4	Port 2, Pins 0,1,2,3,4	In/Output
38	DS	Data Strobe	Output
39	NC	No Connection	
40	R/W	Read/Write	Output
41–43	P25–P27	Port 2, Pins 5,6,7	In/Output
44	P04	Port 0, Pin 4	In/Output

PIN IDENTIFICATION (Continued)

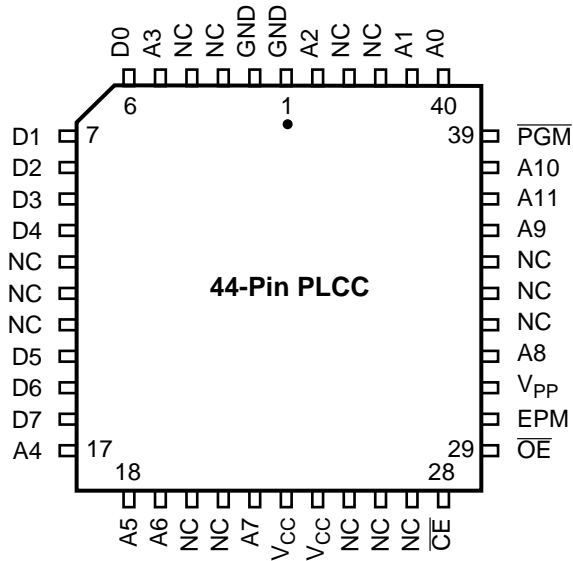


Figure 7. 44-Pin PLCC Pin Configuration
EPROM Programming Mode

Table 5. 44-Pin PLCC Pin Configuration
EPROM Programming Mode

Pin #	Symbol	Function	Direction
1–2	GND	Ground	
3–4	NC	No Connection	
5	A3	Address 3	Input
6–10	D0–D4	Data 0,1,2,3,4	In/Output
11–13	NC	No Connection	
14–16	D5–D7	Data 5,6,7	In/Output
17–19	A4–A6	Address 4,5,6	Input
20–21	NC	No Connection	
22	A7	Address 7	Input
23–24	V _{CC}	Power Supply	
25–27	NC	No Connection	
28	CE	Chip Select	Input
29	OE	Output Enable	Input
30	EPM	EPROM Prog. Mode	Input

Table 5. 44-Pin PLCC Pin Configuration
EPROM Programming Mode

Pin #	Symbol	Function	Direction
31	V _{PP}	Prog. Voltage	Input
32	A8	Address 8	Input
33–35	NC	No Connection	
36	A9	Address 9	Input
37	A11	Address 11	Input
38	A10	Address 10	Input
39	PGM	Prog. Mode	Input
40–41	A0,A1	Address 0,1	Input
42–43	NC	No Connection	
44	A2	Address 2	Input

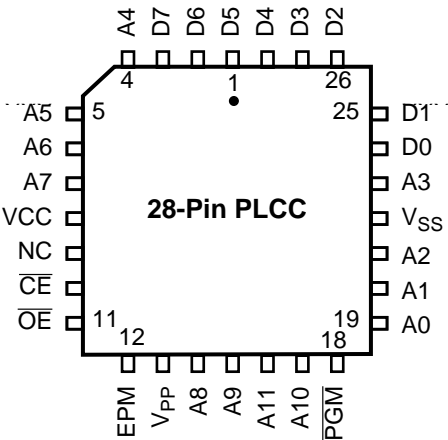
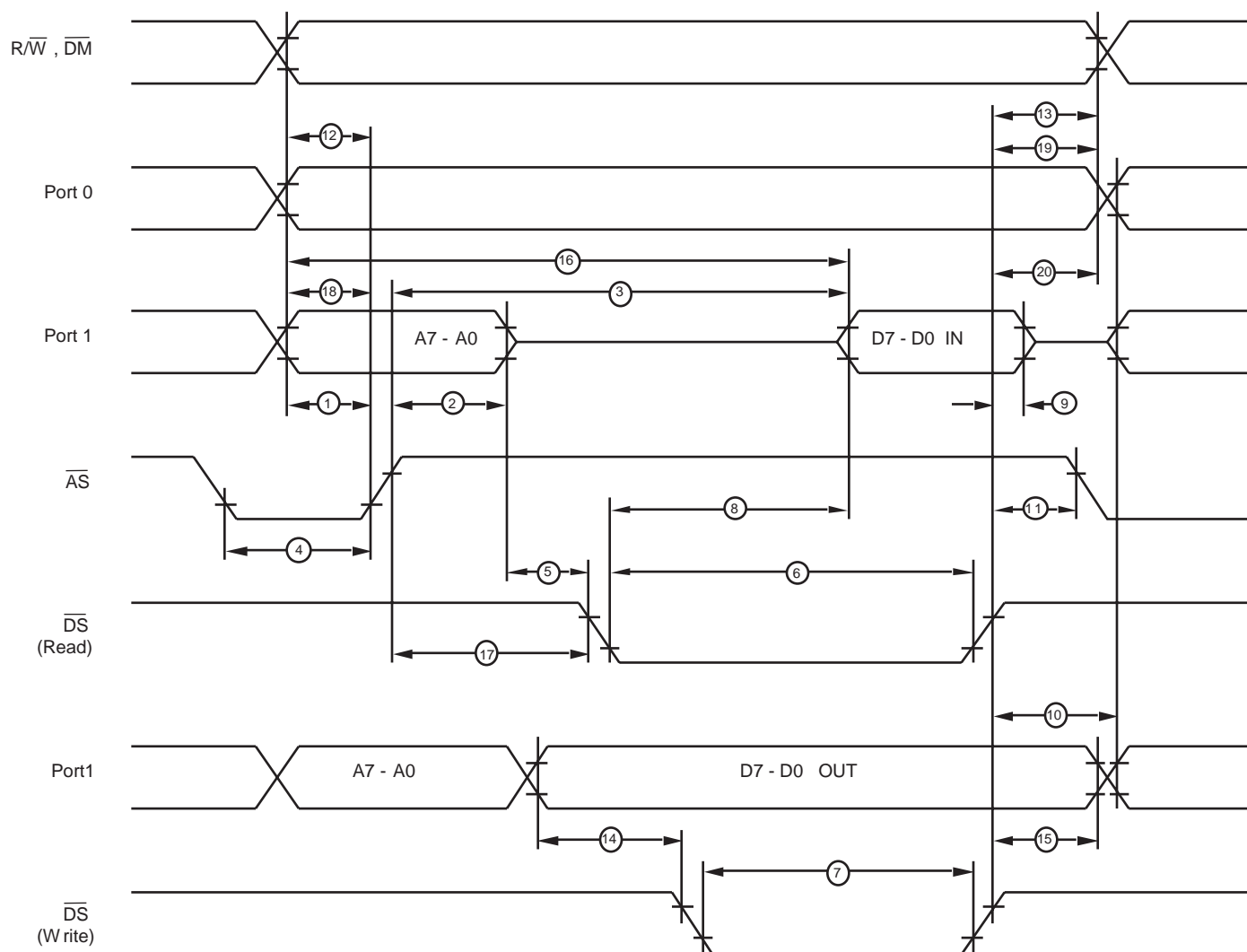


Figure 12. EPROM Programming Mode
28-Pin PLCC Pin Configuration

Table 8. 28-Pin EPROM
Pin Identification

Pin #	Symbol	Function	Direction
1–3	D5–D7	Data 5,6,7	In/Output
4–7	A4–A7	Address 4,5,6,7	Input
8	V _{CC}	Power Supply	
9	NC	No connection	
10	$\overline{\text{CE}}$	Chip Select	Input
11	$\overline{\text{OE}}$	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V _{PP}	Prog. Voltage	Input
14–15	A8–A9	Address 8,9	Input
16	A11	Address 11	Input
17	A10	Address 10	Input
18	$\overline{\text{PGM}}$	Prog. Mode	Input
19–21	A0–A2	Address 0,1,2	Input
22	V _{SS}	Ground	
23	A3	Address 3	Input
24–28	D0–D4	Data 0,1,2,3,4	In/Output



**Figure 14. External I/O or Memory Read/Write Timing
Z86E40 Only**

T _A = -40°C to 105°C 16 MHz							
No	Symbol	Parameter	Note [3] V _{CC}	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to \overline{AS} Rise Delay	4.5V 5.5V	25 25		ns ns	2
2	TdAS(A)	\overline{ASAS} Rise to Address Float Delay	4.5V 5.5V	35 35		ns ns	2
3	TdAS(DR)	\overline{AS} Rise to Read Data Req'd Valid	4.5V 5.5V		180 180	ns ns	1,2
4	TwAS	\overline{AS} Low Width	4.5V 5.5V	40 40		ns ns	2
5	TdAS(DS)	Address Float to \overline{DS} Fall	4.5V 5.5V	0 0		ns ns	
6	TwDSR	\overline{DS} (Read) Low Width	4.5V 5.5V	135 135		ns ns	1,2
7	TwDSW	\overline{DS} (Write) Low Width	4.5V 5.5V	80 80		ns ns	1,2
8	TdDSR(DR)	\overline{DS} Fall to Read Data Req'd Valid	4.5V 5.5V		75 75	ns ns	1,2
9	ThDR(DS)	Read Data to \overline{DS} Rise Hold Time	4.5V 5.5V	0 0		ns ns	2
10	TdDS(A)	\overline{DS} Rise to Address Active Delay	4.5V 5.5V	50 50		ns ns	2
11	TdDS(AS)	\overline{DS} Rise to \overline{AS} Fall Delay	4.5V 5.5V	35 35		ns ns	2
12	TdR/W(AS)	R/ \overline{W} Valid to \overline{AS} Rise Delay	4.5V 5.5V	25 25		ns ns	2
13	TdDS(R/W)	\overline{DS} Rise to R/ \overline{W} Not Valid	4.5V 5.5V	35 35		ns ns	2
14	TdDW(DSW)	Write Data Valid to \overline{DS} Fall (Write) Delay	4.5V 5.5V	55 55	25 25	ns ns	2
15	TdDS(DW)	\overline{DS} Rise to Write Data Not Valid Delay	4.5V 5.5V	35 35		ns ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	4.5V 5.5V		230 230	ns ns	1,2
17	TdAS(DS)	\overline{AS} Rise to \overline{DS} Fall Delay	4.5V 5.5V	45 45		ns ns	2
18	TdDM(AS)	/DM Valid to \overline{AS} Fall Delay	4.5V 5.5V	30 30		ns ns	2
20	ThDS(AS)	\overline{DS} Valid to Address Valid Hold Time	4.5V 5.5V	35 35		ns ns	

Notes:

1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

DC ELECTRICAL CHARACTERISTICS (Continued)

Handshake Timing Diagrams

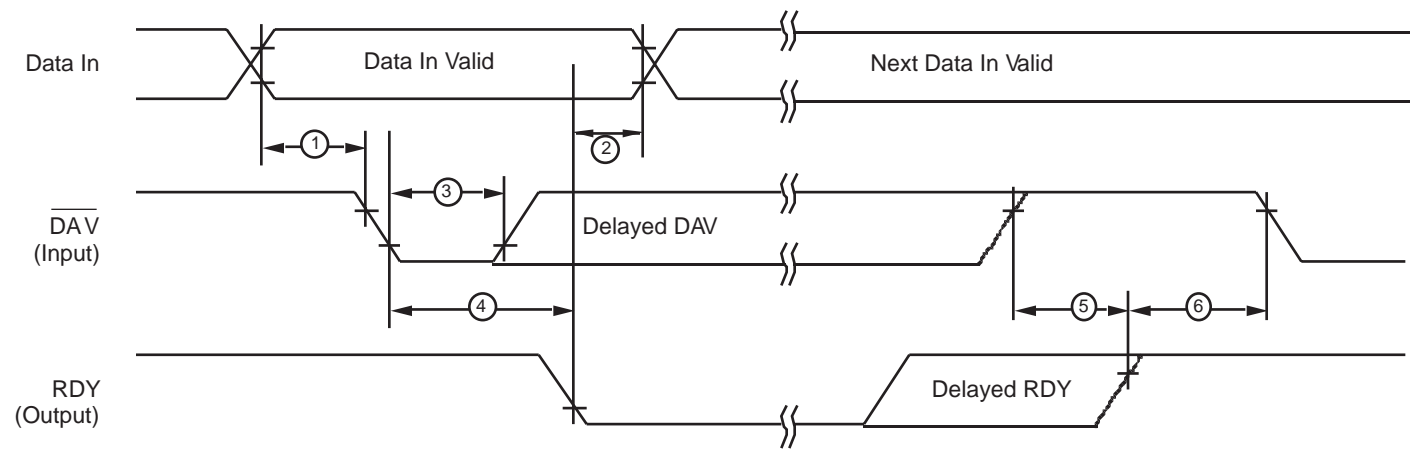


Figure 16. Input Handshake Timing

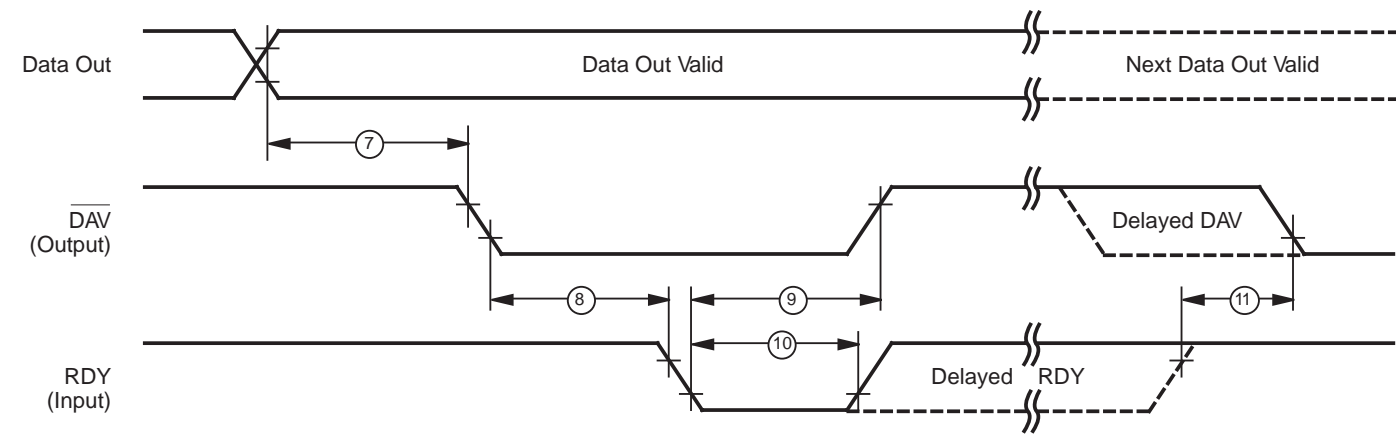


Figure 17. Output Handshake Timing

Port 0 (P07–P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble programmed. Either nibble output that can be globally programmed as push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can be placed under handshake control. In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11–A8 (lower nibble) or A15–A8 (lower and upper

nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. In ROMless mode, after a hardware reset, Port 0 is configured as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include re-configuration to eliminate this extended timing mode. In ROM mode, Port 0 is defined as input after reset.

Port 0 can be set in the High-Impedance Mode if selected as an address output state, along with Port 1 and the control signals \overline{AS} , \overline{DS} , and R/\overline{W} (Figure 18).

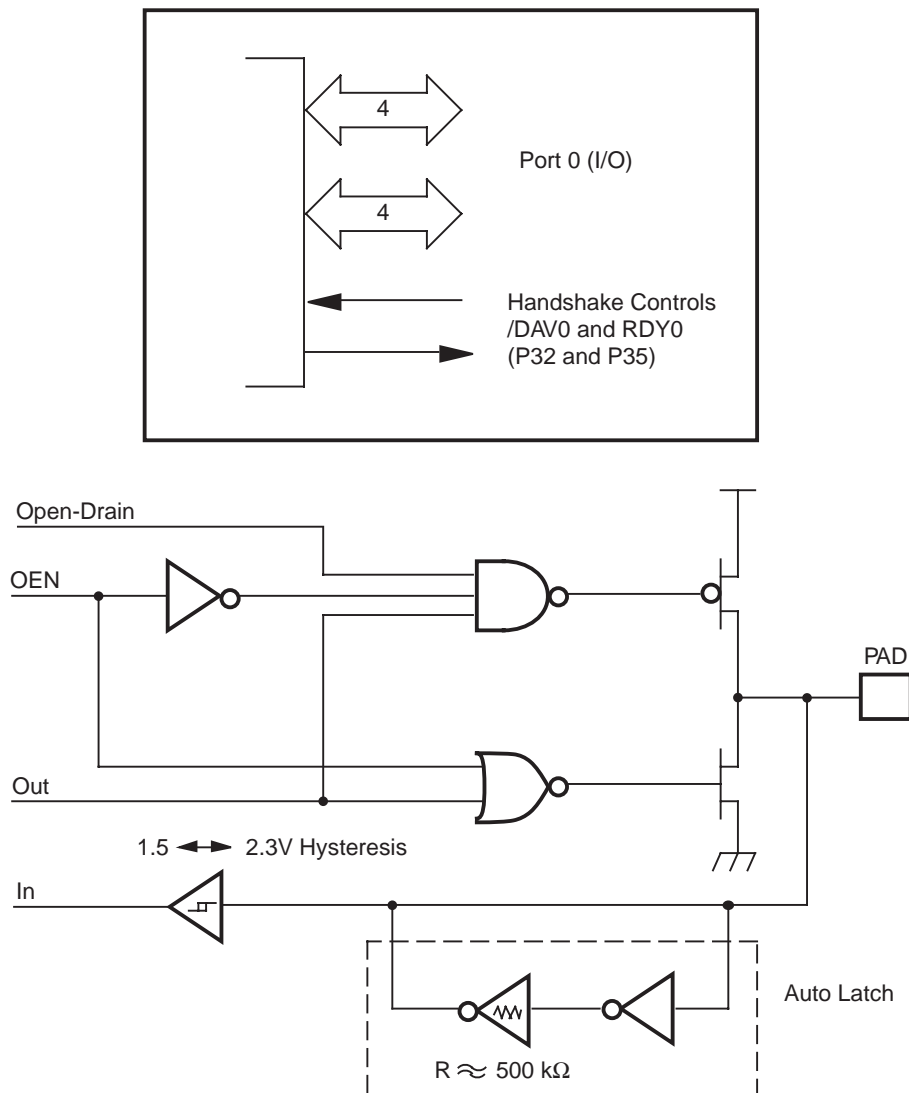


Figure 18. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37–P30). Port 3 is an 8-bit, CMOS-compatible port with four fixed inputs (P33–P30) and four fixed outputs (P37–P34). These eight lines can be configured by software for interrupt and handshake control functions. Port 3, Pin 0 is Schmitt-triggered. P31, P32, and P33 are standard CMOS inputs with single trip point (no Auto Latches) and P34, P35, P36, and P37 are push-pull output lines. Low EMI output buffers can be globally programmed by the software. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by setting the D1 of Port 3 Mode Register (P3M). The comparator output can be outputted from P34 and P37, respectively, by setting PCON register Bit D0 to 1 state. For the interrupt function, P30 and P33 are falling edge triggered interrupt inputs. P31 and P32 can be programmed as falling, rising or both edges triggered interrupt inputs (Figure 21). Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Port 0, Port 1, and Port 2 are also available on Port 3 (Table 9).

Note: When enabling/ or disabling analog mode, the following is recommended:

1. Allow two NOP delays before reading this comparator output.
2. Disable global interrupts, switch to analog mode, clear interrupts, and then re-enable interrupts.
3. IRQ register bits 3 to 0 must be cleared after enabling analog mode.

Note: P33–P30 differs from the Z86C30/C31/C40 in that there is no clamping diode to V_{CC} due to the EPROM high-voltage circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode.

FUNCTIONAL DESCRIPTION (Continued)

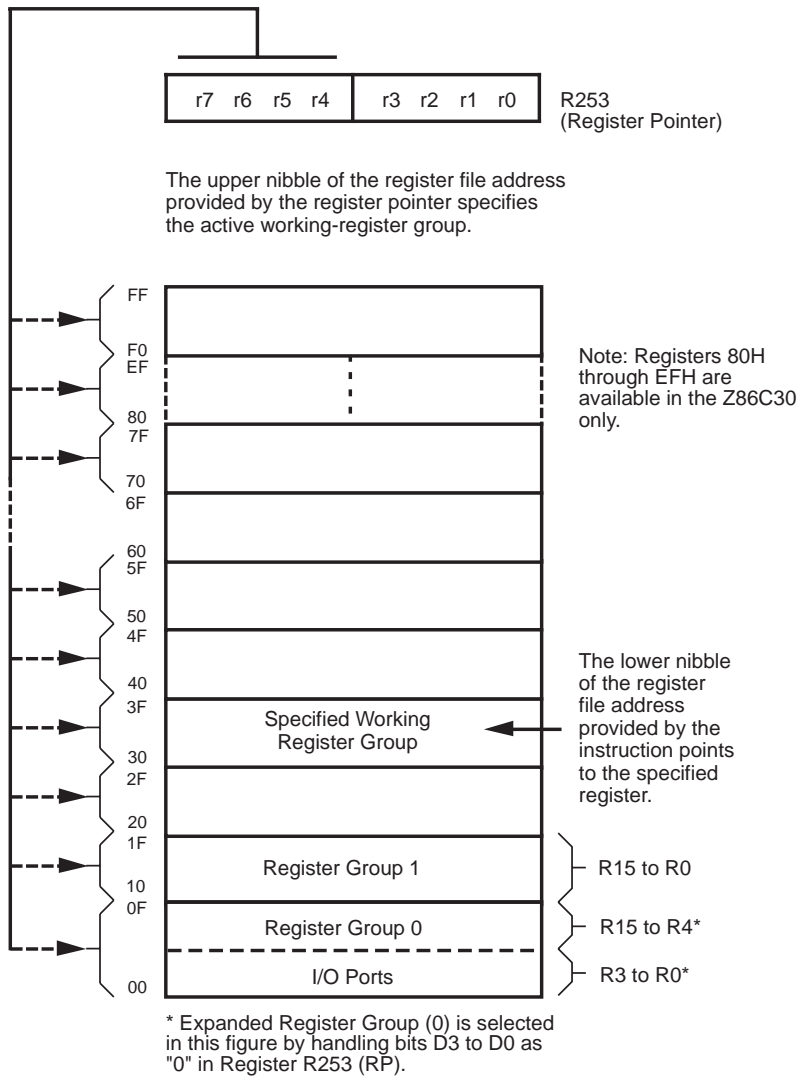


Figure 25. Register Pointer

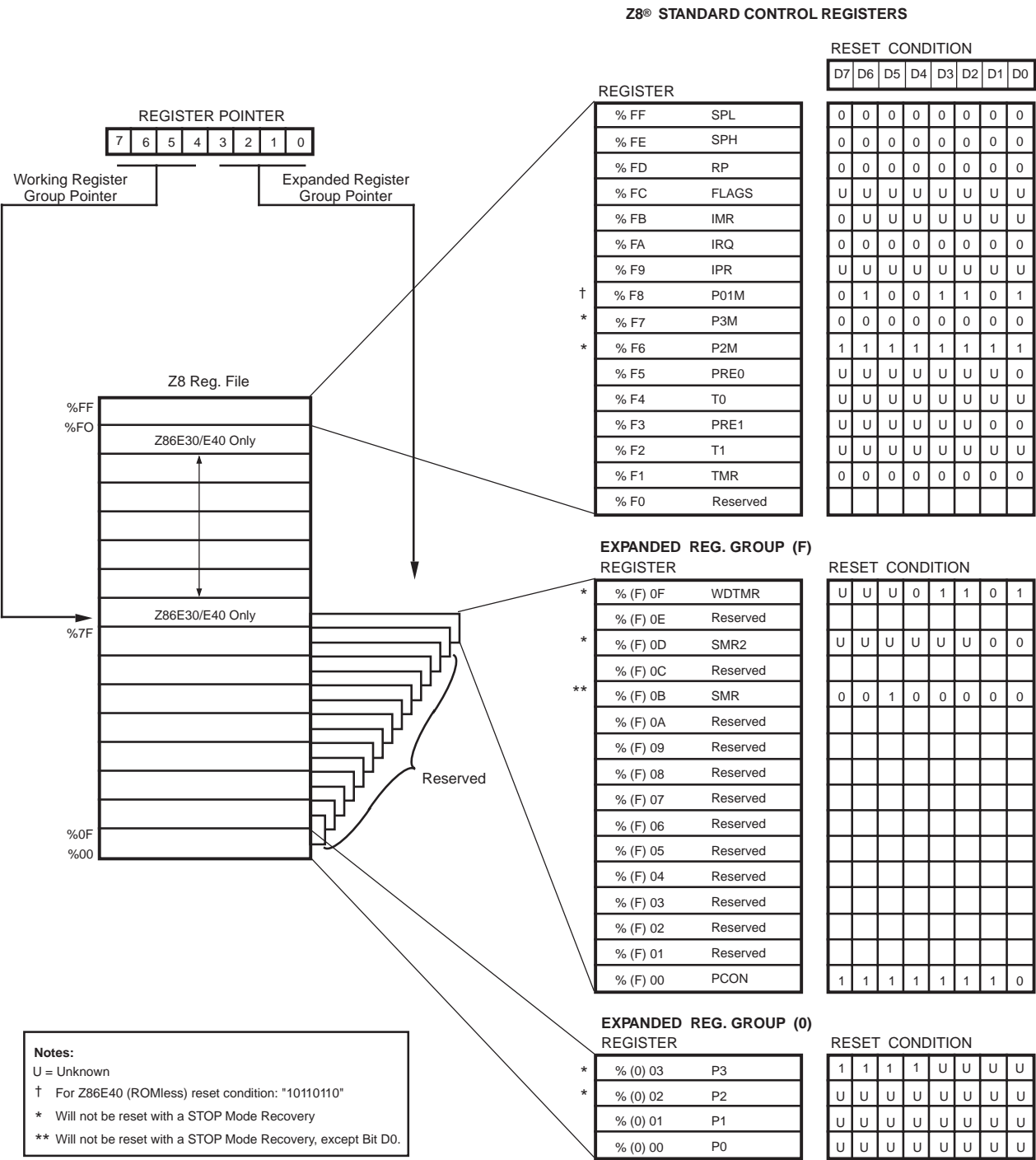


Figure 26. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. The register R254 is general-purpose on Z86E30/E31. R254 and R255 are set to 00H after any reset or STOP-Mode Recovery.

RAM Protect. The upper portion of the RAM's address spaces 80H to EFH (excluding the control registers) can be protected from reading and writing. This option can be selected during the EPROM Programming Mode. After this option is selected, the user can activate this feature from the internal EPROM. D6 of the IMR control register (R251) is used to turn off/on the RAM protect by loading a 0 or 1, respectively. A "1" in D6 indicates RAM Protect enabled. RAM Protect is not available on the Z86E31.

Stack. The Z86E40 external data memory or the internal register file can be used for the stack. The 16-bit Stack Pointer (R254–R255) is used for the external stack, which can reside anywhere in the data memory for ROMless mode, but only from 4096 to 65535 in ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack on the Z86E30/E31/E40 that resides within the 236 general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register when using internal stack only. R254 and R255 are set to 00H after any reset or Stop-Mode Recovery.

Counter/Timers. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 27).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256), that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (T_{OUT}) through which T0, T1, or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The MCU has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 28). The six sources are divided as follows: four sources are claimed by Port 3 lines P33–P30) and two

in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 10).

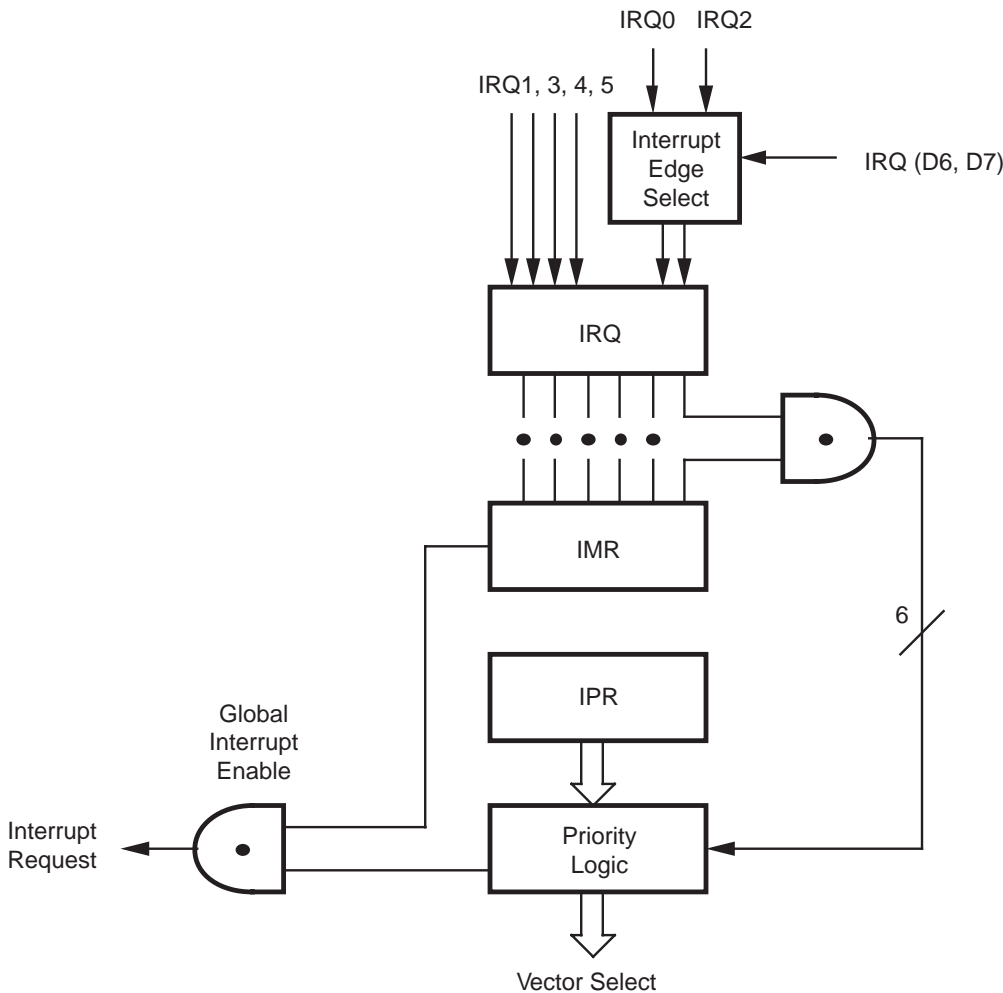


Figure 28. Interrupt Block Diagram

Table 10. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	$\overline{\text{DAV0}}$, IRQ0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	$\overline{\text{DAV2}}$, IRQ2, T_{IN}	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Falling Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

SCLK/TCLK Divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of

PCON further helps lower EMI (i.e., D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake up source of the STOP-Mode Recovery (Figure 32). Table 12 shows the SMR source selected with the setting of D2 to D4. P33–P31 cannot be used to wake up from STOP mode when programmed as analog inputs. When the STOP-Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: If the Port2 pin is configured as an output, this output level will be read by the SMR circuitry.

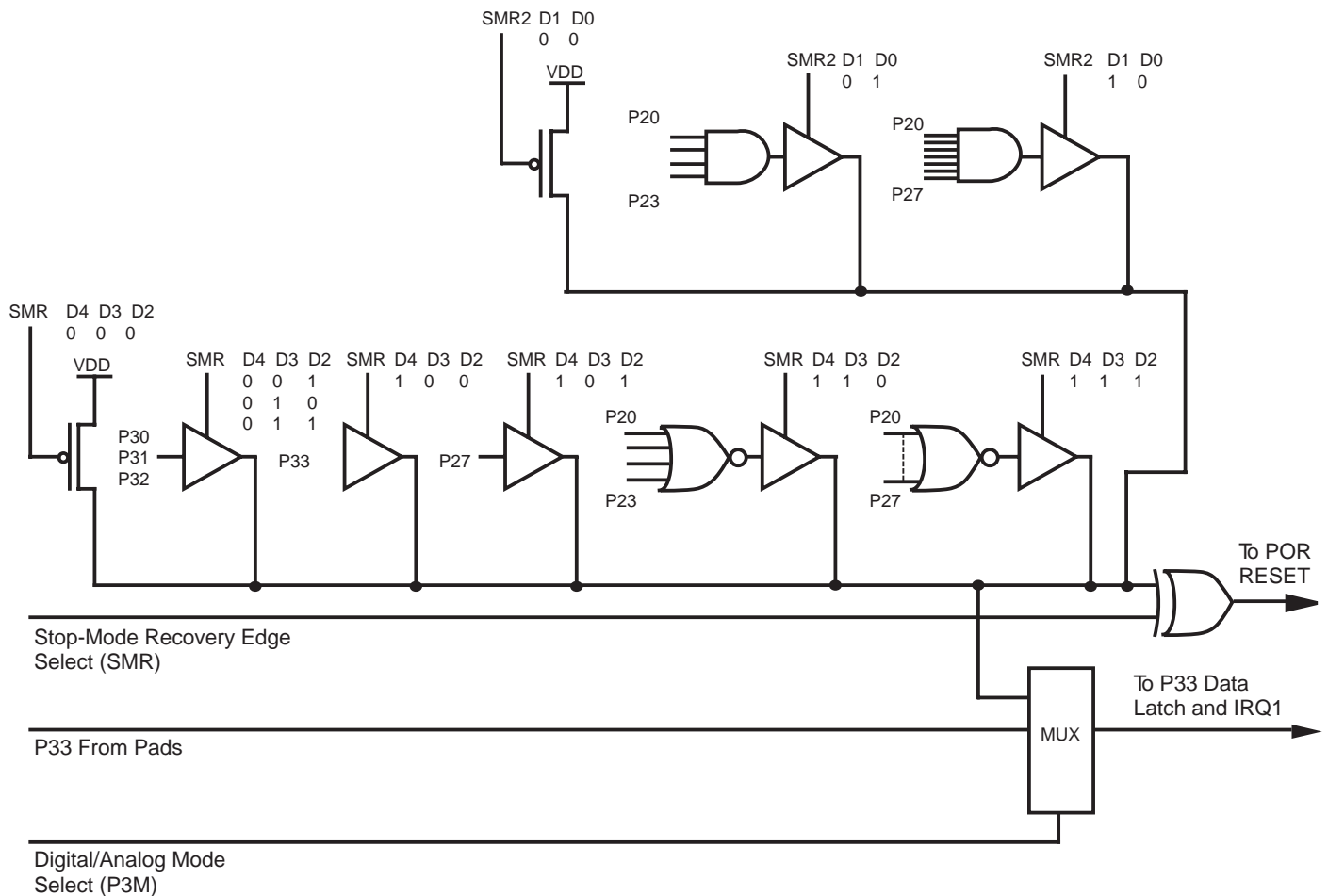


Figure 32. Stop-Mode Recovery Source

FUNCTIONAL DESCRIPTION (Continued)

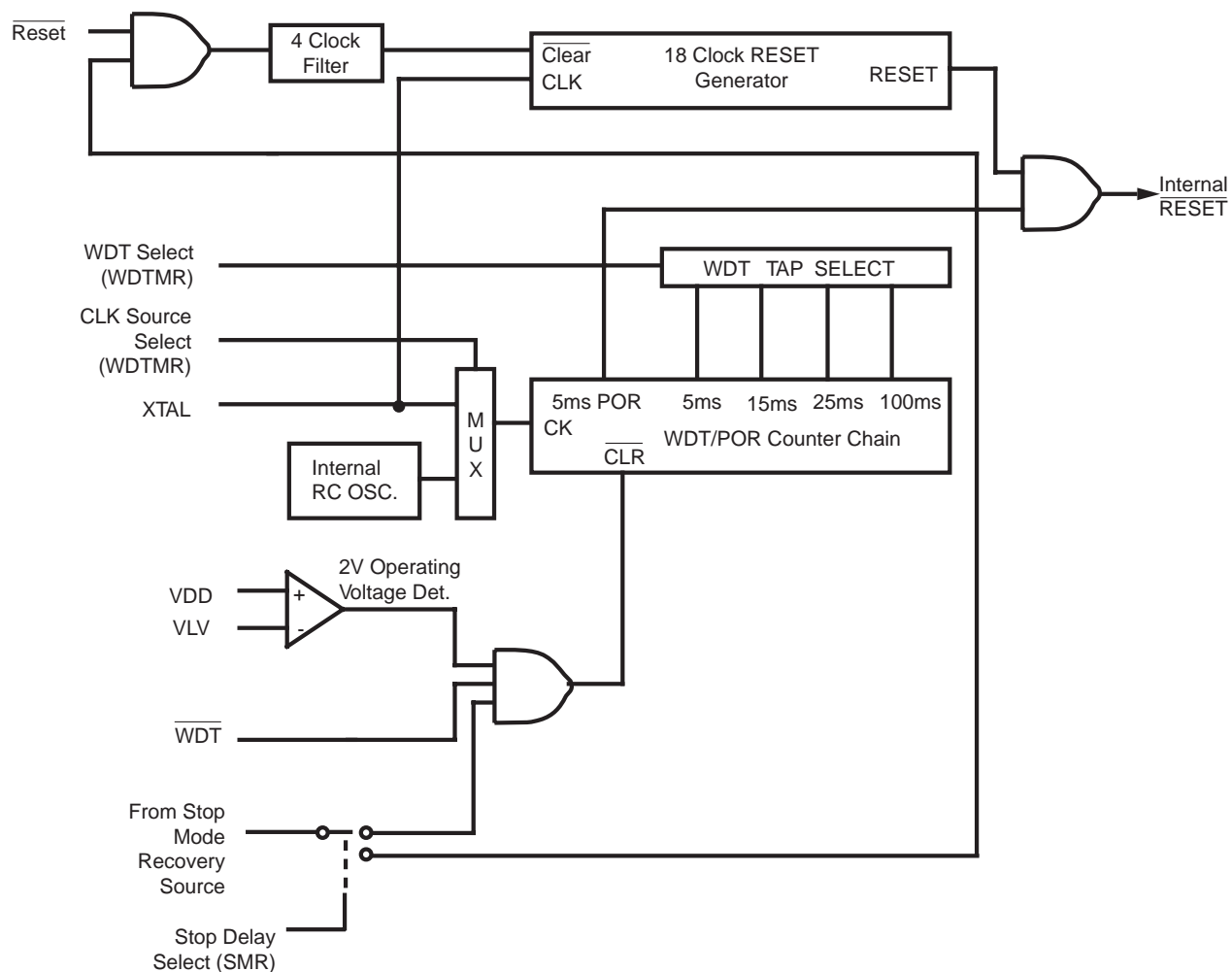


Figure 34. Resets and WDT

Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{LV} (Figure 35).

Note: V_{CC} must be in the allowed operating range prior to the minimum Power-On Reset time-out (T_{POR}).

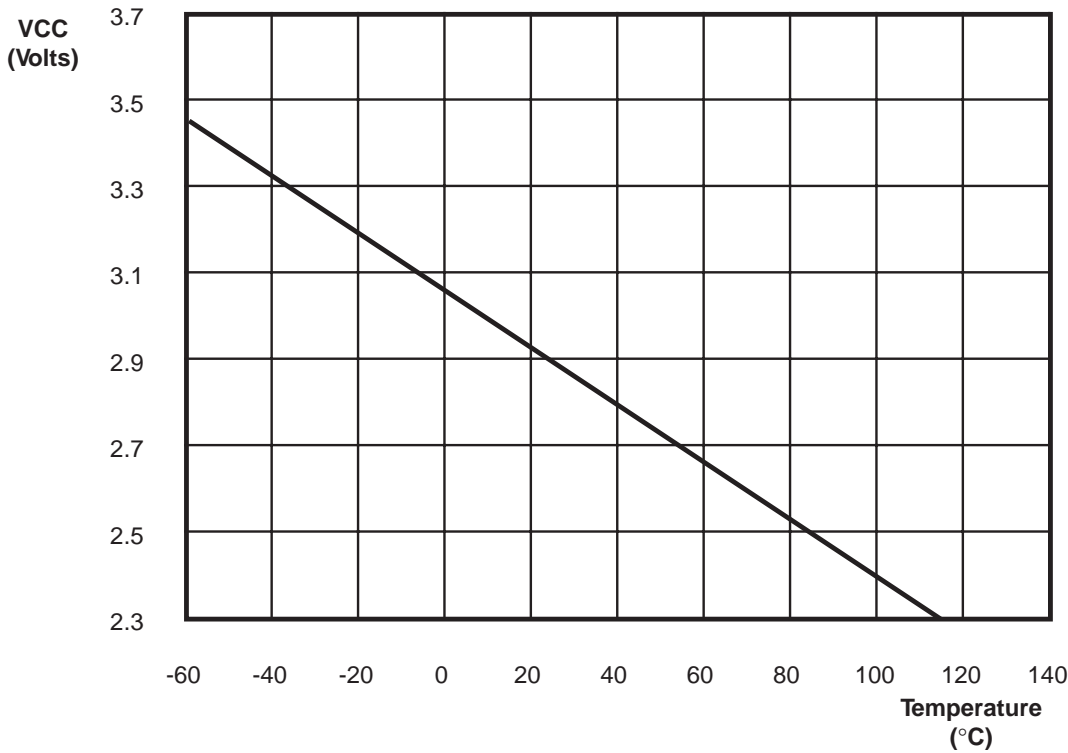


Figure 35. Typical Z86E40 V_{LV} Voltage vs. Temperature

FUNCTIONAL DESCRIPTION (Continued)

EPROM MODE

Table 14 shows the programming voltages of each programming mode. Table 15, and figures that follow show the programming timing of each programming mode. Figure 38 shows the circuit diagram of a Z86E40 programming adapter, which adapts from 2764A to Z86E40 and Figure 39 shows the Z86E30/E31 Programming Adapter Circuitry. Figure 40 shows the flowchart of an Intelligent Programming Algorithm, which is compatible with 2764A EPROM (Z86E40 is 4K EPROM, 2764A is 8K EPROM). Since the EPROM size of Z86E30/E31/E40 differs from 2764A, the programming address range has to be set from 0000H to 0FFFH for the Z86E30/E40 and 0000H to 07FFH for Z86E31. Otherwise, the upper portion of EPROM data will overwrite the lower portion of EPROM data. Figure 39 shows the adaptation from the 2764A to Z86E30/E31.

Note: EPROM Protect feature allows the LDC, LDCI, LDE, and LDEI instructions from internal program memory. A ROM lookup table can be used with this feature.

During programming, the V_{PP} input pin supplies the programming voltage and current to the EPROM. This pin is also used to latch which EPROM mode is to be used (R/W EPROM or R/W Option bits). The mode is set by placing the correct mode number on the least significant bits of the address and raising the EPM pin above V . After a setup time, the V_{PP} pin can then be raised or lowered. The latched EPROM mode will remain until the EPM pin is reduced below V_H .

Mode Name	Mode #	LSB Addr
EPROM R/W	0	0000
Option Bit R/W	3	0011

EPROM R/W mode allows the programming of the user mode program ROM.

Option Bit R/W allows the programming of the Z8 option bits. When the device is latched into Option Bit R/W mode, the address must then be changed to 63 decimals (000000111111 Binary). The Options are mapped into this address as follows:

Bit	Option
7	Unused
6	Unused
5	32 KHz XTAL Option
4	Permanent WDT
3	Auto Latch Disable
2	RC Oscillator Option
1	RAM Protect
0	ROM Protect

Table 14 gives the proper conditions for EPROM R/W operations, once the mode is latched.

Table 14. EPROM Programming Table

Programming Modes	V _{PP}	EPM	\overline{CE}	\overline{OE}	\overline{PGM}	ADDR	DATA	V _{CC} *
EPROM READ1	X	V _H	V _{IL}	V _{IL}	V _{IH}	ADDR	Out	4.5V†
EPROM READ2	X	V _H	V _{IL}	V _{IL}	V _{IH}	ADDR	Out	5.5V†
PROGRAM	V _H	V _H	V _{IL}	V _{IH}	V _{IL}	ADDR	In	6.4V
PROGRAM VERIFY	V _H	V _H	V _{IL}	V _{IL}	V _{IH}	ADDR	Out	6.0V
OPTION BIT PGM	V _H	V _H	V _{IL}	V _{IH}	V _{IL}	63	IN	6.4V
OPTION BIT READ	X	V _H	V _{IL}	V _{IL}	V _{IH}	63	OUT	6.0V

Notes:V_H = 13.0 V ± 0.1 VV_{IH} = As per specific Z8 DC specificationV_{IL} = As per specific Z8 DC specificationX=Not used, but must be set to V_H, V_{IH}, or V_{IL} level.NU = Not used, but must be set to either V_{IH} or V_{IL} level.I_{PP} during programming = 40 mA maximum.I_{CC} during programming, verify, or read = 40 mA maximum.*V_{CC} has a tolerance of ±0.25V.

† Zilog recommends an EPROM read at V_{CC} = 4.5 V and 5.5 V to ensure proper device operations during the V_{CC} after programming, but V_{CC} = 5.0 V is acceptable.

Table 15. EPROM Programming Timing

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		μs
2	Data Setup Time	2		μs
3	V _{PP} Setup	2		μs
4	V _{CC} Setup Time	2		μs
5	Chip Enable Setup Time	2		μs
6	Program Pulse Width	0.95	1.05	ms
7	Data Hold Time	2		μs
8	\overline{OE} Setup Time	2		μs
9	Data Access Time	200		ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width/Option Program Pulse Width	2.85		ms
12	EPM Setup Time	2		μs
13	\overline{PGM} Setup Time	2		μs
14	Address to \overline{OE} Setup Time	2		μs
15	\overline{OE} Width	250		ns
16	Address to \overline{OE} Low	125		ns

PACKAGE INFORMATION (Continued)

PACKAGE INFORMATION

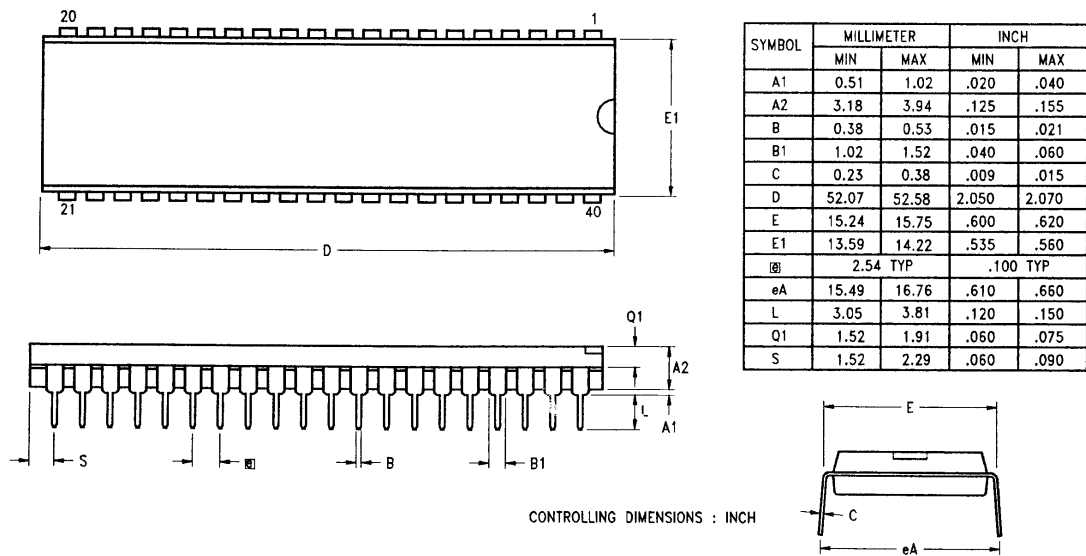


Figure 61. 40-Pin DIP Package Diagram

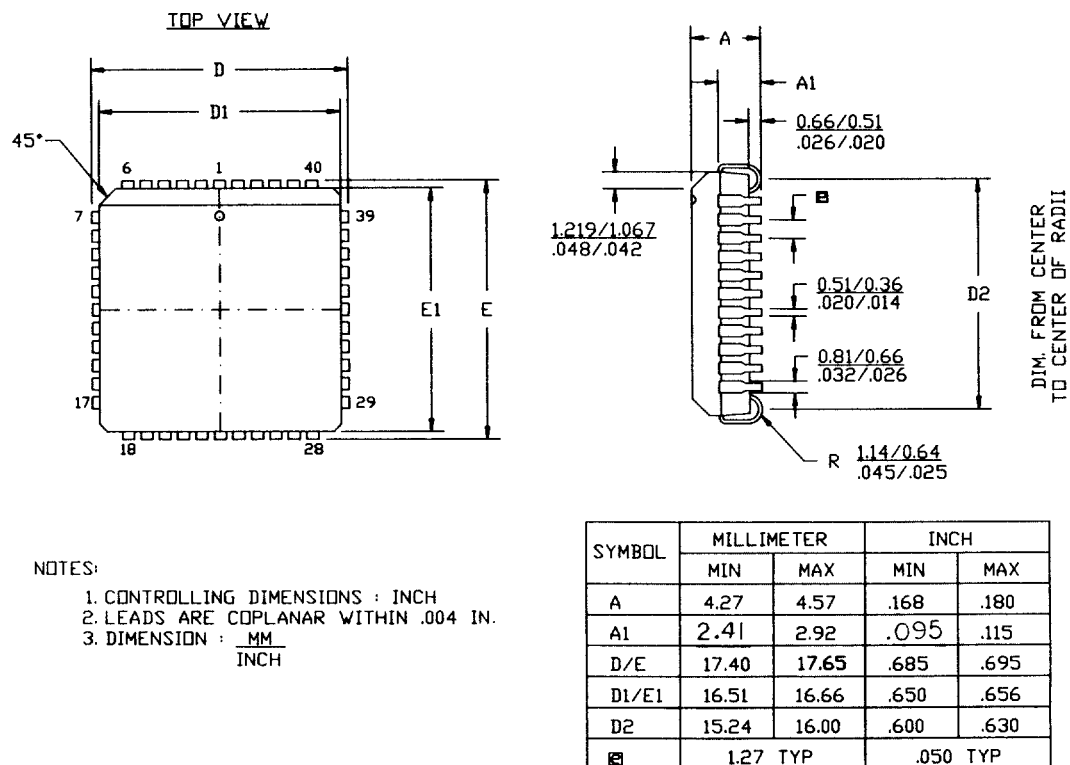


Figure 62. 44-Pin PLCC Package Diagram

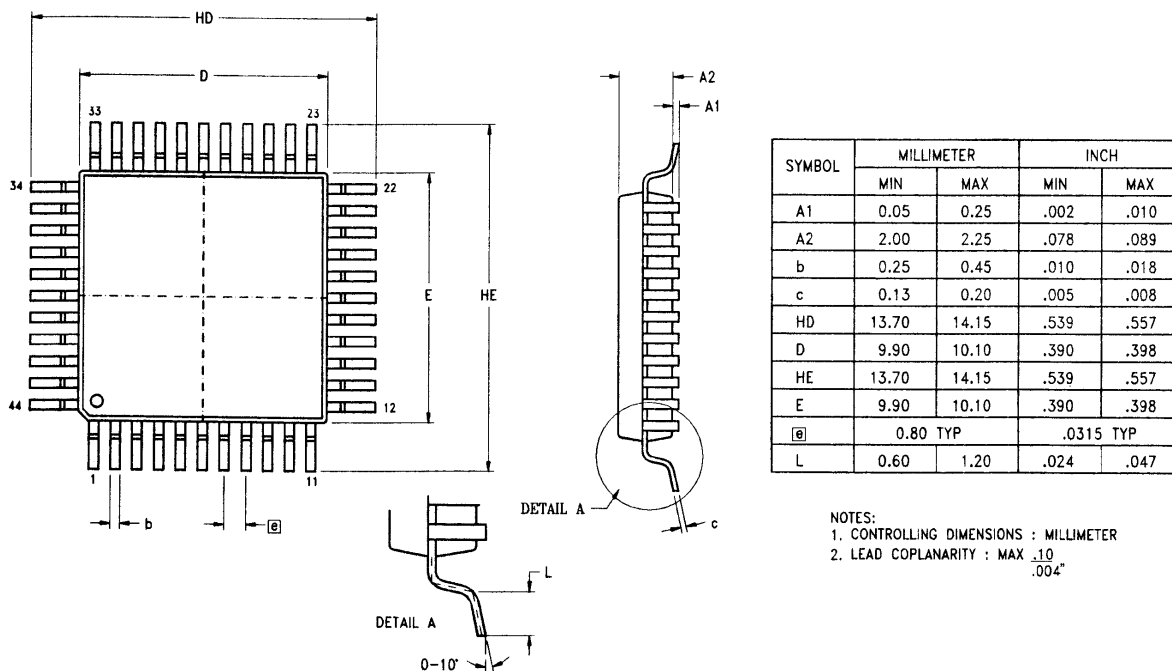


Figure 63. 44-Pin LQFP Package Diagram

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For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at <http://support.zilog.com>.