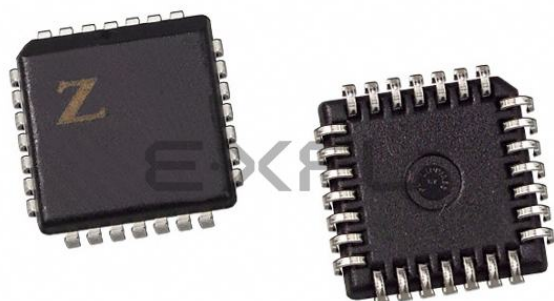




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What is "[Embedded - Microcontrollers](#)"?

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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	2KB (2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e3116veg

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

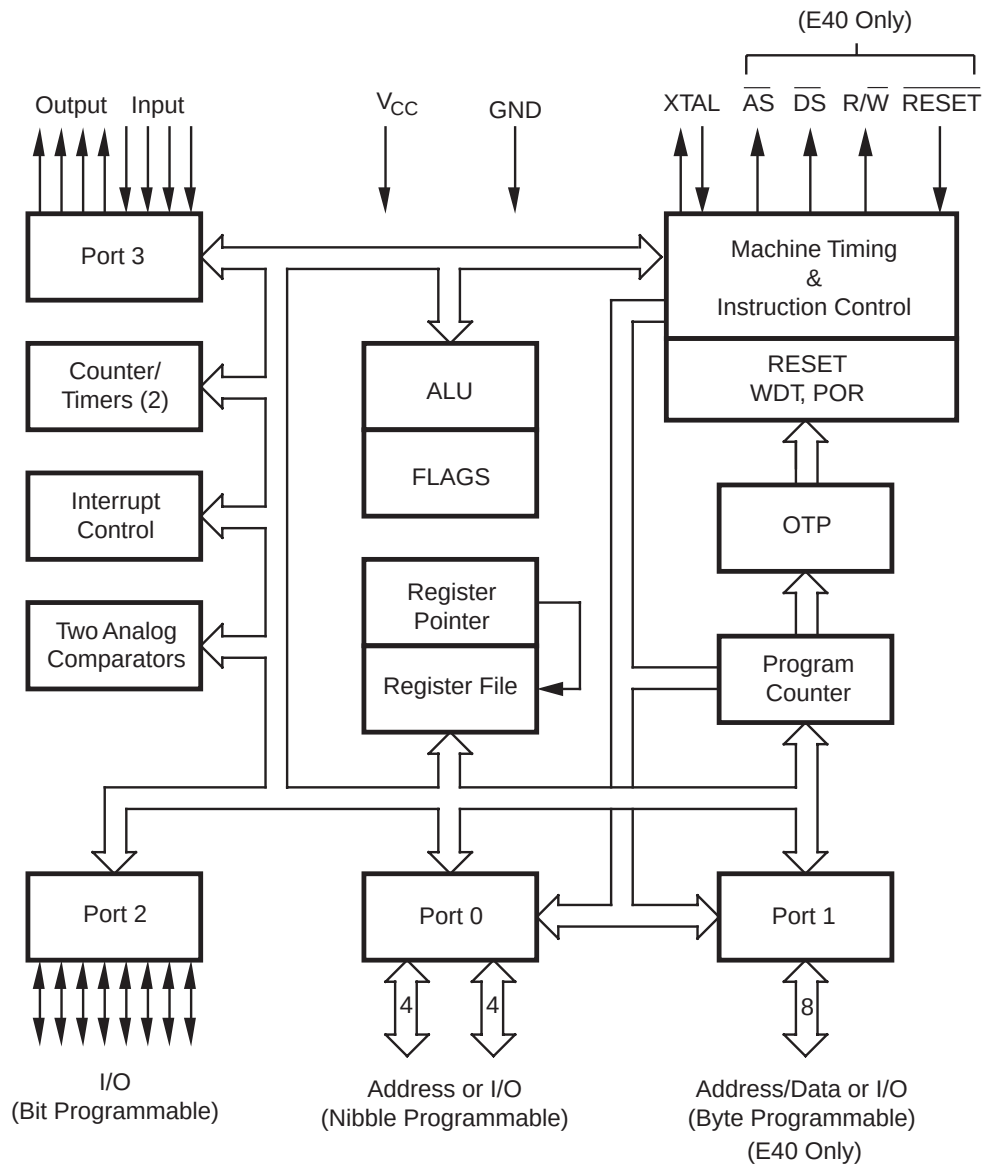


Figure 1. Z86E30/E31/E40 Functional Block Diagram

PIN IDENTIFICATION

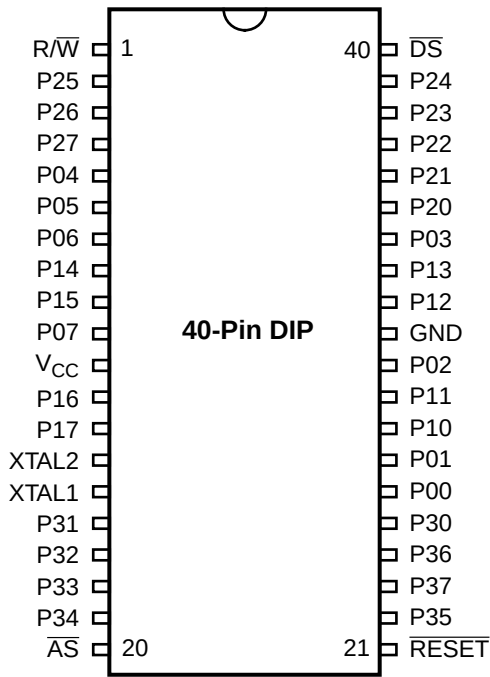


Figure 3. 40-Pin DIP Pin Configuration
Standard Mode

Table 1. 40-Pin DIP Pin Identification
Standard Mode

Pin #	Symbol	Function	Direction
1	R/W	Read/Write	Output
2–4	P25–P27	Port 2, Pins 5,6,7	In/Output
5–7	P04–P06	Port 0, Pins 4,5,6	In/Output
8–9	P14–P15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V _{CC}	Power Supply	
12–13	P16–P17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal Oscillator	Output
15	XTAL1	Crystal Oscillator	Input
16–18	P31–P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	AS	Address Strobe	Output
21	RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26–27	P00–P01	Port 0, Pins 0,1	In/Output
28–29	P10–P11	Port 1, Pins 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground	
32–33	P12–P13	Port 1, Pins 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35–39	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output
40	DS	Data Strobe	Output

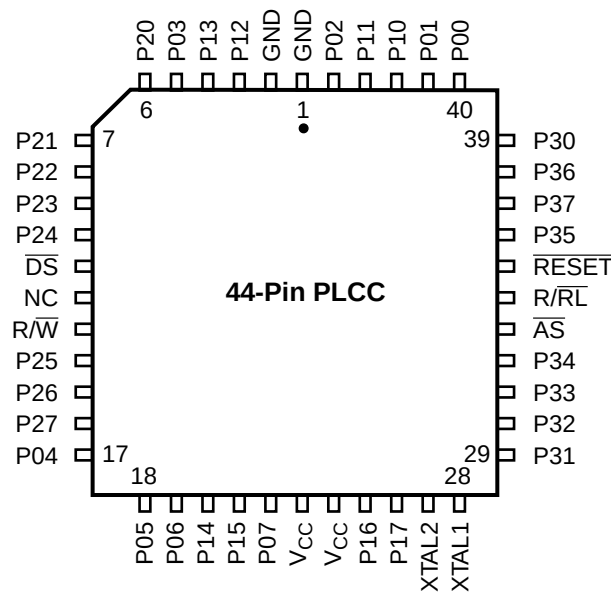


Figure 4. 44-Pin PLCC Pin Configuration
Standard Mode

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1–2	GND	Ground	
3–4	P12–P13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6–10	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output
11	$\overline{DS}$	Data Strobe	Output
12	NC	No Connection	
13	$R/\overline{W}$	Read/Write	Output
14–16	P25–P27	Port 2, Pins 5,6,7	In/Output
17–19	P04–P06	Port 0, Pins 4,5,6	In/Output
20–21	P14–P15	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23–24	V_{CC}	Power Supply	
25–26	P16–P17	Port 1, Pins 6,7	In/Output
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29–31	P31–P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
33	$\overline{AS}$	Address Strobe	Output
34	$R/\overline{RL}$	ROM/ROMless select	Input
35	$\overline{RESET}$	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40–41	P00–P01	Port 0, Pins 0,1	In/Output
42–43	P10–P11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

PIN IDENTIFICATION (Continued)

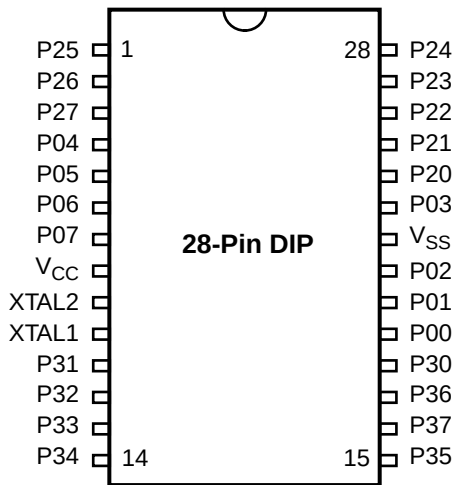


Figure 9. Standard Mode
28-Pin DIP/SOIC Pin Configuration

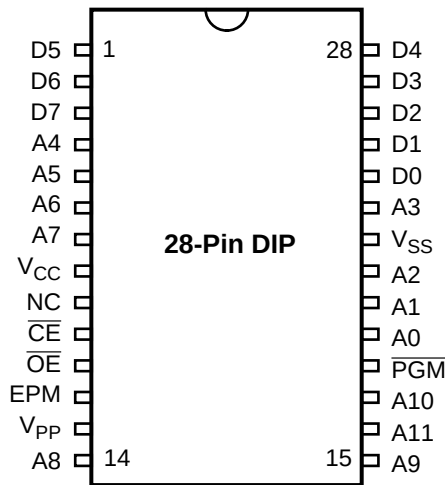


Figure 10. EPROM Programming Mode
28-Pin DIP/SOIC Pin Configuration

Table 7. 28-Pin DIP/SOIC/PLCC
Pin Identification*

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Pins 5,6,	In/Output
4–7	P04–P07	Port 0, Pins 4,5,6,7	In/Output
8	V _{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11–13	P31–P33	Port 3, Pins 1,2,3	Input
14–15	P34–P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19–21	P00–P02	Port 0, Pins 0,1,2	In/Output
22	V _{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24–28	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output

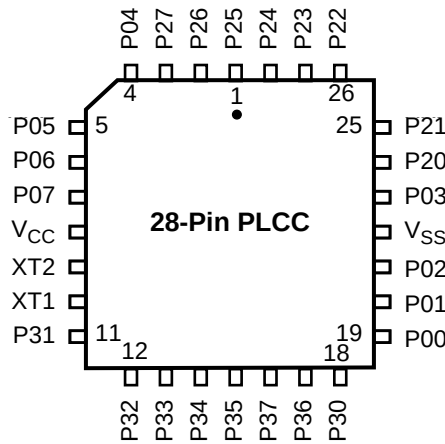


Figure 11. Standard Mode
28-Pin PLCC Pin Configuration

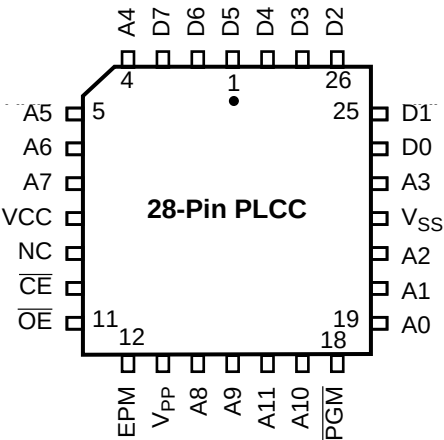


Figure 12. EPROM Programming Mode
28-Pin PLCC Pin Configuration

Table 8. 28-Pin EPROM
Pin Identification

Pin #	Symbol	Function	Direction
1–3	D5–D7	Data 5,6,7	In/Output
4–7	A4–A7	Address 4,5,6,7	Input
8	V _{CC}	Power Supply	
9	NC	No connection	
10	$\overline{\text{CE}}$	Chip Select	Input
11	$\overline{\text{OE}}$	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V _{PP}	Prog. Voltage	Input
14–15	A8–A9	Address 8,9	Input
16	A11	Address 11	Input
17	A10	Address 10	Input
18	$\overline{\text{PGM}}$	Prog. Mode	Input
19–21	A0–A2	Address 0,1,2	Input
22	V _{SS}	Ground	
23	A3	Address 3	Input
24–28	D0–D4	Data 0,1,2,3,4	In/Output

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{ MHz}$; unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

$T_A = 0^\circ\text{C to } +70^\circ\text{C}$								
Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	1.8	V	Driven by External Clock Generator	
		5.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V		
V_{CL}	Clock Input Low Voltage	3.5V	$\text{GND} - 0.3$	$0.2 V_{CC}$	0.9	V	Driven by External Clock Generator	
		4.5V	$\text{GND} - 0.3$	$0.2 V_{CC}$	1.5	V		
V_{IH}	Input High Voltage	3.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V		
		5.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V		
V_{IL}	Input Low Voltage	3.5V	$\text{GND} - 0.3$	$0.2 V_{CC}$	1.5	V		
		5.5V	$\text{GND} - 0.3$	$0.2 V_{CC}$	1.5	V		
V_{OH}	Output High Voltage Low EMI Mode	3.5V	$V_{CC} - 0.4$		3.3	V	$I_{OH} = -0.5\text{ mA}$	
		5.5V	$V_{CC} - 0.4$		4.8	V		
V_{OH1}	Output High Voltage	3.5V	$V_{CC} - 0.4$		3.3	V	$I_{OH} = -2.0\text{ mA}$ $I_{OH} = -2.0\text{ mA}$	
		5.5V	$V_{CC} - 0.4$		4.8	V		
V_{OL}	Output Low Voltage Low EMI Mode	3.5V		0.4	0.2	V	$I_{OL} = 1.0\text{ mA}$ $I_{OL} = 1.0\text{ mA}$	
		4.5V		0.4	0.2	V		
V_{OL1}	Output Low Voltage	3.5V		0.4	0.1	V	$I_{OL} = +4.0\text{ mA}$ $I_{OL} = +4.0\text{ mA}$	8
		4.5V		0.4	0.1	V		
V_{OL2}	Output Low Voltage	3.5V		1.2	0.5	V	$I_{OL} = +12\text{ mA}$ $I_{OL} = +12\text{ mA}$	8
		4.5V		1.2	0.5	V		
V_{RH}	Reset Input High Voltage	3.5V	$.8 V_{CC}$	V_{CC}	1.7	V		
		5.5V	$.8 V_{CC}$	V_{CC}	2.1	V		
V_{RL}	Reset Input Low Voltage	3.5V	$\text{GND} - 0.3$	$0.2 V_{CC}$	1.3	V		13
		5.5V	$\text{GND} - 0.3$	$0.2 V_{CC}$	1.7	V		
V_{OLR}	Reset Output Low Voltage	3.5V		0.6	0.3	V	$I_{OL} = 1.0\text{ mA}$ $I_{OL} = 1.0\text{ mA}$	
		5.5V		0.6	0.2	V		
V_{OFFSET}	Comparator Input Offset Voltage	3.5V		25	10	mV		
		4.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	3.5V	0	$V_{CC} - 1.0\text{V}$		V		10
		5.5V	0	$V_{CC} - 1.0\text{V}$		V		
I_{IL}	Input Leakage	3.5V	-1	2	0.032	μA	$V_{IN} = 0\text{V}, V_{CC}$ $V_{IN} = 0\text{V}, V_{CC}$	
		4.5V	-1	2	0.032	μA		
I_{OL}	Output Leakage	3.5V	-1	2	0.032	μA	$V_{IN} = 0\text{V}, V_{CC}$ $V_{IN} = 0\text{V}, V_{CC}$	
		4.5V	-1	2	0.032	μA		
I_{IR}	Reset Input Current	3.5V	-20	-130	-65	μA		
		4.5V	-20	-180	-112	μA		

DC ELECTRICAL CHARACTERISTICS (Continued)

				$T_A = 0^{\circ}\text{C to } 70^{\circ}\text{C}$ 16 MHz			
No	Symbol	Parameter	Note [3] V_{CC}	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	3.5V 5.5V	25 25		ns ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	3.5V 5.5V	35 35		ns ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	3.5V 5.5V		180 180	ns ns	1,2
4	TwAS	$\overline{AS}$ Low Width	3.5V 5.5V	40 40		ns ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	3.5V 5.5V	0 0		ns ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	3.5V 5.5V	135 135		ns ns	1,2
7	TwDSW	$\overline{DS}$ (Write) Low Width	3.5V 5.5V	80 80		ns ns	1,2
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid	3.5V 5.5V		75 75	ns ns	1,2
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	3.5V 5.5V	0 0		ns ns	2
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	3.5V 5.5V	50 50		ns ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	3.5V 5.5V	35 35		ns ns	2
12	TdR/W(AS)	R/ $\overline{W}$ Valid to $\overline{AS}$ Rise Delay	3.5V 5.5V	25 25		ns ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/ $\overline{W}$ Not Valid	3.5V 5.5V	35 35		ns ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	3.5V 5.5V	55 55	25 25	ns ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	3.5V 5.5V	35 35		ns ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.5V 5.5V		230 230	ns ns	1,2
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	3.5V 5.5V	45 45		ns ns	2
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Fall Delay	3.5V 5.5V	30 30		ns ns	2
20	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	3.5V 5.5V	35 35		ns ns	

Notes:

1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V $\pm 0.5V$ and the V_{CC} voltage specification of 3.5V guarantees only 3.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR D1 = 0, D0 = 0.

Additional Timing Table (Divide-By-One Mode)

				$T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$		$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$			
				4 MHz		4 MHz			
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.5V 5.5V	250 250	DC DC	250 250	DC DC	ns ns	1,7,8 1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V 5.5V		25 25		25 25	ns ns	1,7,8 1,7,8
3	TwC	Input Clock Width	3.5V 5.5V	100 100		100 100		ns ns	1,7,8 1,7,8
4	TwTinL	Timer Input Low Width	3.5V 5.5V	100 70		100 70		ns ns	1,7,8 1,7,8
5	TwTinH	Timer Input High Width	3.5V 5.5V	5TpC 5TpC		5TpC 5TpC			1,7,8 1,7,8
6	TpTin	Timer Input Period	3.5V 5.5V	8TpC 8TpC		8TpC 8TpC			1,7,8 1,7,8
7	TrTin, Tftin	Timer Input Rise & Fall Timer	3.5V 5.5V		100 100		100 100	ns ns	1,7,8 1,7,8
8A	TwIL	Int. Request Low Time	3.5V 5.5V	100 70		100 70		ns ns	1,2,7,8 1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V 5.5V	5TpC 5TpC		5TpC 5TpC			1,3,7,8 1,3,7,8
9	TwIH	Int. Request Input High Time	3.5V 5.5V	5TpC 5TpC		5TpC 5TpC			1,2,7,8 1,2,7,8
10	Twsm	STOP Mode Recovery Width Spec	3.5V 5.5V	12 12		12 12		ns ns	4,8 4,8
11	Tost	Oscillator Startup Time	3.5V 5.5V		5TpC 5TpC		5TpC		4,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31–P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 1, POR STOP Mode Delay is on.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 5.5V guarantees 5.0V $\pm$ 0.5V and the V_{CC} voltage specification of 3.5V guarantees 3.5V only.
7. SMR D1 = 0.
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

Additional Timing Table

$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$								
16 MHz								
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Units	Conditions	Notes
1	TpC	Input Clock Period	3.5V	62.5	DC	ns		1,7,8
			5.5V	62.5	DC	ns		1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15	ns		1,7,8
			5.5V		15	ns		1,7,8
3	TwC	Input Clock Width	3.5V	31		ns		1,7,8
			5.5V	31		ns		1,7,8
4	TwTinL	Timer Input Low Width	3.5V	70		ns		1,7,8
			5.5V	70		ns		1,7,8
5	TwTinH	Timer Input High Width	3.5V	5TpC				1,7,8
			5.5V	5TpC				1,7,8
6	TpTin	Timer Input Period	3.5V	8TpC				1,7,8
			5.5V	8TpC				1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100	ns		1,7,8
			5.5V		100	ns		1,7,8
8A	TwIL	Int. Request Low Time	3.5V	70		ns		1,2,7,8
			5.5V	70		ns		1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V	5TpC				1,3,7,8
			5.5V	5TpC				1,3,7,8
9	TwIH	Int. Request Input High Time	3.5V	5TpC				1,2,7,8
			5.5V					
10	Twsm	STOP Mode Recovery Width Spec	3.5V	12		ns		4,8
			5.5V	12		ns		4,8
11	Tost	Oscillator Startup Time	3.5V		5TpC			4,8
			5.5V		5TpC			4,8
12	Twdt	Watch-Dog Timer Delay Time Before Timeout	3.5V	10		ms	D0 = 0	5,11
			5.5V	5		ms	D1 = 0	5,11
			3.5V	20		ms	D0 = 1	5,11
			5.5V	10		ms	D1 = 0	5,11
			3.5V	40		ms	D0 = 0	5,11
			5.5V	20		ms	D1 = 1	5,11
			3.5V	160		ms	D0 = 1	5,11
			5.5V	80		ms	D1 = 1	5,11

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31–P33)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Reg. WDTMR
6. The V_{CC} voltage spec. of 5.5V guarantees 5.0V $\pm$ 0.5V.
7. SMR D1 = 0
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
9. For RC and LC oscillator, and for oscillator driven by clock driver.
10. Standard Mode (not Low EMI output ports)
11. Using internal RC

PIN FUNCTIONS

EPROM Programming Mode

D7–D0 Data Bus. The data can be read from or written to external memory through the data bus.

A11–A0 Address Bus. During programming, the EPROM address is written to the address bus.

V_{CC} Power Supply. This pin must supply 5V during the EPROM read mode and 6V during other modes.

$\overline{CE}$ Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

$\overline{OE}$ Output Enable (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM EPROM Program Mode. This pin controls the different EPROM Program Mode by applying different voltages.

V_{PP} Program Voltage. This pin supplies the program voltage.

$\overline{PGM}$ Program Mode (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if excessive noise surges above V_{CC} occur on pins XTAL1 and $\overline{RESET}$.

In addition, processor operation of Z8 OTP devices may be affected by excessive noise surges on the V_{PP} , $\overline{CE}$, $\overline{EPM}$, $\overline{OE}$ pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{CC}
- Adding a capacitor to the affected pin

Standard Mode

XTAL Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network, or external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network to the on-chip oscillator output.

$R/\overline{W}$ Read/Write (output, write Low). The $R/\overline{W}$ signal is Low when the CCP is writing to the external program or data memory (Z86E40 only).

$\overline{RESET}$ Reset (input, active Low). Reset will initialize the MCU. Reset is accomplished either through Power-On, Watch-Dog Timer reset, STOP-Mode Recovery, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin low for the POR time. Any devices driving the reset line must be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. After the POR time, $\overline{RESET}$ is a Schmitt-triggered input.

To avoid asynchronous and noisy reset problems, the Z86E40 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. During the reset cycle, $\overline{DS}$ is held active Low while $\overline{AS}$ cycles at a rate of TpC/2. Program execution begins at location 000CH, 5–10 TpC cycles after $\overline{RESET}$ is released. For Power-On Reset, the reset output time is 5 ms. The Z86E40 does not reset WDTMR, SMR, P2M, and P3M registers on a STOP-Mode Recovery operation.

$\overline{ROMless}$ (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90/C89 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC} , the device functions normally as a Z8 ROM version).

Note: When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC} .

FUNCTIONAL DESCRIPTION (Continued)

Data Memory ($\overline{DM}$). In EPROM Mode, the Z86E40 can address up to 60 KB of external data memory beginning at location 4096. In ROMless mode, the Z86E40 can address up to 64 KB of data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/O function that can be

programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 23). The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory.

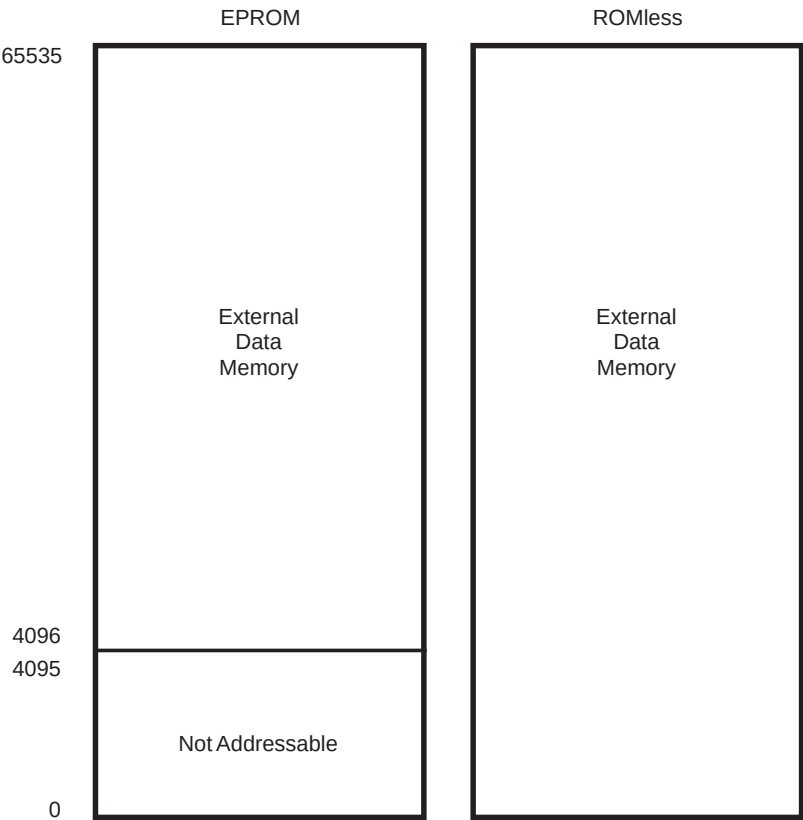


Figure 23. Data Memory Map

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The MCU has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 28). The six sources are divided as follows: four sources are claimed by Port 3 lines P33–P30) and two

in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 10).

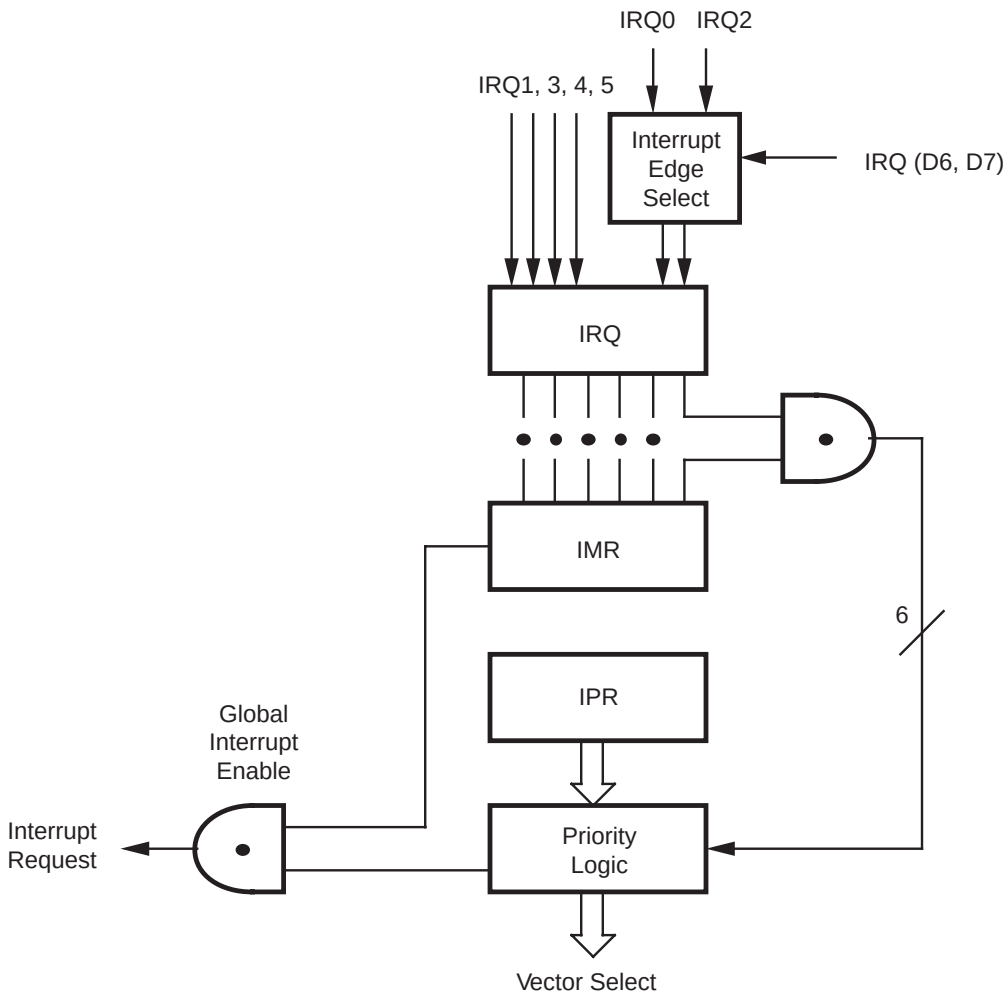


Figure 28. Interrupt Block Diagram

Table 10. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	DAV0, IRQ0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	DAV2, IRQ2, T _{IN}	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Falling Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

SCLK/TCLK Divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of

PCON further helps lower EMI (i.e., D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake up source of the STOP-Mode Recovery (Figure 32). Table 12 shows the SMR source selected with the setting of D2 to D4. P33–P31 cannot be used to wake up from STOP mode when programmed as analog inputs. When the STOP-Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: If the Port2 pin is configured as an output, this output level will be read by the SMR circuitry.

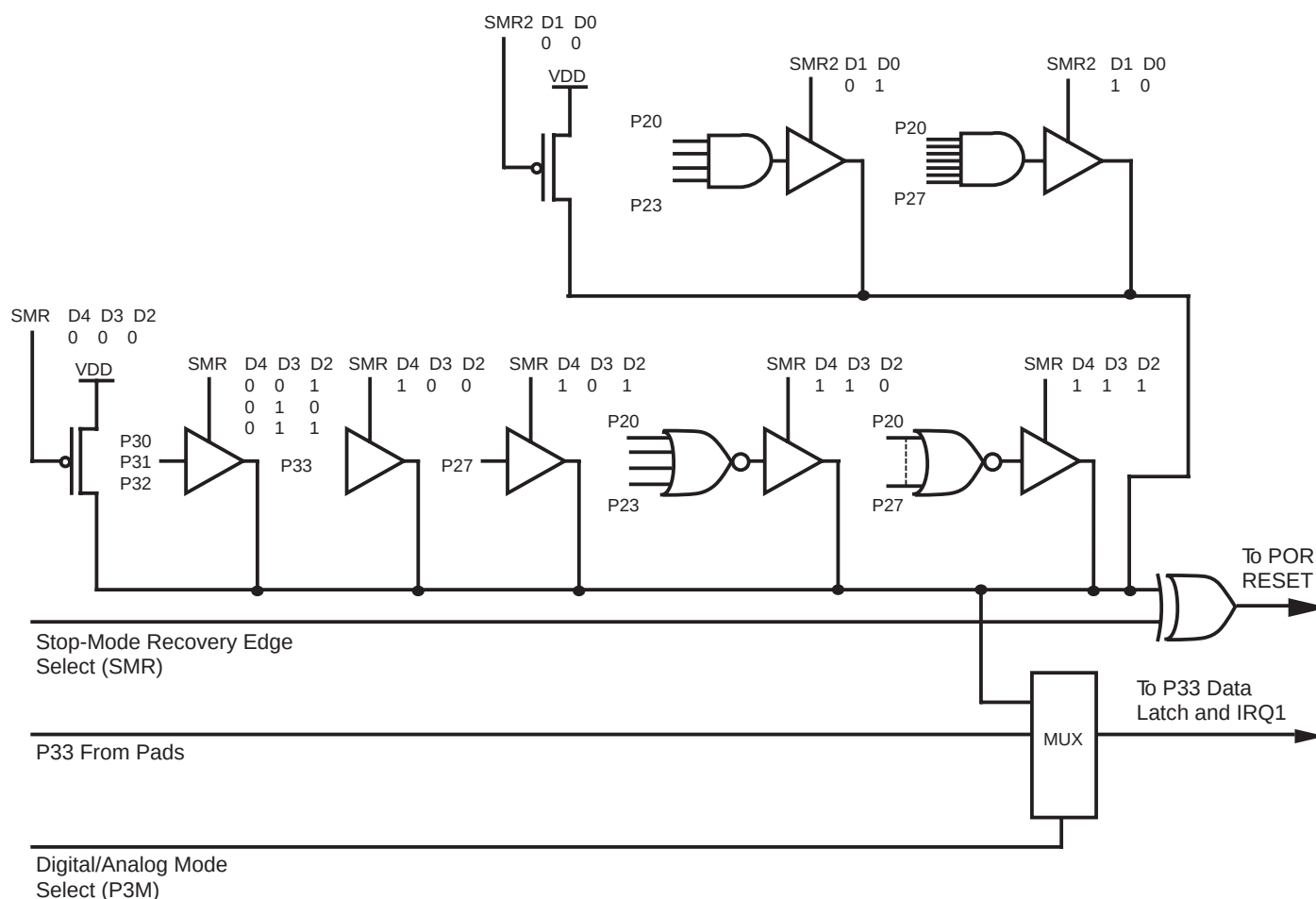


Figure 32. Stop-Mode Recovery Source

FUNCTIONAL DESCRIPTION (Continued)

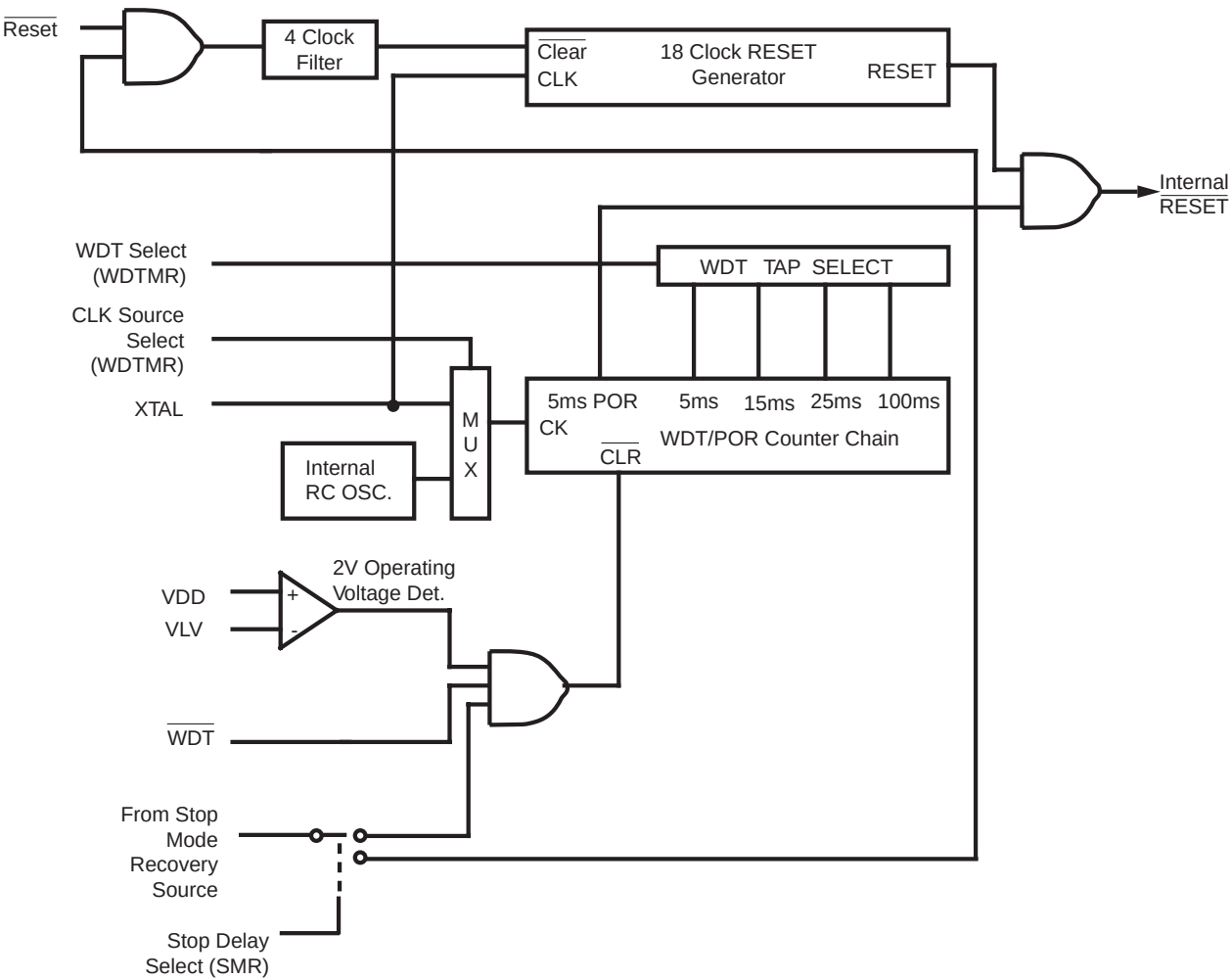


Figure 34. Resets and WDT

Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{LV} (Figure 35).

Note: V_{CC} must be in the allowed operating range prior to the minimum Power-On Reset time-out (T_{POR}).

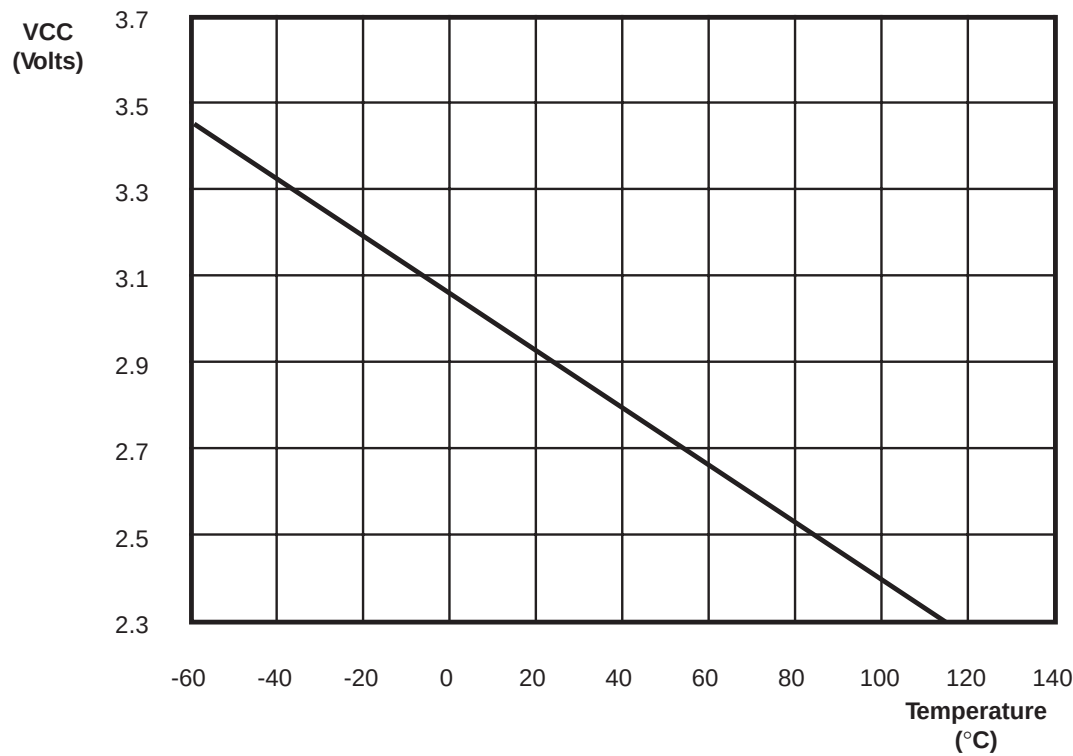


Figure 35. Typical Z86E40 V_{LV} Voltage vs. Temperature

FUNCTIONAL DESCRIPTION (Continued)

EPROM MODE

Table 14 shows the programming voltages of each programming mode. Table 15, and figures that follow show the programming timing of each programming mode. Figure 38 shows the circuit diagram of a Z86E40 programming adapter, which adapts from 2764A to Z86E40 and Figure 39 shows the Z86E30/E31 Programming Adapter Circuitry. Figure 40 shows the flowchart of an Intelligent Programming Algorithm, which is compatible with 2764A EPROM (Z86E40 is 4K EPROM, 2764A is 8K EPROM). Since the EPROM size of Z86E30/E31/E40 differs from 2764A, the programming address range has to be set from 0000H to 0FFFH for the Z86E30/E40 and 0000H to 07FFH for Z86E31. Otherwise, the upper portion of EPROM data will overwrite the lower portion of EPROM data. Figure 39 shows the adaptation from the 2764A to Z86E30/E31.

Note: EPROM Protect feature allows the LDC, LDCI, LDE, and LDEI instructions from internal program memory. A ROM lookup table can be used with this feature.

During programming, the V_{PP} input pin supplies the programming voltage and current to the EPROM. This pin is also used to latch which EPROM mode is to be used (R/W EPROM or R/W Option bits). The mode is set by placing the correct mode number on the least significant bits of the address and raising the EPM pin above V . After a setup time, the V_{PP} pin can then be raised or lowered. The latched EPROM mode will remain until the EPM pin is reduced below V_H .

Mode Name	Mode #	LSB Addr
EPROM R/W	0	0000
Option Bit R/W	3	0011

EPROM R/W mode allows the programming of the user mode program ROM.

Option Bit R/W allows the programming of the Z8 option bits. When the device is latched into Option Bit R/W mode, the address must then be changed to 63 decimals (000000111111 Binary). The Options are mapped into this address as follows:

Bit	Option
7	Unused
6	Unused
5	32 KHz XTAL Option
4	Permanent WDT
3	Auto Latch Disable
2	RC Oscillator Option
1	RAM Protect
0	ROM Protect

Table 14 gives the proper conditions for EPROM R/W operations, once the mode is latched.

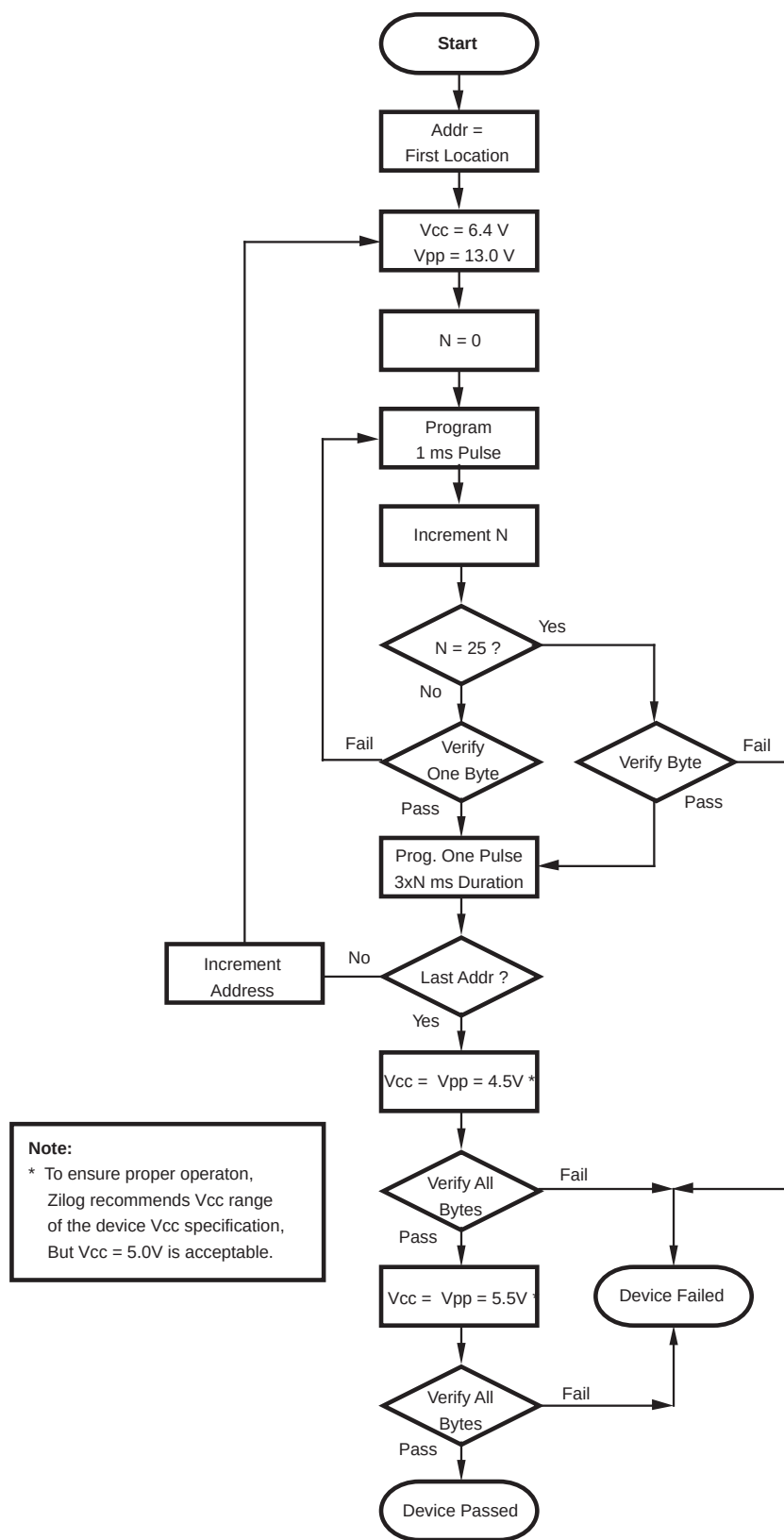


Figure 40. Z86E40 Programming Algorithm

Z8 CONTROL REGISTER DIAGRAMS

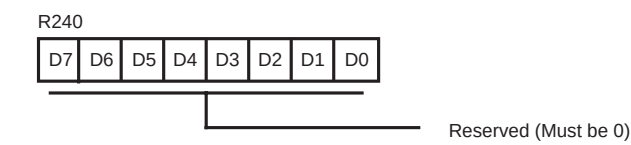


Figure 45. Reserved

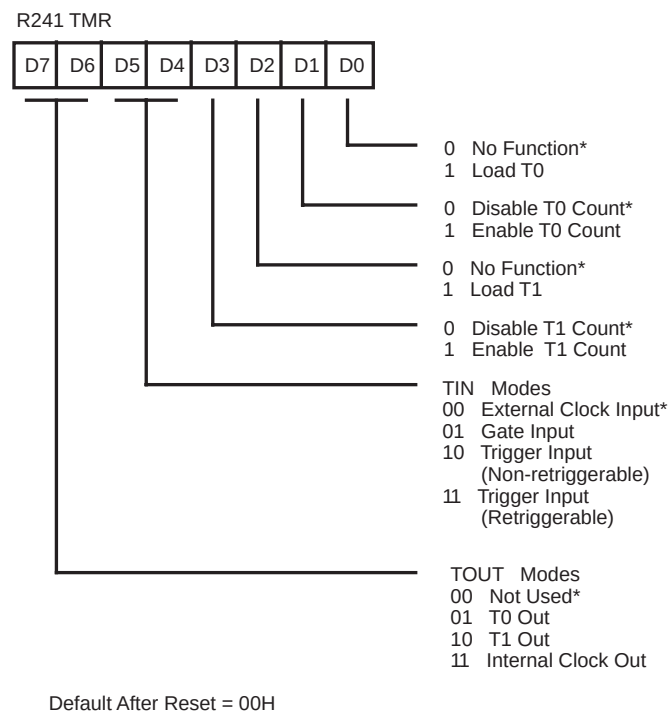


Figure 46. Timer Mode Register
F1H: Read/Write

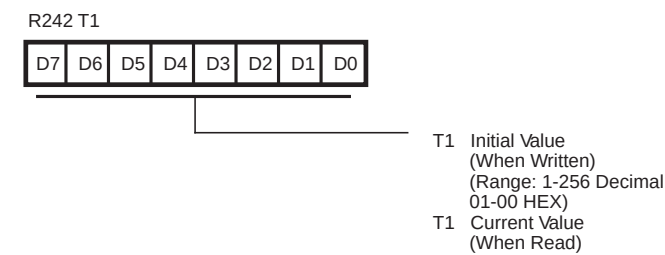


Figure 47. Counter/Timer 1 Register
F2H: Read/Write

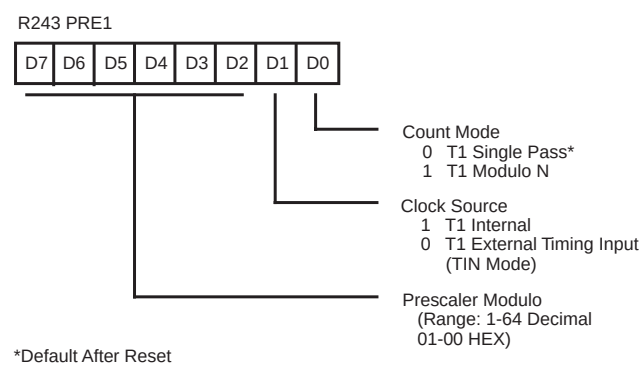


Figure 48. Prescaler 1 Register
F3H: Write Only

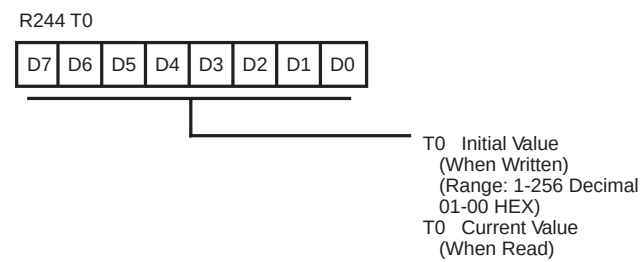


Figure 49. Counter/Timer 0 Register
F4H: Read/Write

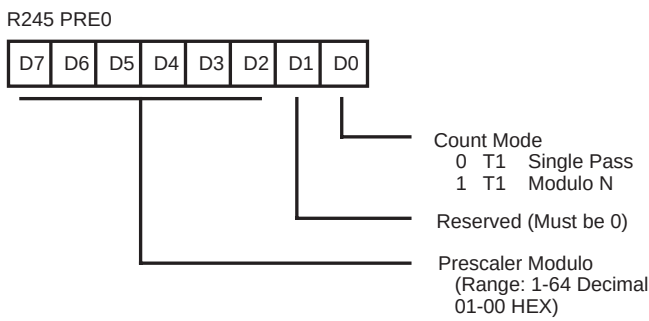


Figure 50. Prescaler 0 Register
F5H: Write Only

Z8 CONTROL REGISTER DIAGRAMS (Continued)

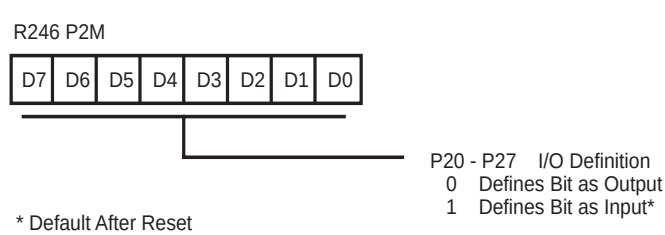


Figure 51. Port 2 Mode Register
F6H: Write Only

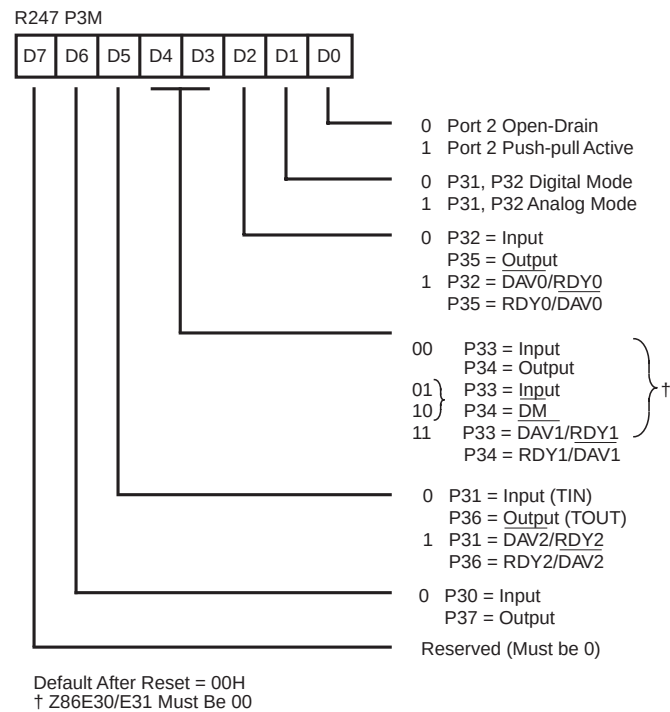


Figure 52. Port 3 Mode Register
F7H: Write Only

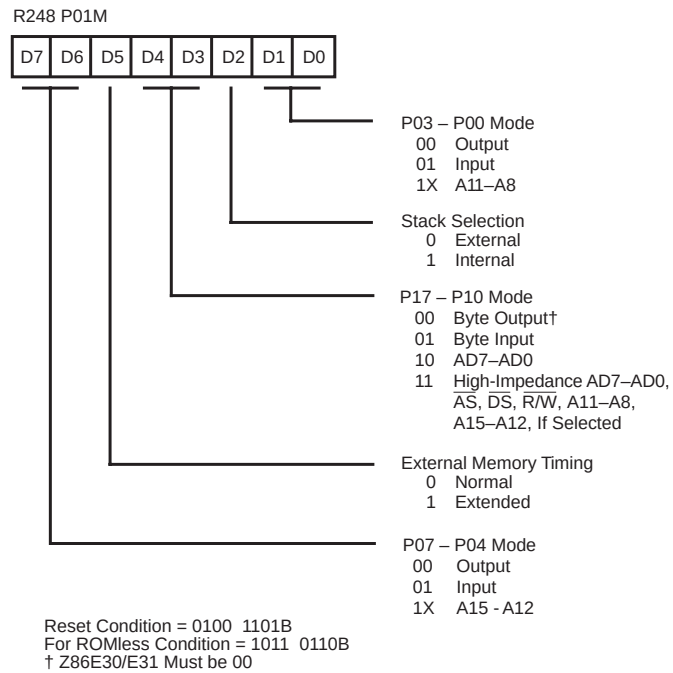


Figure 53. Port 0 and 1 Mode Register
F8H: Write Only
Z86E30/E31 Only

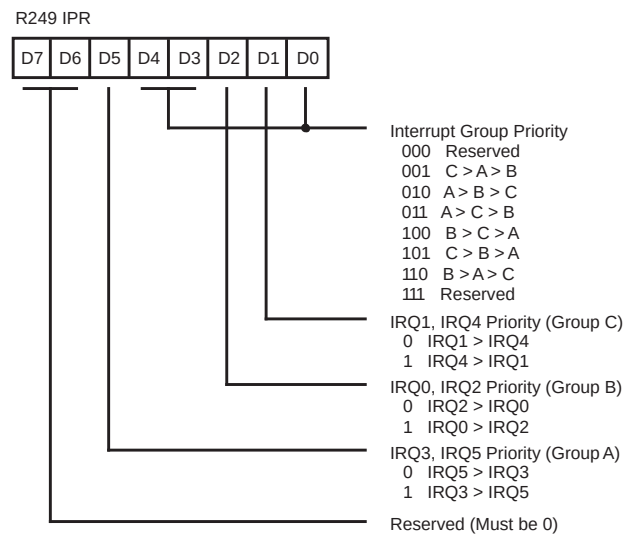


Figure 54. Interrupt Priority Register
F9H: Write Only

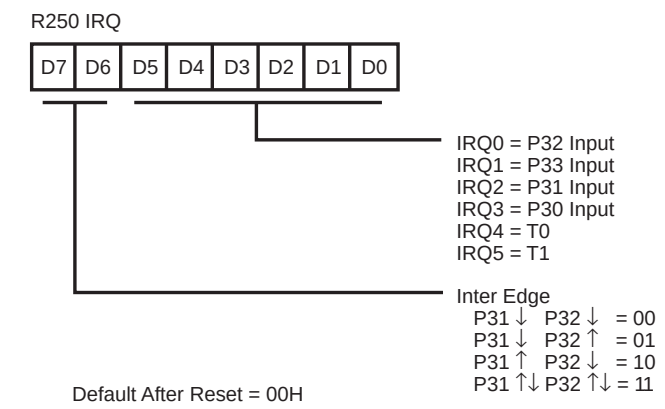


Figure 55. Interrupt Request Register
FAH: Read/Write

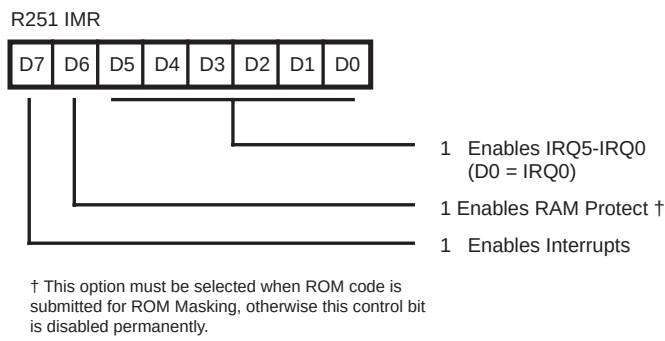


Figure 56. Interrupt Mask Register
FBH: Read/Write

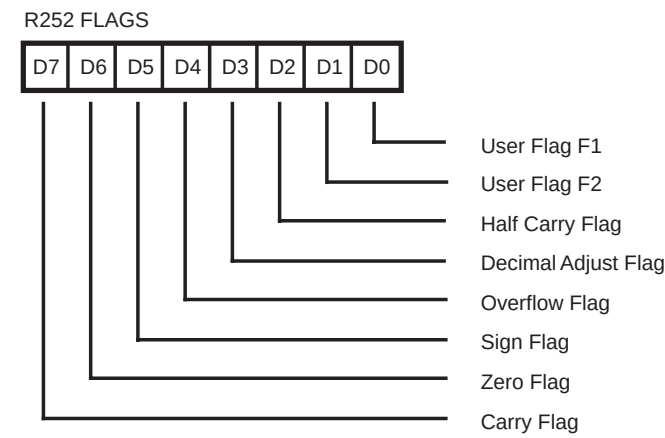


Figure 57. Flag Register
FCH: Read/Write

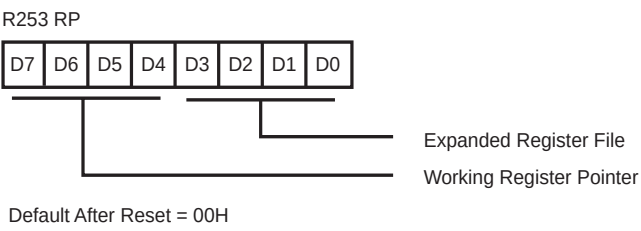


Figure 58. Register Pointer
FDH: Read/Write

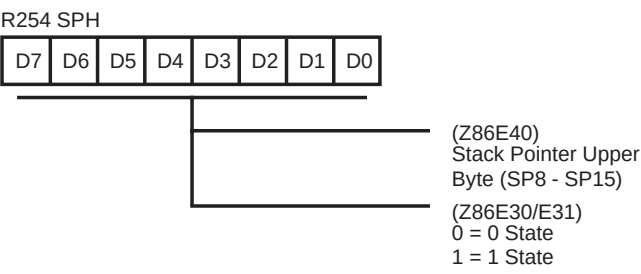


Figure 59. Stack Pointer High
FEH: Read/Write

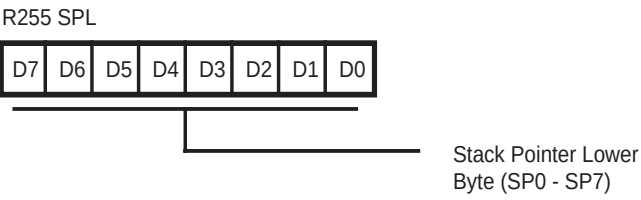


Figure 60. Stack Pointer Low
FFH: Read/Write