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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	2KB (2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e3116vsg

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

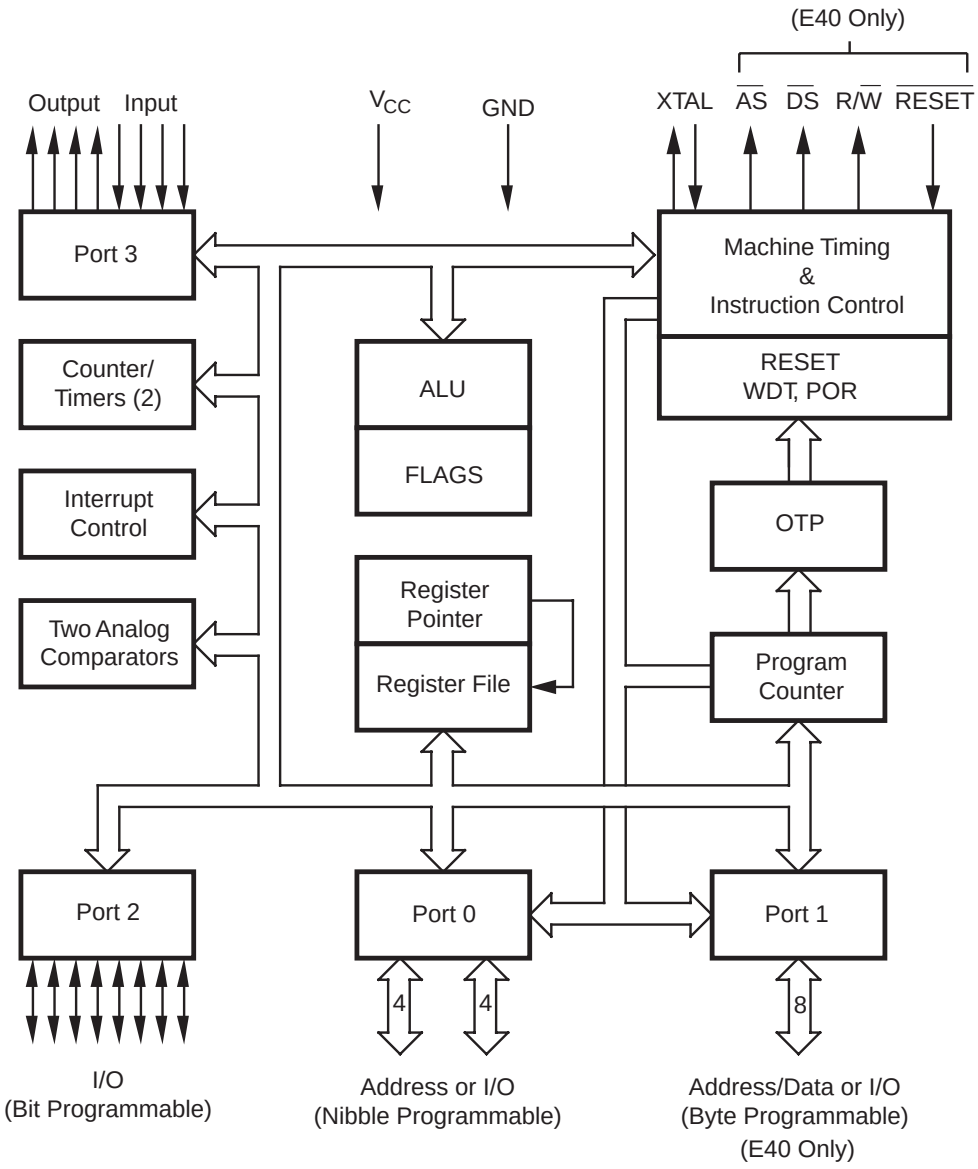


Figure 1. Z86E30/E31/E40 Functional Block Diagram

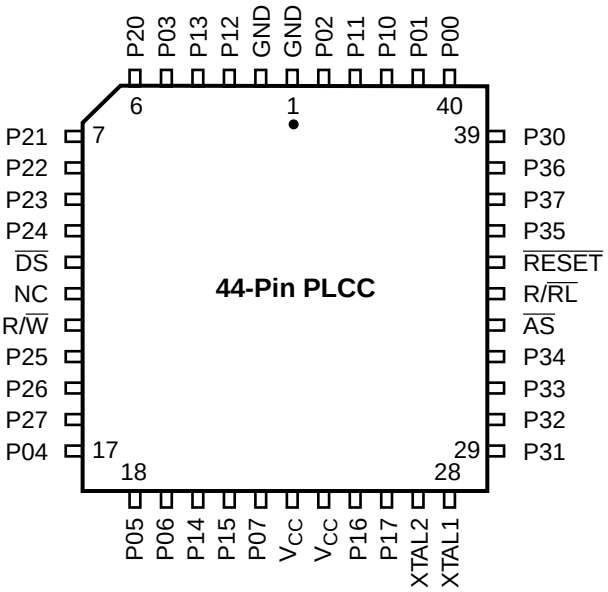


Figure 4. 44-Pin PLCC Pin Configuration
Standard Mode

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1–2	GND	Ground	
3–4	P12–P13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6–10	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output
11	$\overline{DS}$	Data Strobe	Output
12	NC	No Connection	
13	R/$\overline{W}$	Read/Write	Output
14–16	P25–P27	Port 2, Pins 5,6,7	In/Output
17–19	P04–P06	Port 0, Pins 4,5,6	In/Output
20–21	P14–P15	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23–24	V_{CC}	Power Supply	
25–26	P16–P17	Port 1, Pins 6,7	In/Output
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29–31	P31–P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
33	$\overline{AS}$	Address Strobe	Output
34	R/$\overline{RL}$	ROM/ROMless select	Input
35	$\overline{RESET}$	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40–41	P00–P01	Port 0, Pins 0,1	In/Output
42–43	P10–P11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

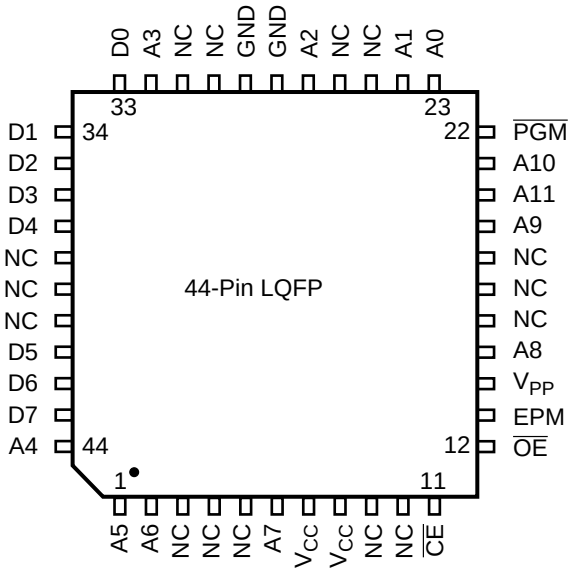


Figure 8. 44-Pin LQFP Pin Configuration EPROM Programming Mode

Table 6. 44-Pin LQFP Pin Configuration EPROM Programming Mode

Pin #	Symbol	Function	Direction
1–2	A5–A6	Address 5,6	Input
3–4	NC	No Connection	
5	A7	Address 7	Input
6–7	V_{CC}	Power Supply	
8–10	NC	No Connection	
11	$\overline{CE}$	Chip Select	Input
12	$\overline{OE}$	Output Enable	Input
13	EPM	EPROM Prog. Mode	Input
14	V_{PP}	Prog. Voltage	Input
15	A8	Address 8	Input
16–18	NC	No Connection	
19	A9	Address 9	Input
20	A11	Address 11	Input
21	A10	Address 10	Input
22	$\overline{PGM}$	Prog. Mode	Input

Table 6. 44-Pin LQFP Pin Configuration EPROM Programming Mode

Pin #	Symbol	Function	Direction
23–24	A0,A1	Address 0,1	Input
25–26	NC	No Connection	
27	A2	Address 2	Input
28–29	GND	Ground	
30–31	NC	No Connection	
32	A3	Address 3	Input
33–37	D0–D4	Data 0,1,2,3,4	In/Output
38–40	NC	No Connection	
41–43	D5–D7	Data 5,6,7	In/Output
44	A4	Address 4	Input

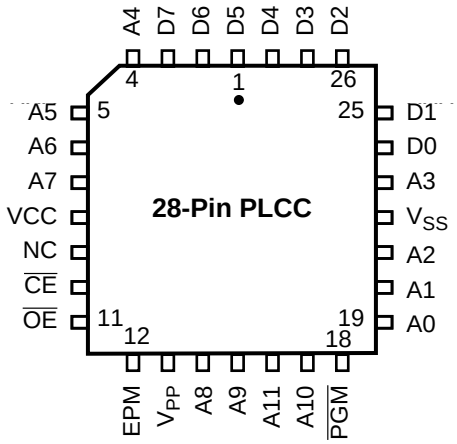


Figure 12. EPROM Programming Mode 28-Pin PLCC Pin Configuration

Table 8. 28-Pin EPROM Pin Identification

Pin #	Symbol	Function	Direction
1–3	D5–D7	Data 5,6,7	In/Output
4–7	A4–A7	Address 4,5,6,7	Input
8	V_{CC}	Power Supply	
9	NC	No connection	
10	$\overline{CE}$	Chip Select	Input
11	$\overline{OE}$	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V_{PP}	Prog. Voltage	Input
14–15	A8–A9	Address 8,9	Input
16	A11	Address 11	Input
17	A10	Address 10	Input
18	$\overline{PGM}$	Prog. Mode	Input
19–21	A0–A2	Address 0,1,2	Input
22	V_{SS}	Ground	
23	A3	Address 3	Input
24–28	D0–D4	Data 0,1,2,3,4	In/Output

DC ELECTRICAL CHARACTERISTICS (Continued)

			T_A= 0 °C to +70 °C					
Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current	3.5V		20	7	mA	@ 16 MHz	4,5
		5.5V		25	20	mA	@ 16 MHz	4,5
I_{CC1}	Standby Current Halt Mode	3.5V		8	3.7	mA	V_{IN} = 0V, V_{CC}	4,5
		5.5V		8	3.7	mA	@ 16 MHz	4,5
		3.5V		7.0	2.9	mA	Clock Divide by	4,5
		5.5V		7.0	2.9	mA	16 @ 16 MHz	4,5
I_{CC2}	Standby Current Stop Mode	3.5V		10	2	µA	V_{IN} = 0V, V_{CC}	6,11
		5.5V		10	3	µA	V_{IN} = 0V, V_{CC}	6,11
		3.5V		800	600	µA	V_{IN} = 0V, V_{CC}	6,11,14
		5.5V		800	600	µA	V_{IN} = 0V, V_{CC}	6,11,14
I_{ALL}	Auto Latch Low Current	3.5V	0.7	8	2.4	µA	0V <V_{IN}<V_{CC}	9
		5.5V	1.4	15	4.7	µA	0V <V_{IN}<V_{CC}	9
I_{ALH}	Auto Latch High Current	3.5V	-0.6	-5	-1.8	µA	0V<V_{IN}<V_{CC}	9
		5.5V	-1	-8	-3.8	µA	0V<V_{IN}<V_{CC}	9
T_{POR}	Power On Reset	3.5V	3.0	24	7	ms		
		5.5V	2.0	13	4	ms		
V_{LV}	Auto Reset Voltage		2.3	3.1	2.9	V		1,7

Notes:

1. Device does function down to the Auto Reset voltage.
2. GND=0V
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1= CL2 = 22 pF
6. Same as note [4] except inputs at $V_{CC.}$
7. Max. temperature is 70°C.
8. STD Mode (not Low EMI Mode)
9. Auto Latch (mask option) selected
10. For analog comparator inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.
12. Typicals are at V_{CC} = 5.0V and V_{CC} = 3.5V
13. Z86E40 only
14. WDT running

			T_A = -40°C to 105°C 16 MHz Note [3]				
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	4.5V 5.5V	25 25		ns ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	4.5V 5.5V	35 35		ns ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	4.5V 5.5V		180 180	ns ns	1,2
4	TwAS	$\overline{AS}$ Low Width	4.5V 5.5V	40 40		ns ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	4.5V 5.5V	0 0		ns ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	4.5V 5.5V	135 135		ns ns	1,2
7	TwDSW	$\overline{DS}$ (Write) Low Width	4.5V 5.5V	80 80		ns ns	1,2
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid	4.5V 5.5V		75 75	ns ns	1,2
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	4.5V 5.5V	0 0		ns ns	2
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	4.5V 5.5V	50 50		ns ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	4.5V 5.5V	35 35		ns ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	4.5V 5.5V	25 25		ns ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	4.5V 5.5V	35 35		ns ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	4.5V 5.5V	55 55	25 25	ns ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	4.5V 5.5V	35 35		ns ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	4.5V 5.5V		230 230	ns ns	1,2
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	4.5V 5.5V	45 45		ns ns	2
18	TdDM(AS)	/DM Valid to $\overline{AS}$ Fall Delay	4.5V 5.5V	30 30		ns ns	2
20	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	4.5V 5.5V	35 35		ns ns	

Notes:

1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

DC ELECTRICAL CHARACTERISTICS (Continued)

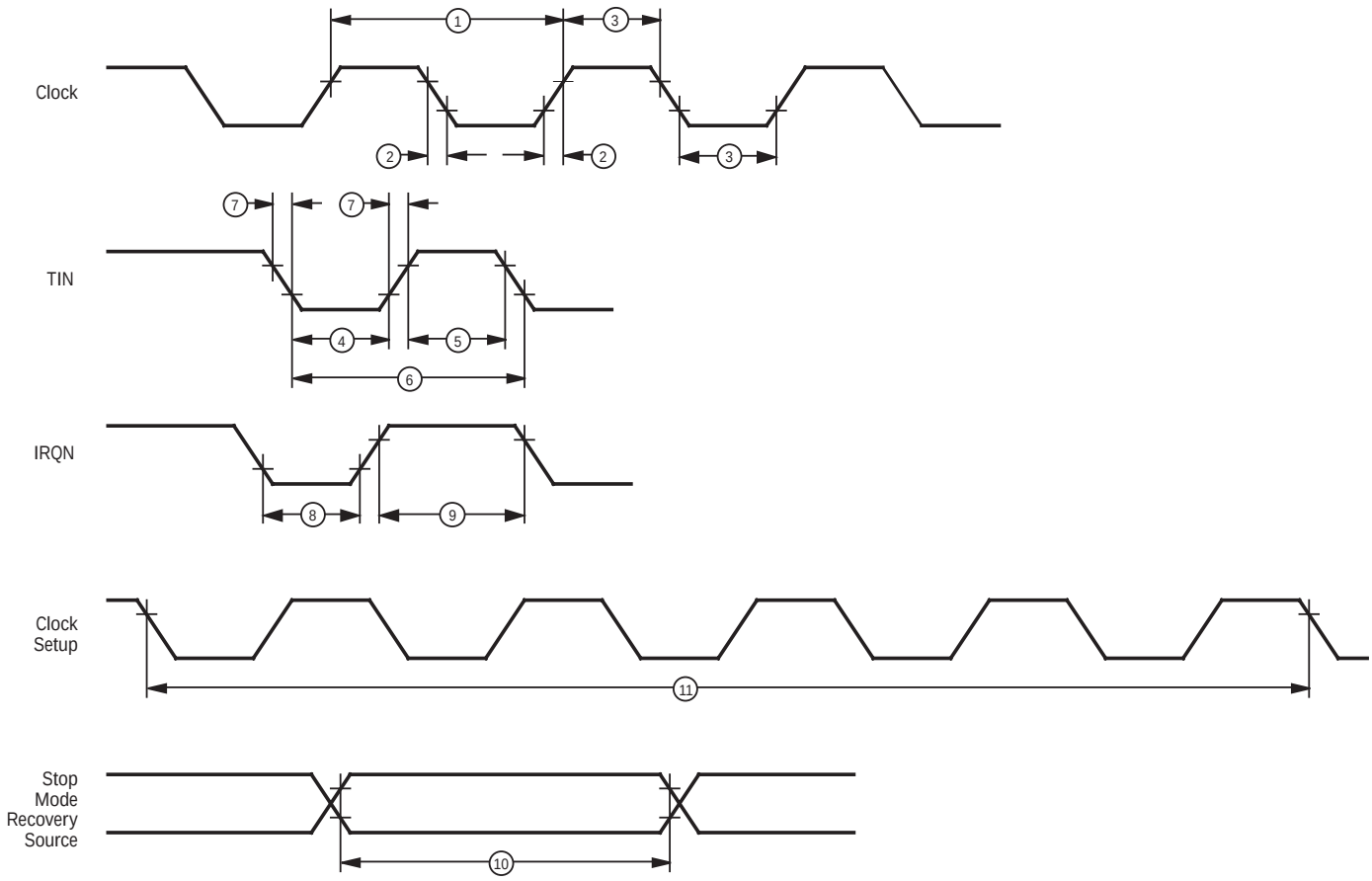


Figure 15. Additional Timing Diagram

DC ELECTRICAL CHARACTERISTICS (Continued)

Handshake Timing Diagrams

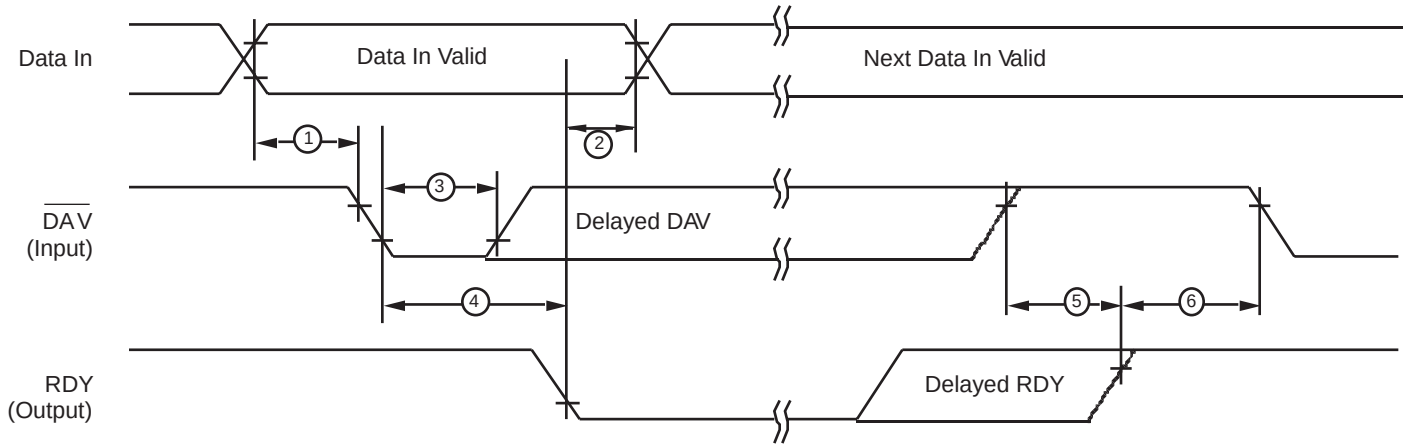


Figure 16. Input Handshake Timing

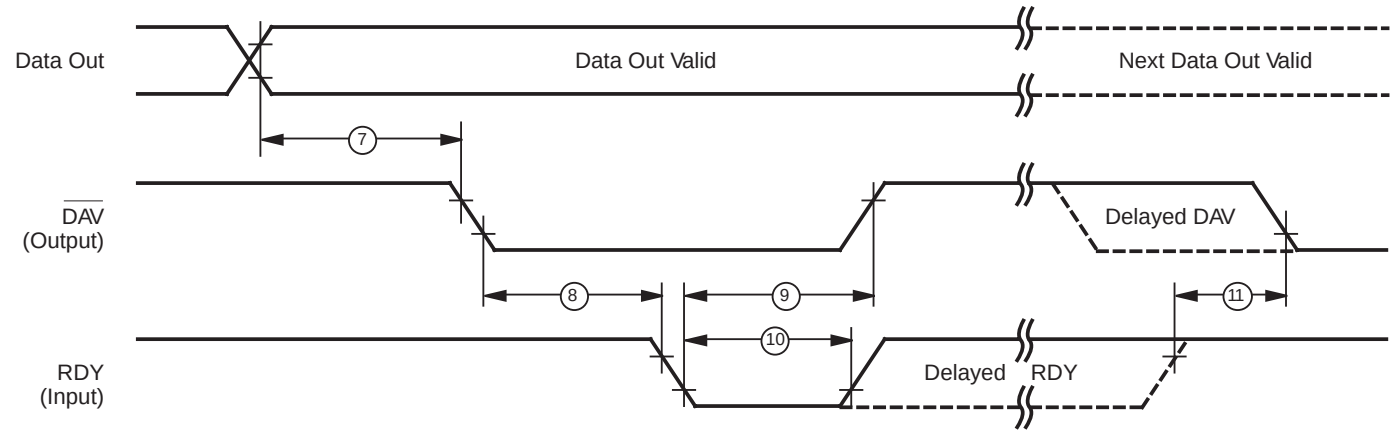


Figure 17. Output Handshake Timing

PIN FUNCTIONS (Continued)

Port 1 (P17–P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7–A0) and Data (D7–D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and /DAV1 (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (Figure 19).

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z86E40 to share common resources in multiprocessor and DMA applications.

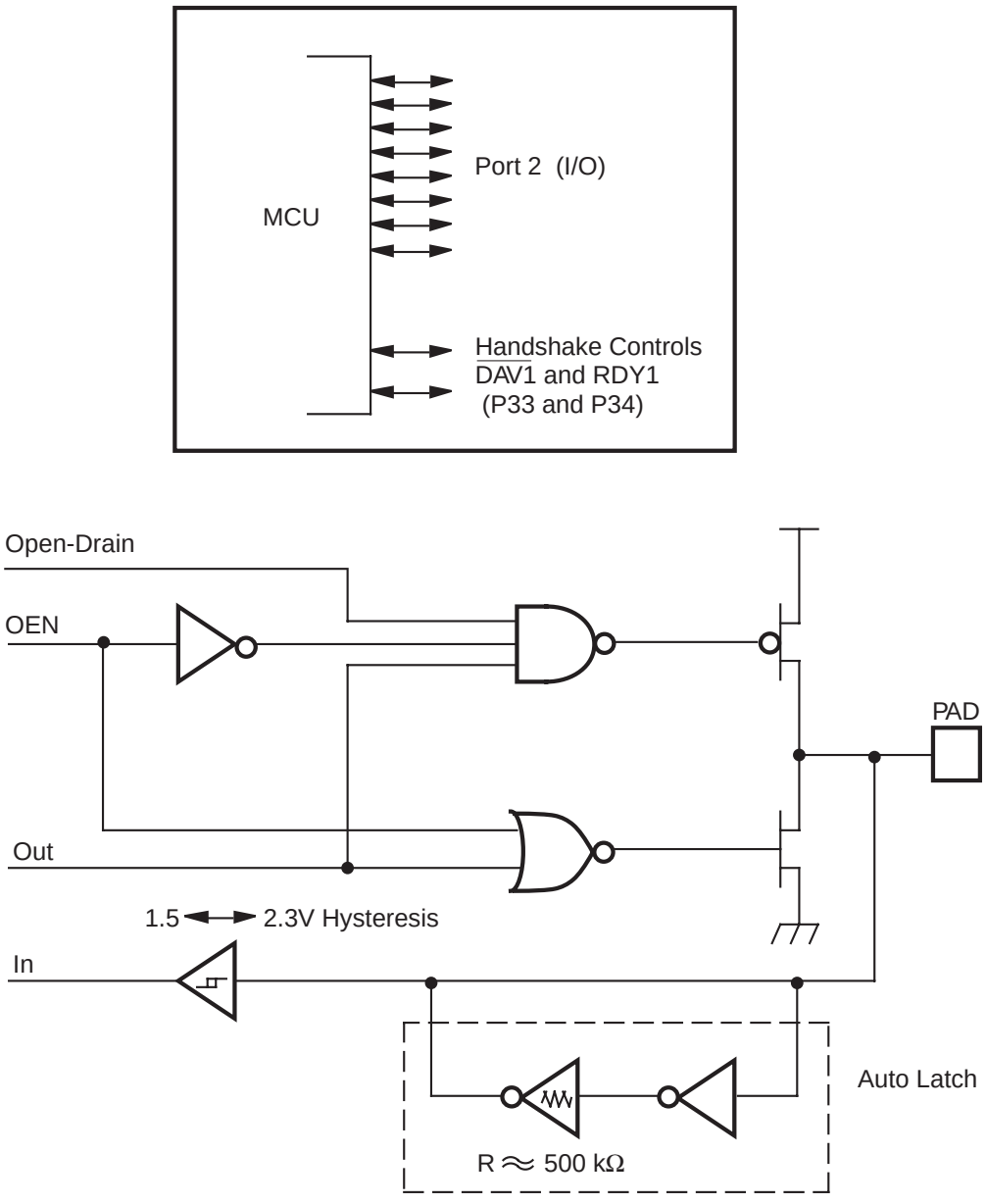


Figure 19. Port 1 Configuration (Z86E40 Only)

PIN FUNCTIONS (Continued)

Comparator Inputs. Port 3, P31, and P32, each have a comparator front end. The comparator reference voltage P33 is common to both comparators. In analog mode, P31 and P32 are the positive input of the comparators and P33 is the reference voltage of the comparators.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33–P31) that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Auto Latches are available on Port 0, Port 2, and P30. There are no Auto Latches on P31, P32, and P33.

Low EMI Emission. The Z86E40 can be programmed to operate in a low EMI Emission Mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Low EMI Oscillator.
- Internal SCLK/TCLK= XTAL operation limited to a maximum of 4 MHz – 250 ns cycle time, when Low EMI Oscillator is selected and system clock (SCLK = XTAL, SMR Reg. Bit D1 =1).
- **Note for emulation only:**
  Do not set the emulator to emulate Port 1 in low EMI mode. Port 1 must always be configured in Standard Mode.

FUNCTIONAL DESCRIPTION

The MCU incorporates the following special functions to enhance the standard Z8 architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of three ways:

1. Power-On Reset
2. Watch-Dog Timer
3. STOP-Mode Recovery Source

Note: Having the Auto Power-On Reset circuitry built-in, the MCU does not need to be connected to an external power-on reset circuit. The reset time is 5 ms (typical). The MCU does not reinitialize WDTMR, SMR, P2M, and P3M registers to their reset values on a STOP-Mode Recovery operation.

Note: The device V_{CC} must rise up to the operating V_{CC} specification before the TPOR expires.

Program Memory. The MCU can address up to 4 KB of Internal Program Memory (Figure 22). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 12 (000CH) to address 4095 (0FFFH) consists of programmable EPROM. After reset, the program counter points at the address 000CH, which is the starting address of the user program.

In ROMless mode, the Z86E40 can address up to 64 KB of External Program Memory. The ROM/ROMless option is only available on the 44-pin devices.

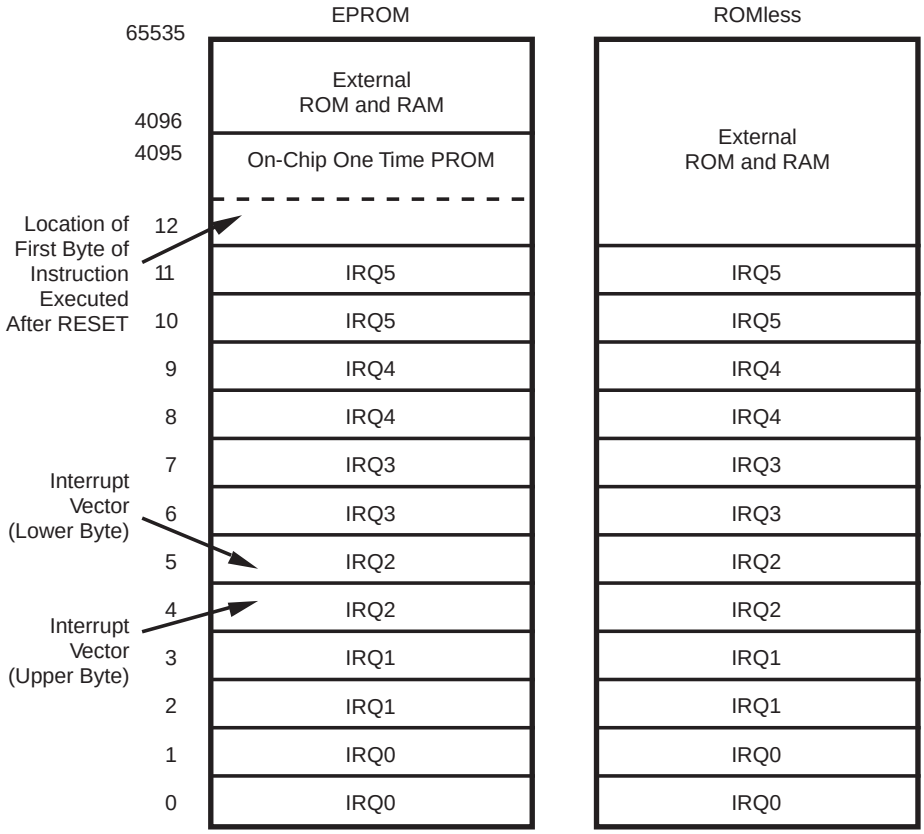


Figure 22. Program Memory Map (ROMless Z86E40 Only)

EPROM Protect. When in ROM Protect Mode, and executing out of External Program Memory, instructions LDC, LDCI, LDE, and LDEI cannot read Internal Program Memory.

When in ROM Protect Mode and executing out of Internal Program Memory, instructions LDC, LDCI, LDE, and LDEI can read Internal Program Memory.

FUNCTIONAL DESCRIPTION (Continued)

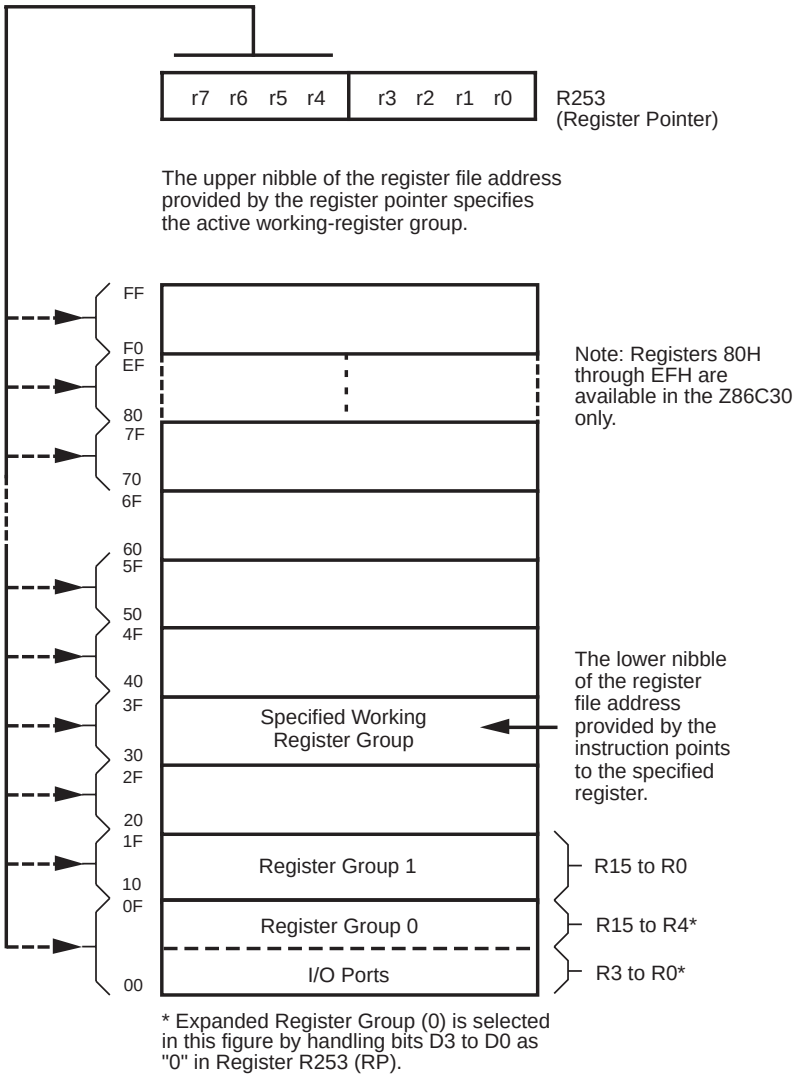


Figure 25. Register Pointer

FUNCTIONAL DESCRIPTION (Continued)

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. The register R254 is general-purpose on Z86E30/E31. R254 and R255 are set to 00H after any reset or STOP-Mode Recovery.

RAM Protect. The upper portion of the RAM's address spaces 80H to EFH (excluding the control registers) can be protected from reading and writing. This option can be selected during the EPROM Programming Mode. After this option is selected, the user can activate this feature from the internal EPROM. D6 of the IMR control register (R251) is used to turn off/on the RAM protect by loading a 0 or 1, respectively. A “1” in D6 indicates RAM Protect enabled. RAM Protect is not available on the Z86E31.

Stack. The Z86E40 external data memory or the internal register file can be used for the stack. The 16-bit Stack Pointer (R254–R255) is used for the external stack, which can reside anywhere in the data memory for ROMless mode, but only from 4096 to 65535 in ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack on the Z86E30/E31/E40 that resides within the 236 general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register when using internal stack only. R254 and R255 are set to 00H after any reset or Stop-Mode Recovery.

Counter/Timers. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 27).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256), that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (T_{OUT}) through which T0, T1, or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register (IPR). An interrupt machine cycle is activated when an interrupt request is granted. Thus, disabling all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in bits D7 and D6 of the IRQ Register (R250). The configuration is shown in Table 11.

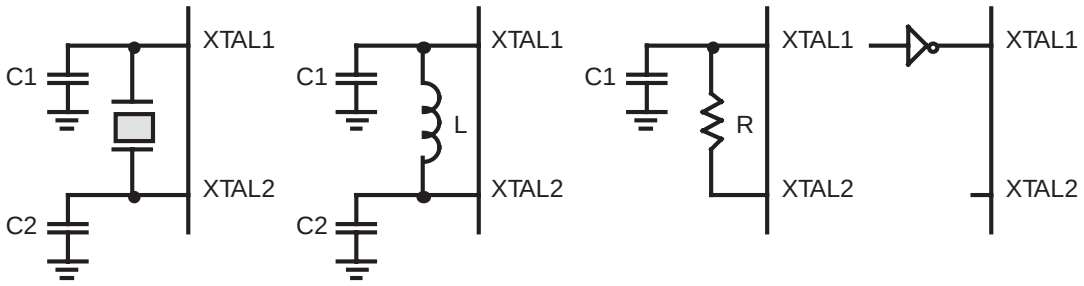
Table 11. IRQ Register Configuration

IRQ		Interrupt Edge	
D7	**D6**	**P31**	**P32**
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 KHz to 16 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to device pin Ground. The RC oscillator option can be selected in the programming mode. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Figure 29).



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
F = 8 MHz

LC
C1, C2 = 22 pF

L = 130 µH *
F = 3 MHz *

RC
@ 5V Vcc (TYP)

C1 = 100 pF
R = 2K
F = 6 MHz

External Clock

* Typical value including pin parasitics

Figure 29. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

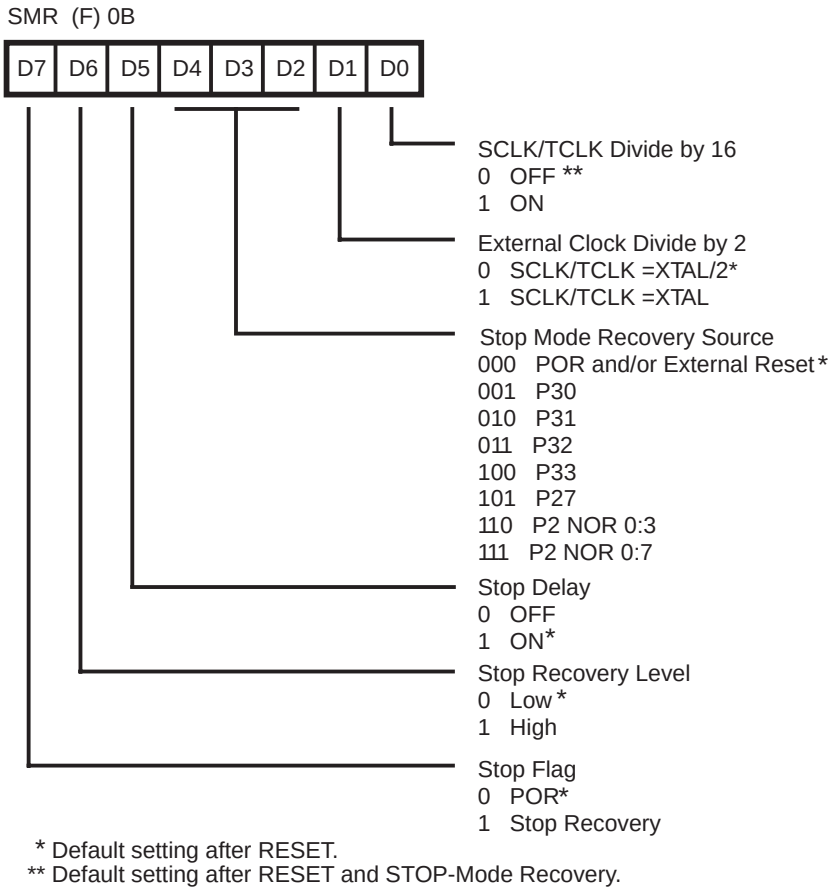
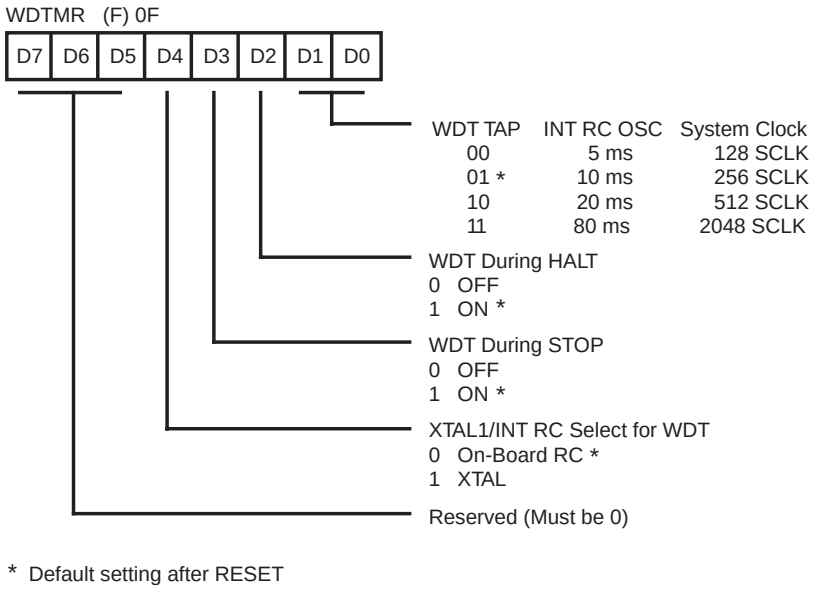


Figure 31. STOP-Mode Recovery Register (Write-Only Except Bit D7, Which is Read-Only)

cycles from the execution of the first instruction after Power-On Reset, Watch-Dog reset or a STOP-Mode Recovery (Figures 33 and 34). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH.



* Default setting after RESET

Figure 33. Watch-Dog Timer Mode Register Write Only

FUNCTIONAL DESCRIPTION (Continued)

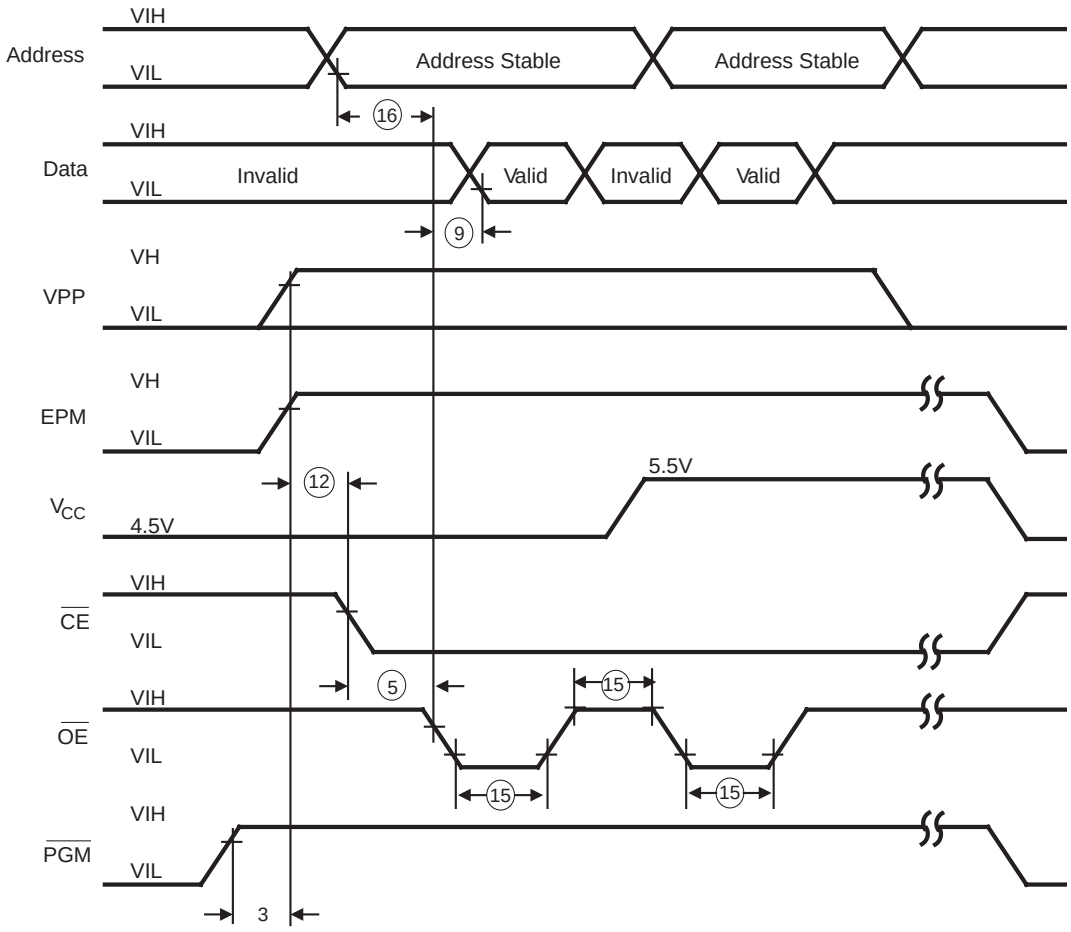


Figure 36. EPROM Read Mode Timing Diagram

Z86E40 TIMING DIAGRAMS (Continued)

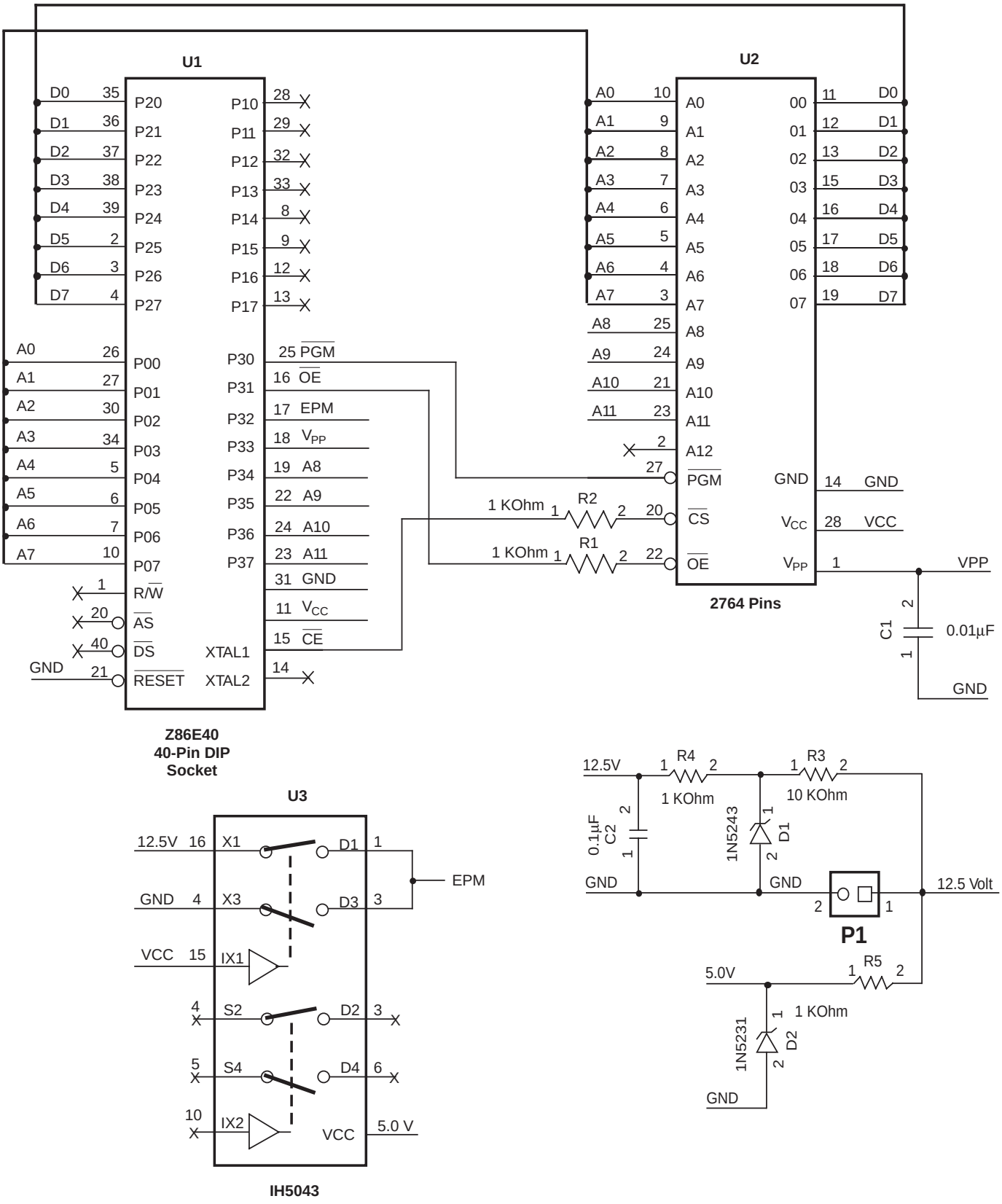
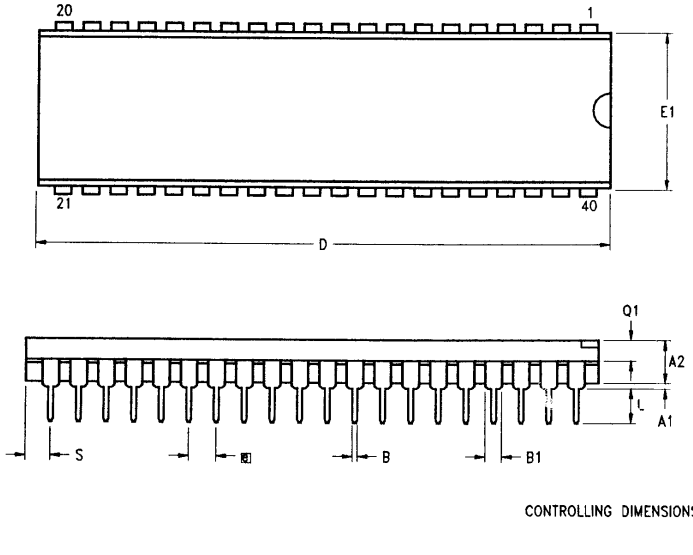


Figure 38. Z86E40 Z8 OTP Programming Adapter
For use with Standard EPROM Programmers

PACKAGE INFORMATION (Continued)

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

Figure 61. 40-Pin DIP Package Diagram

Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.