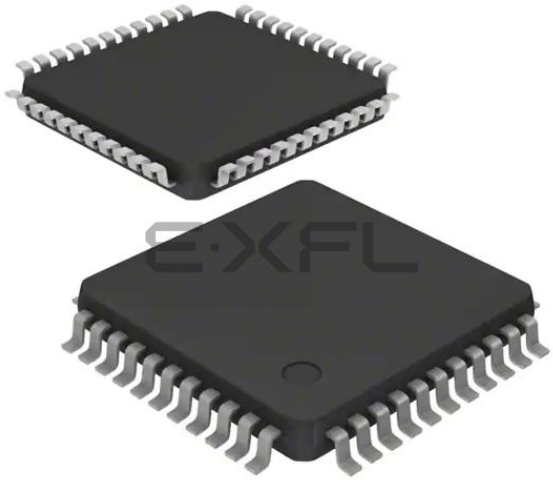

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e4016asg

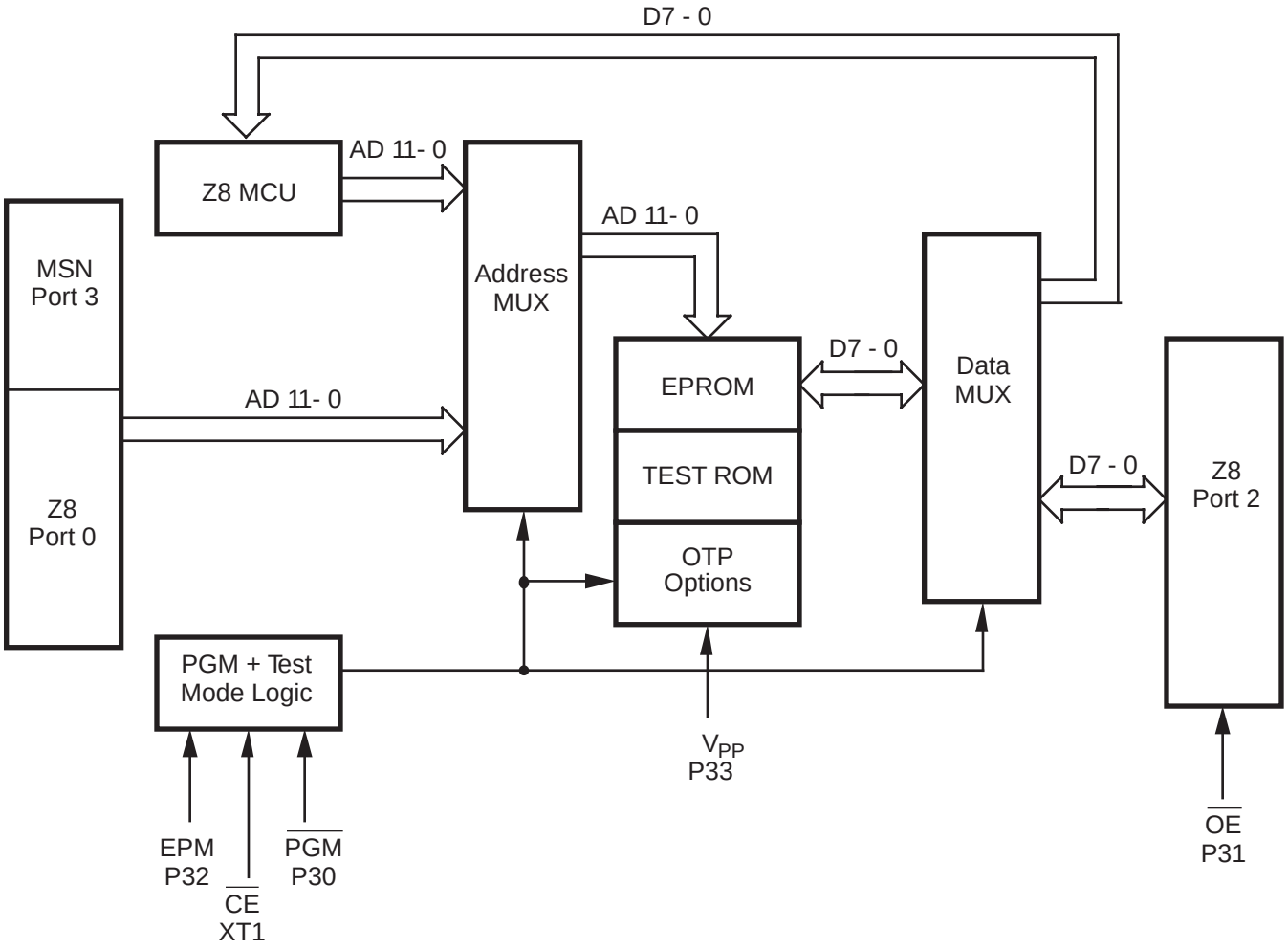


Figure 2. EPROM Programming Block Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

			T_A= 0 °C to +70 °C					
Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V 5.5V	0.7 V_{CC} 0.7 V_{CC}	V_{CC}+0.3 V_{CC}+0.3	1.8 2.5	V V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V 4.5V	GND -0.3 GND -0.3	0.2 V_{CC} 0.2 V_{CC}	0.9 1.5	V V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V 5.5V	0.7 V_{CC} 0.7 V_{CC}	V_{CC}+0.3 V_{CC}+0.3	2.5 2.5	V V		
V_{IL}	Input Low Voltage	3.5V 5.5V	GND -0.3 GND -0.3	0.2 V_{CC} 0.2 V_{CC}	1.5 1.5	V V		
V_{OH}	Output High Voltage Low EMI Mode	3.5V 5.5V	V_{CC} -0.4 V_{CC} -0.4		3.3 4.8	V V	I_{OH} = – 0.5 mA	
V_{OH1}	Output High Voltage	3.5V 5.5V	V_{CC} -0.4 V_{CC} -0.4		3.3 4.8	V V	I_{OH} = -2.0 mA I_{OH} = -2.0 mA	
V_{OL}	Output Low Voltage Low EMI Mode	3.5V 4.5V		0.4 0.4	0.2 0.2	V V	I_{OL} = 1.0 mA I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	3.5V 4.5V		0.4 0.4	0.1 0.1	V V	I_{OL} = + 4.0 mA I_{OL} = + 4.0 mA	8 8
V_{OL2}	Output Low Voltage	3.5V 4.5V		1.2 1.2	0.5 0.5	V V	I_{OL} = + 12 mA I_{OL} = + 12 mA	8 8
V_{RH}	Reset Input High Voltage	3.5V 5.5V	.8 V_{CC} .8 V_{CC}	V_{CC} V_{CC}	1.7 2.1	V V		
V_{RL}	Reset Input Low Voltage	3.5V 5.5V	GND -0.3 GND -0.3	0.2 V_{CC} 0.2 V_{CC}	1.3 1.7	V V		13
V_{OLR}	Reset Output Low Voltage	3.5V 5.5V		0.6 0.6	0.3 0.2	V V	I_{OL} = 1.0 mA I_{OL} = 1.0 mA	
V_{OFFSET}	Comparator Input Offset Voltage	3.5V 4.5V		25 25	10 10	mV mV		
V_{ICR}	Input Common Mode Voltage Range	3.5V 5.5V	0 0	V_{CC} -1.0V V_{CC} -1.0V		V V		10 10
I_{IL}	Input Leakage	3.5V 4.5V	-1 -1	2 2	0.032 0.032	µA µA	V_{IN} = 0V, V_{CC} V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V 4.5V	-1 -1	2 2	0.032 0.032	µA µA	V_{IN} = 0V, V_{CC} V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.5V 4.5V	-20 -20	-130 -180	-65 -112	µA µA		

DC ELECTRICAL CHARACTERISTICS (Continued)

				T_A = 0°C to 70°C 16 MHz			
No	Symbol	Parameter	Note [3] V_{CC}	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	3.5V 5.5V	25 25		ns ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	3.5V 5.5V	35 35		ns ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	3.5V 5.5V		180 180	ns ns	1,2
4	TwAS	$\overline{AS}$ Low Width	3.5V 5.5V	40 40		ns ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	3.5V 5.5V	0 0		ns ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	3.5V 5.5V	135 135		ns ns	1,2
7	TwDSW	$\overline{DS}$ (Write) Low Width	3.5V 5.5V	80 80		ns ns	1,2
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid	3.5V 5.5V		75 75	ns ns	1,2
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	3.5V 5.5V	0 0		ns ns	2
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	3.5V 5.5V	50 50		ns ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	3.5V 5.5V	35 35		ns ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	3.5V 5.5V	25 25		ns ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	3.5V 5.5V	35 35		ns ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	3.5V 5.5V	55 55	25 25	ns ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	3.5V 5.5V	35 35		ns ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.5V 5.5V		230 230	ns ns	1,2
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	3.5V 5.5V	45 45		ns ns	2
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Fall Delay	3.5V 5.5V	30 30		ns ns	2
20	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	3.5V 5.5V	35 35		ns ns	

Notes:

1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR D1 = 0, D0 = 0.

			T_A = -40°C to 105°C 16 MHz Note [3]				
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	4.5V 5.5V	25 25		ns ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	4.5V 5.5V	35 35		ns ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	4.5V 5.5V		180 180	ns ns	1,2
4	TwAS	$\overline{AS}$ Low Width	4.5V 5.5V	40 40		ns ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	4.5V 5.5V	0 0		ns ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	4.5V 5.5V	135 135		ns ns	1,2
7	TwDSW	$\overline{DS}$ (Write) Low Width	4.5V 5.5V	80 80		ns ns	1,2
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid	4.5V 5.5V		75 75	ns ns	1,2
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	4.5V 5.5V	0 0		ns ns	2
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	4.5V 5.5V	50 50		ns ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	4.5V 5.5V	35 35		ns ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	4.5V 5.5V	25 25		ns ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	4.5V 5.5V	35 35		ns ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	4.5V 5.5V	55 55	25 25	ns ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	4.5V 5.5V	35 35		ns ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	4.5V 5.5V		230 230	ns ns	1,2
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	4.5V 5.5V	45 45		ns ns	2
18	TdDM(AS)	/DM Valid to $\overline{AS}$ Fall Delay	4.5V 5.5V	30 30		ns ns	2
20	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	4.5V 5.5V	35 35		ns ns	

Notes:

1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

DC ELECTRICAL CHARACTERISTICS (Continued)

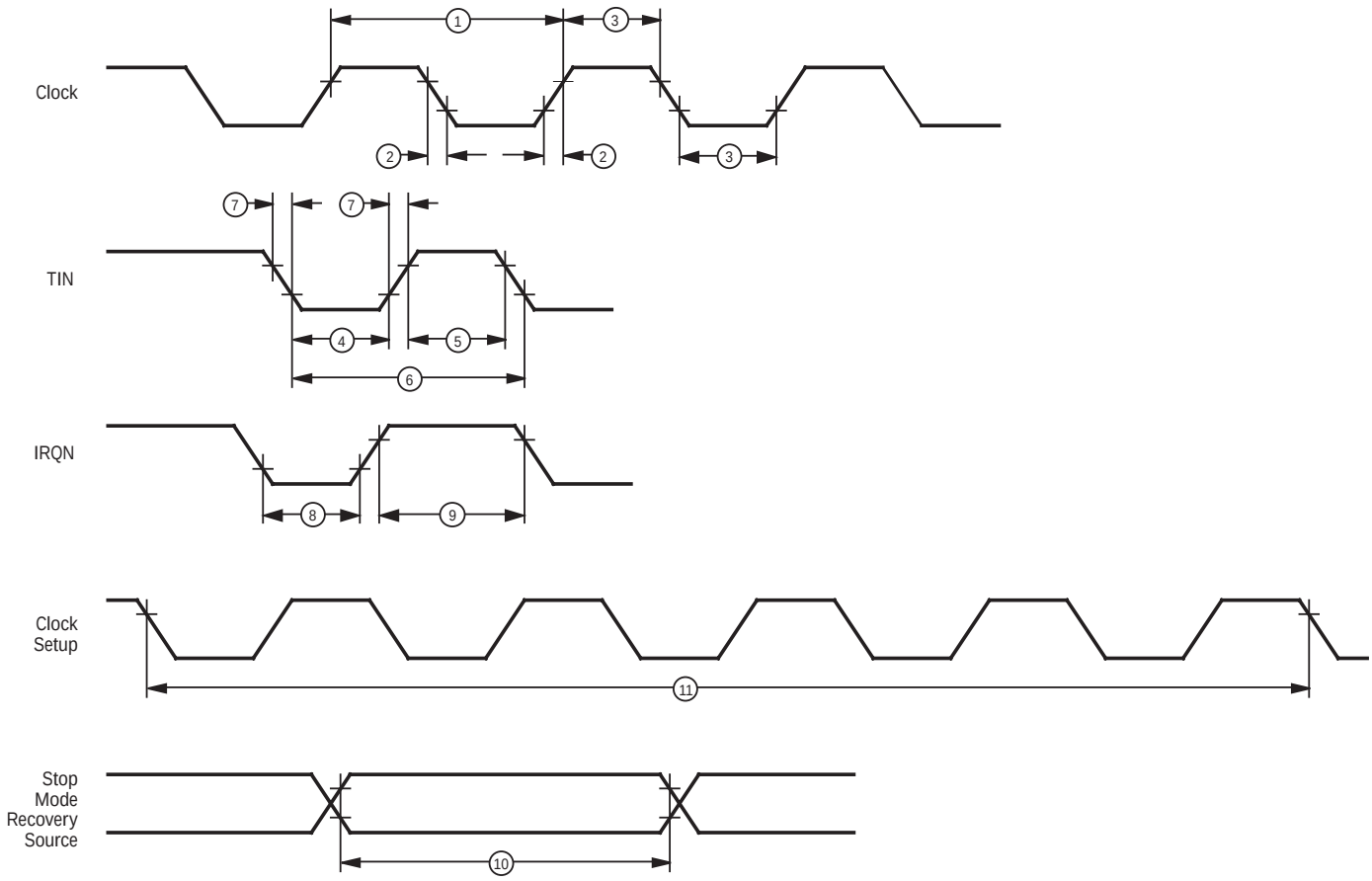


Figure 15. Additional Timing Diagram

DC ELECTRICAL CHARACTERISTICS (Continued)

Handshake Timing Diagrams

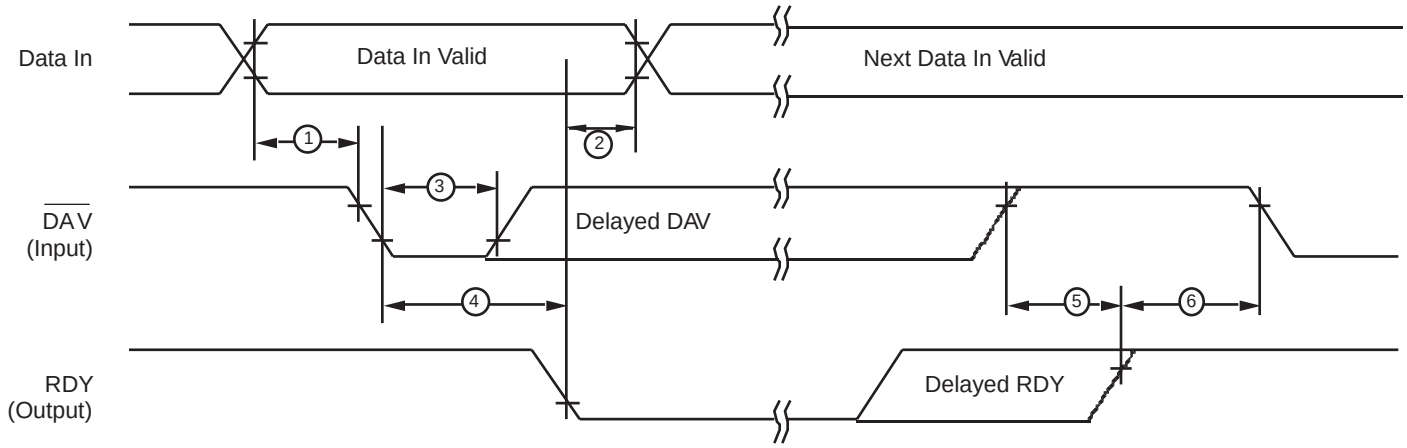


Figure 16. Input Handshake Timing

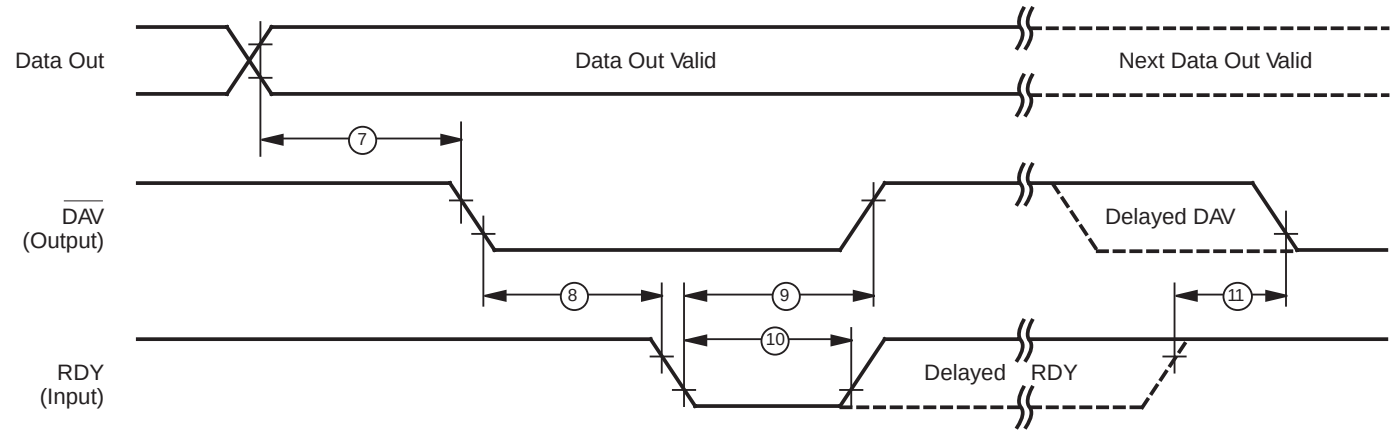


Figure 17. Output Handshake Timing

Additional Timing Table

				T_A = -40 °C to +105 °C 16 MHz				
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Units	Conditions	Notes
1	TpC	Input Clock Period	3.5V	62.5	DC	ns		1,7,8
			5.5V	62.5	DC	ns		1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15	ns		1,7,8
			5.5V		15	ns		1,7,8
3	TwC	Input Clock Width	3.5V	31		ns		1,7,8
			5.5V	31		ns		1,7,8
4	TwTinL	Timer Input Low Width	3.5V	70		ns		1,7,8
			5.5V	70		ns		1,7,8
5	TwTinH	Timer Input High Width	3.5V	5TpC				1,7,8
			5.5V	5TpC				1,7,8
6	TpTin	Timer Input Period	3.5V	8TpC				1,7,8
			5.5V	8TpC				1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100	ns		1,7,8
			5.5V		100	ns		1,7,8
8A	TwIL	Int. Request Low Time	3.5V	70		ns		1,2,7,8
			5.5V	70		ns		1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V	5TpC				1,3,7,8
			5.5V	5TpC				1,3,7,8
9	TwIH	Int. Request Input High Time	3.5V	5TpC				1,2,7,8
			5.5V					
10	Twsm	STOP Mode Recovery Width Spec	3.5V	12		ns		4,8
			5.5V	12		ns		4,8
11	Tost	Oscillator Startup Time	3.5V		5TpC			4,8
			5.5V		5TpC			4,8
12	Twdt	Watch-Dog Timer Delay Time Before Timeout	3.5V	10		ms	D0 = 0	5,11
			5.5V	5		ms	D1 = 0	5,11
			3.5V	20		ms	D0 = 1	5,11
			5.5V	10		ms	D1 = 0	5,11
			3.5V	40		ms	D0 = 0	5,11
			5.5V	20		ms	D1 = 1	5,11
			3.5V	160		ms	D0 = 1	5,11
			5.5V	80		ms	D1 = 1	5,11

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31–P33)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Reg. WDTMR
6. The V_{CC} voltage spec. of 5.5V guarantees 5.0V ± 0.5V.
7. SMR D1 = 0
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
9. For RC and LC oscillator, and for oscillator driven by clock driver.
10. Standard Mode (not Low EMI output ports)
11. Using internal RC

PIN FUNCTIONS (Continued)

Port 1 (P17–P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7–A0) and Data (D7–D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and /DAV1 (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (Figure 19).

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z86E40 to share common resources in multiprocessor and DMA applications.

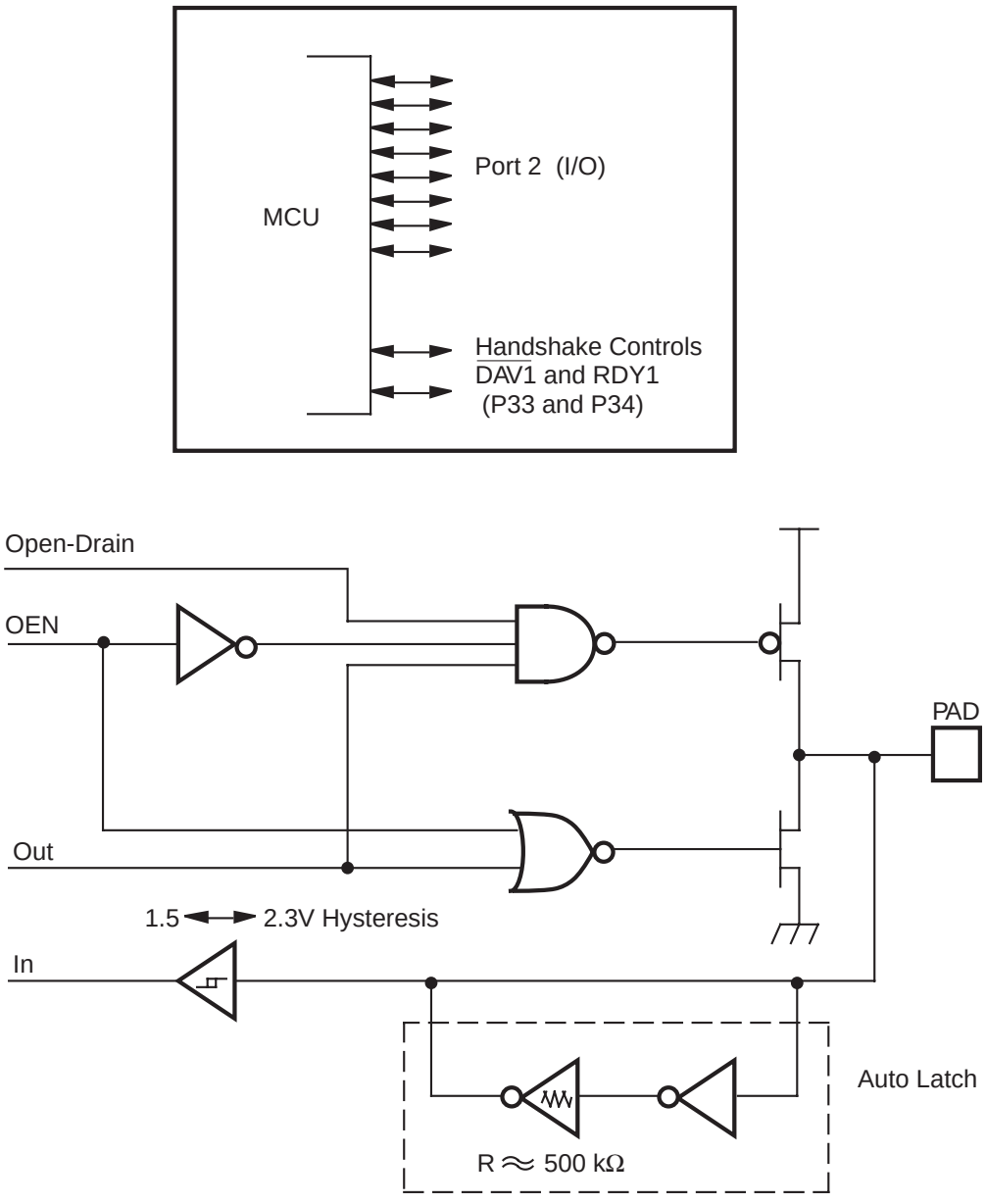


Figure 19. Port 1 Configuration (Z86E40 Only)

Port 2 (P27–P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control.

In Handshake Mode, Port 3 lines P31 and P36 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2 (Figure 20).

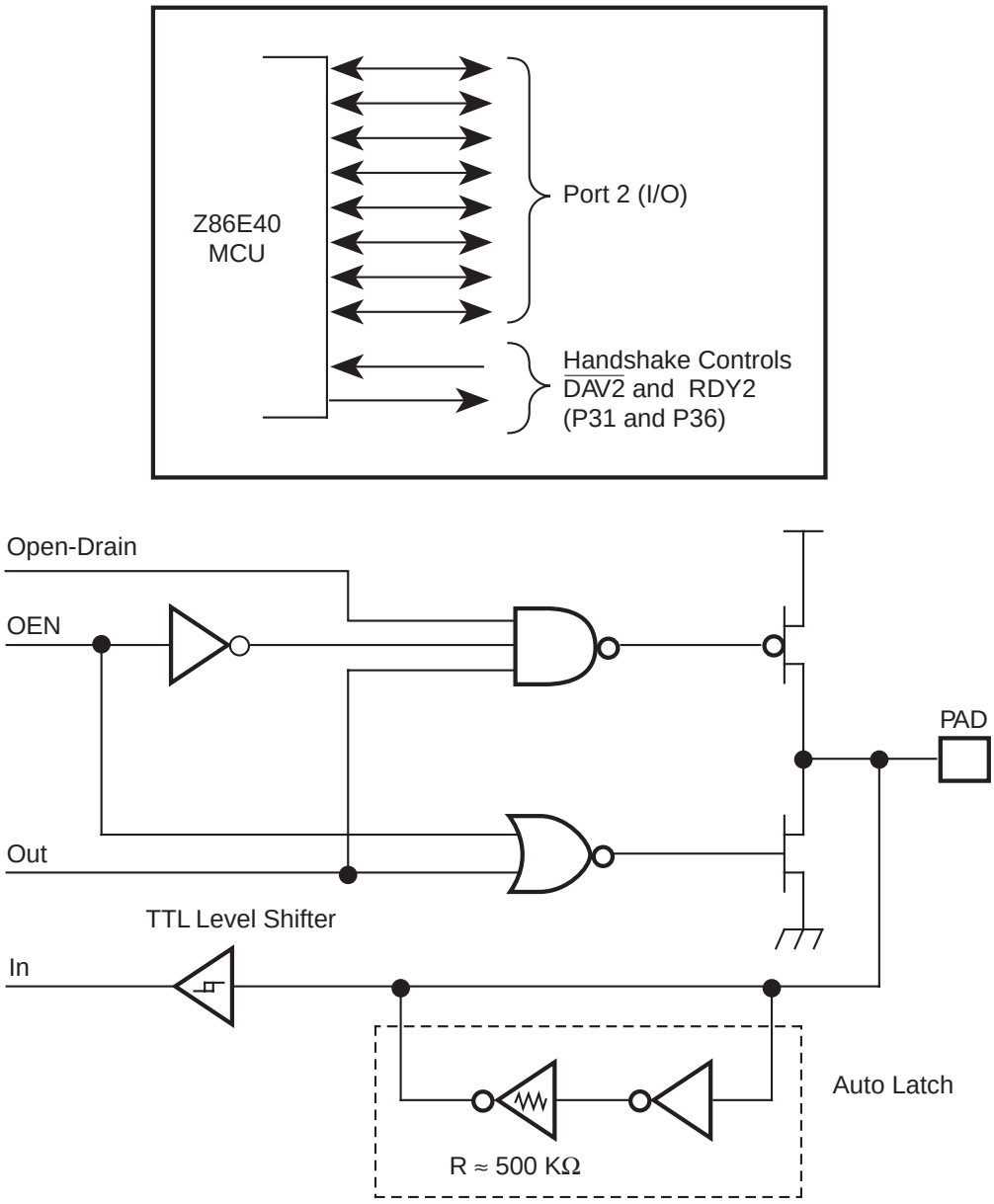


Figure 20. Port 2 Configuration

FUNCTIONAL DESCRIPTION

The MCU incorporates the following special functions to enhance the standard Z8 architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of three ways:

1. Power-On Reset
2. Watch-Dog Timer
3. STOP-Mode Recovery Source

Note: Having the Auto Power-On Reset circuitry built-in, the MCU does not need to be connected to an external power-on reset circuit. The reset time is 5 ms (typical). The MCU does not reinitialize WDTMR, SMR, P2M, and P3M registers to their reset values on a STOP-Mode Recovery operation.

Note: The device V_{CC} must rise up to the operating V_{CC} specification before the TPOR expires.

Program Memory. The MCU can address up to 4 KB of Internal Program Memory (Figure 22). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 12 (000CH) to address 4095 (0FFFH) consists of programmable EPROM. After reset, the program counter points at the address 000CH, which is the starting address of the user program.

In ROMless mode, the Z86E40 can address up to 64 KB of External Program Memory. The ROM/ROMless option is only available on the 44-pin devices.

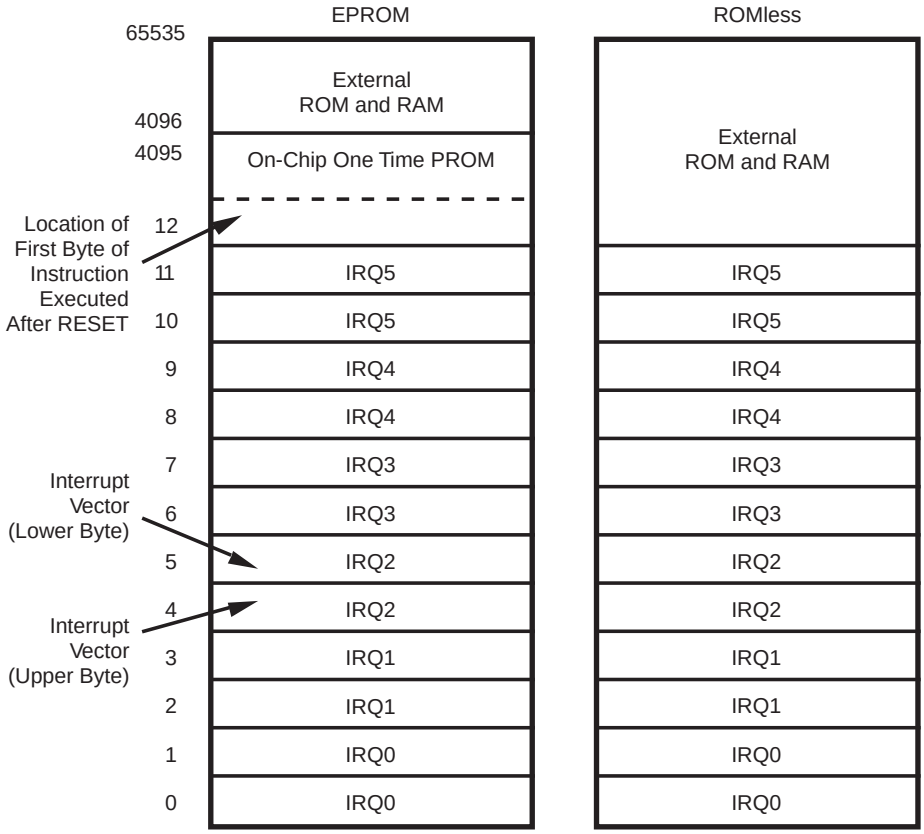


Figure 22. Program Memory Map (ROMless Z86E40 Only)

EPROM Protect. When in ROM Protect Mode, and executing out of External Program Memory, instructions LDC, LDCI, LDE, and LDEI cannot read Internal Program Memory.

When in ROM Protect Mode and executing out of Internal Program Memory, instructions LDC, LDCI, LDE, and LDEI can read Internal Program Memory.

FUNCTIONAL DESCRIPTION (Continued)

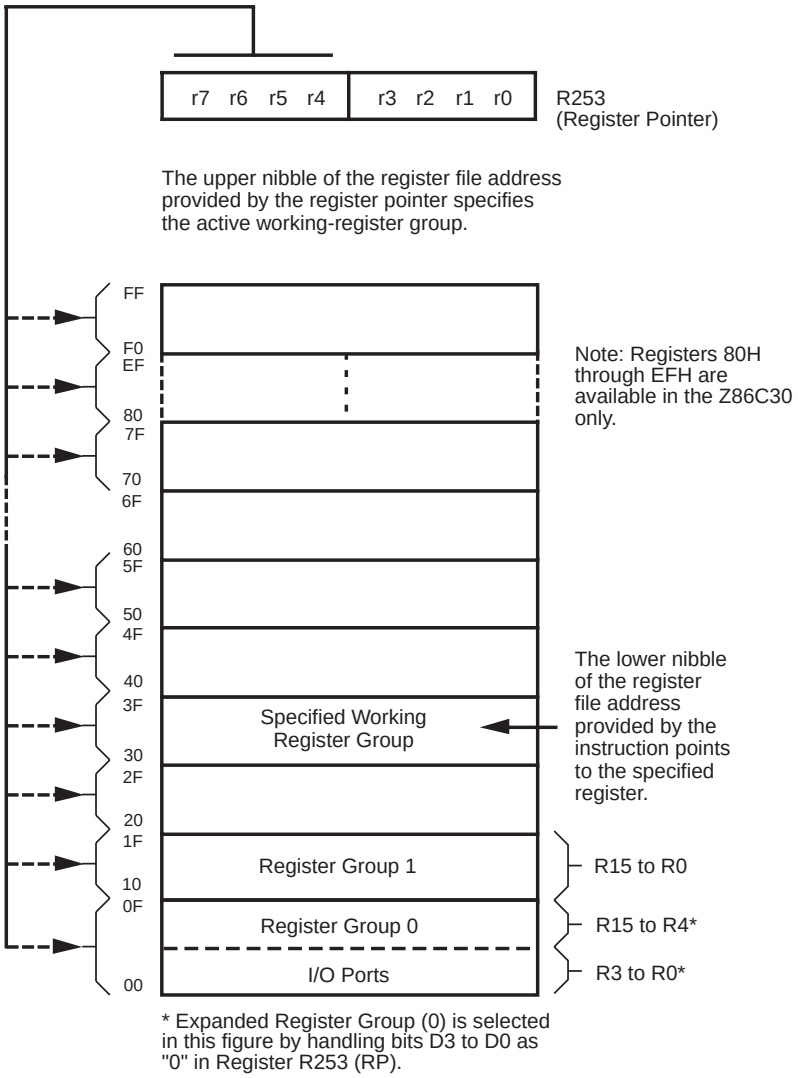


Figure 25. Register Pointer

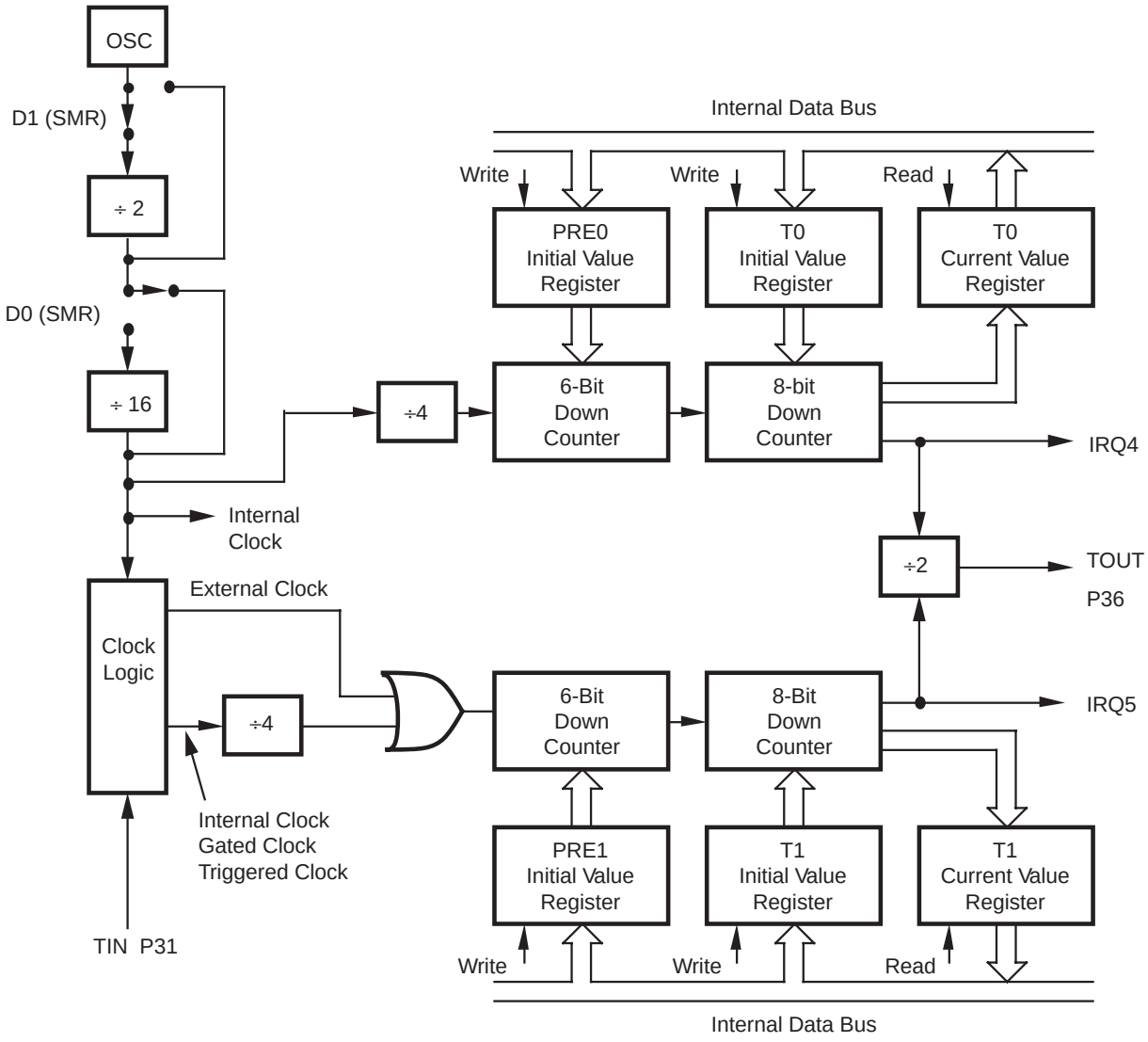


Figure 27. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The MCU has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 28). The six sources are divided as follows: four sources are claimed by Port 3 lines P33–P30) and two in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 10).

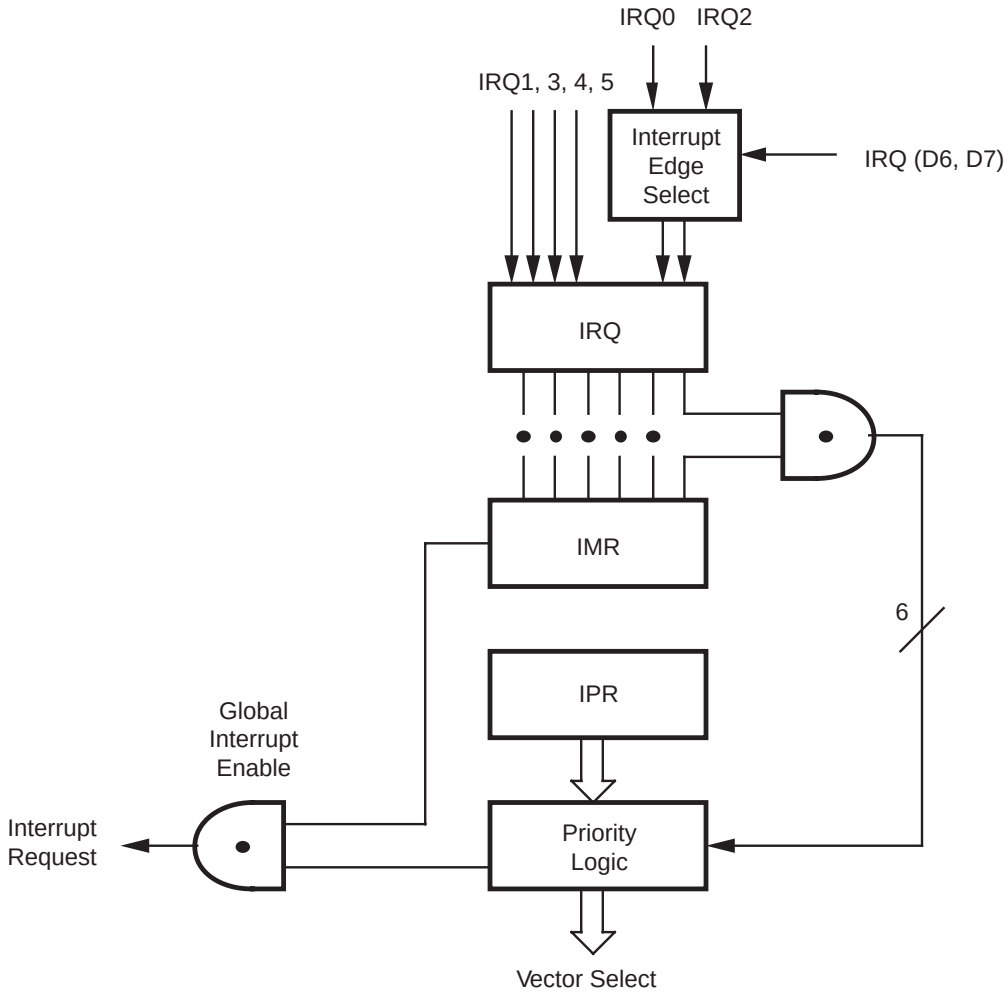


Figure 28. Interrupt Block Diagram

Table 10. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	$\overline{DAV0}$, IRQ0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	$\overline{DAV2}$, IRQ2, T_{IN}	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Falling Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	TI	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register (IPR). An interrupt machine cycle is activated when an interrupt request is granted. Thus, disabling all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in bits D7 and D6 of the IRQ Register (R250). The configuration is shown in Table 11.

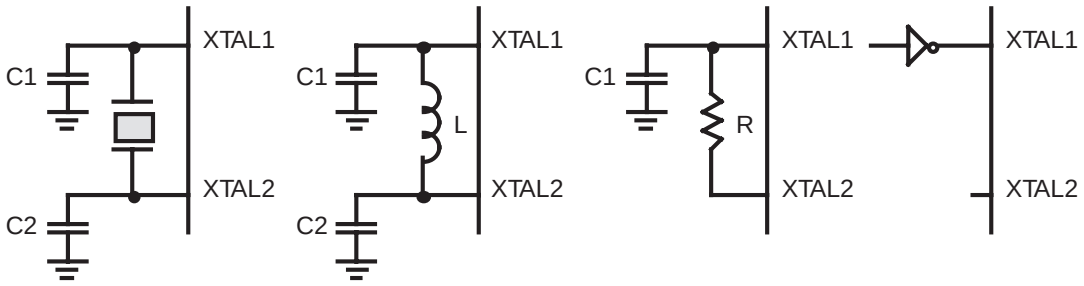
Table 11. IRQ Register Configuration

IRQ		Interrupt Edge	
D7	**D6**	**P31**	**P32**
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 KHz to 16 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to device pin Ground. The RC oscillator option can be selected in the programming mode. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Figure 29).



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
F = 8 MHz

LC
C1, C2 = 22 pF

L = 130 µH *
F = 3 MHz *

RC
@ 5V Vcc (TYP)

C1 = 100 pF
R = 2K
F = 6 MHz

External Clock

* Typical value including pin parasitics

Figure 29. Oscillator Configuration

Comparator Output Port 3 (D0). Bit 0 controls the comparator output in Port 3. A “1” in this location brings the comparator outputs to P34 and P37, and a “0” releases the Port to its standard I/O configuration. The default value is 0.

Port 1 Open-Drain (D1). Port 1 can be configured as an open-drain by resetting this bit (D1=0) or configured as push-pull active by setting this bit (D1=1). The default value is 1.

Port 0 Open-Drain (D2). Port 0 can be configured as an open-drain by resetting this bit (D2=0) or configured as push-pull active by setting this bit (D2=1). The default value is 1.

Low EMI Port 0 (D3). Port 0 can be configured as a Low EMI Port by resetting this bit (D3=0) or configured as a Standard Port by setting this bit (D3=1). The default value is 1.

Low EMI Port 1 (D4). Port 1 can be configured as a Low EMI Port by resetting this bit (D4=0) or configured as a Standard Port by setting this bit (D4=1). The default value is 1. **Note:** The emulator does not support Port 1 low EMI mode and must be set D4 = 1.

Low EMI Port 2 (D5). Port 2 can be configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting this bit (D5=1). The default value is 1.

Low EMI Port 3 (D6). Port 3 can be configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting this bit (D6=1). The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A “1” in this location configures the oscillator with standard drive. While a “0” configures the oscillator with low noise drive, however, it does not affect the relationship of SCLK and XTAL. The low EMI mode will reduce the drive of the oscillator (OSC). The default value is 1. **Note:** 4 MHz is the maximum external clock frequency when running in the low EMI oscillator mode.

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 31). All bits are Write Only except bit 7 which is a Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power-on cycle. Bit 6 controls whether a low or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the Stop-Mode Recovery Source. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

Table 14. EPROM Programming Table

Programming Modes	V_{PP}	EPM	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	ADDR	DATA	V_{CC}*
EPROM READ1	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	4.5V†
EPROM READ2	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.5V†
PROGRAM	V_H	V_H	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.4V
PROGRAM VERIFY	V_H	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.0V
OPTION BIT PGM	V_H	V_H	V_{IL}	V_{IH}	V_{IL}	63	IN	6.4V
OPTION BIT READ	X	V_H	V_{IL}	V_{IL}	V_{IH}	63	OUT	6.0V

Notes:
V_H = 13.0 V ± 0.1 V
V_{IH} = As per specific Z8 DC specification
VIL= As per specific Z8 DC specification
X=Not used, but must be set to V_H, V_{IH}, or V_{IL} level.
NU = Not used, but must be set to either V_{IH} or V_{IL} level.
I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum.
*V_{CC} has a tolerance of ±0.25V.
† Zilog recommends an EPROM read at V_{CC} = 4.5 V and 5.5 V to ensure proper device operations during the V_{CC} after programming, but V_{CC} = 5.0 V is acceptable.

Table 15. EPROM Programming Timing

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95	1.05	ms
7	Data Hold Time	2		µs
8	$\overline{OE}$ Setup Time	2		µs
9	Data Access Time	200		ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width/Option Program Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	$\overline{PGM}$ Setup Time	2		µs
14	Address to $\overline{OE}$ Setup Time	2		µs
15	$\overline{OE}$ Width	250		ns
16	Address to $\overline{OE}$ Low	125		ns

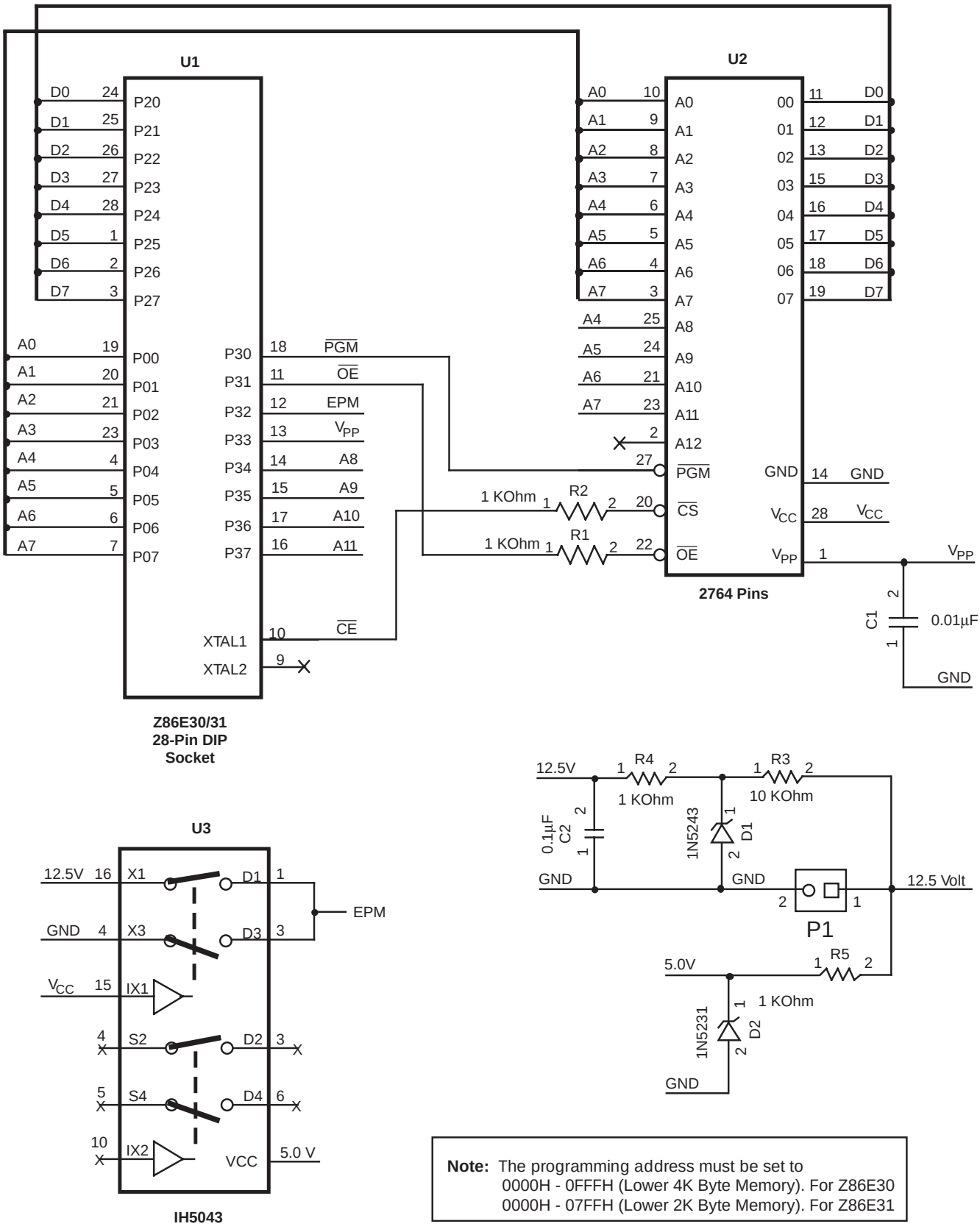


Figure 39. Z86E30/E31 Programming Adapter Circuitry

EXPANDED REGISTER FILE CONTROL REGISTERS

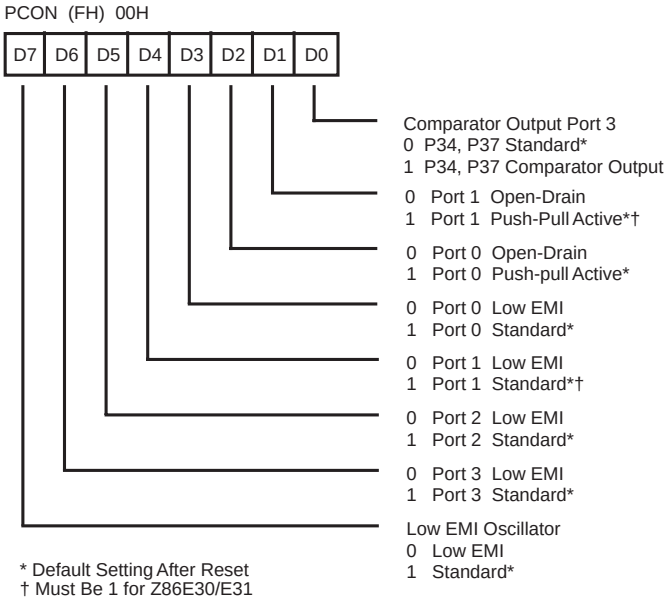


Figure 41. Port Configuration Register Write Only

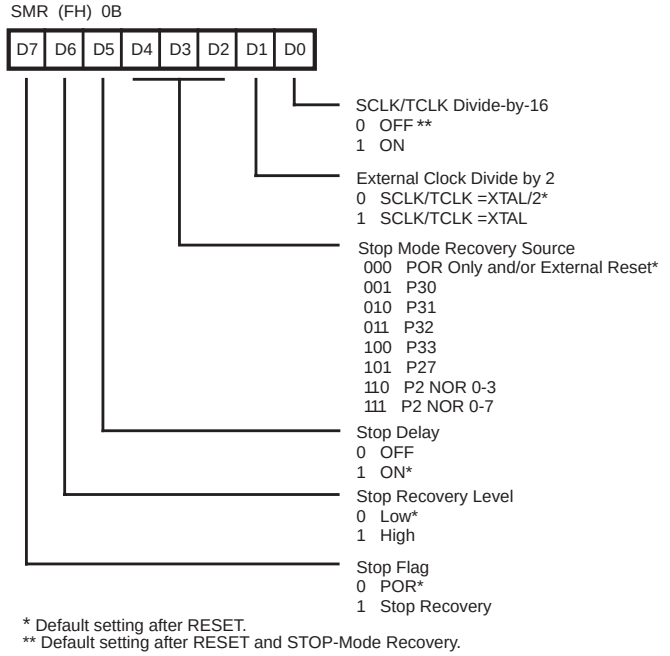


Figure 42. STOP-Mode Recovery Register Write Only Except Bit D7, Which is Read Only

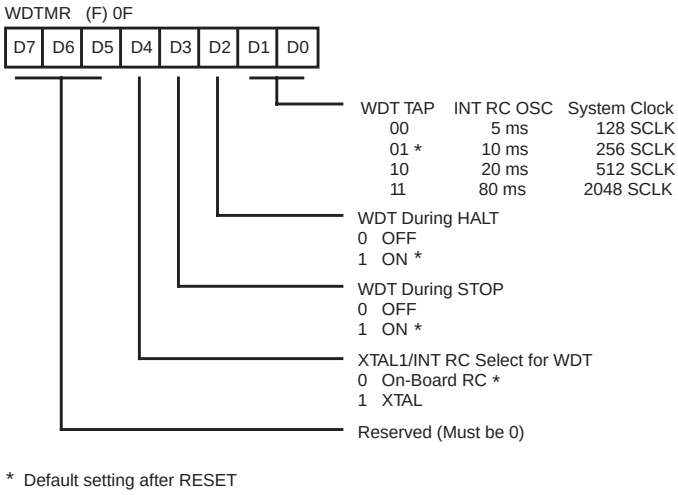


Figure 43. Watch-Dog Timer Mode Register Write Only

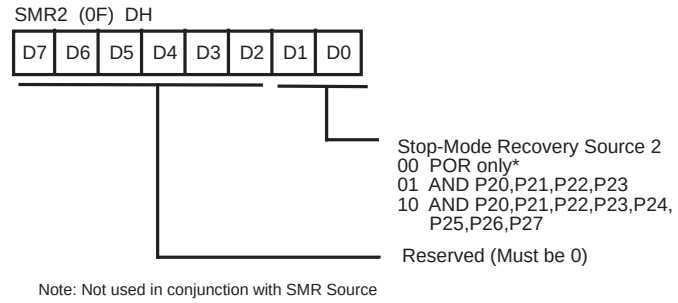


Figure 44. STOP-Mode Recovery Register 2 Write Only

Z8 CONTROL REGISTER DIAGRAMS (Continued)

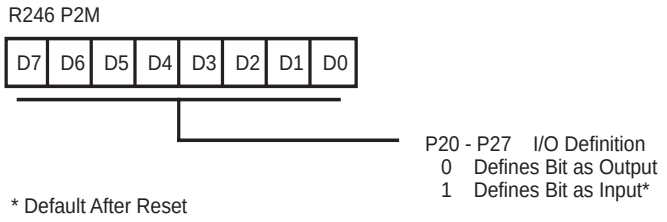


Figure 51. Port 2 Mode Register
F6H: Write Only

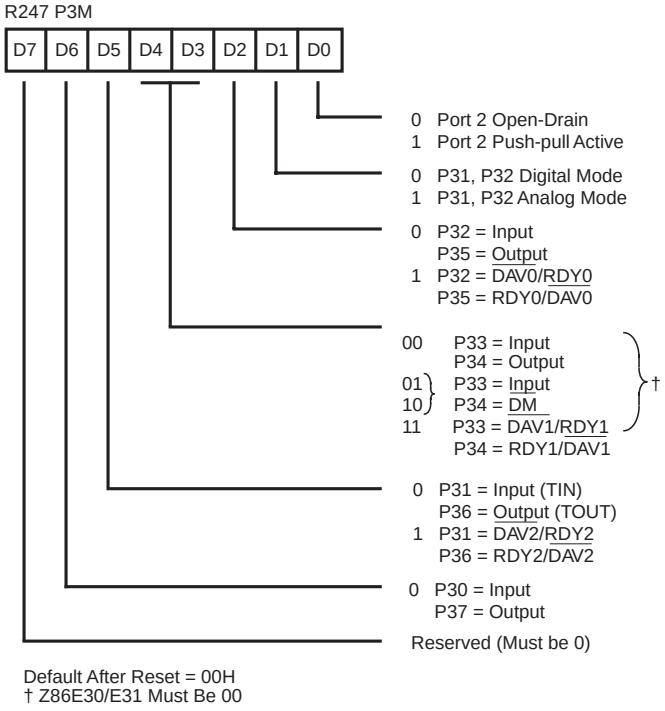


Figure 52. Port 3 Mode Register
F7H: Write Only

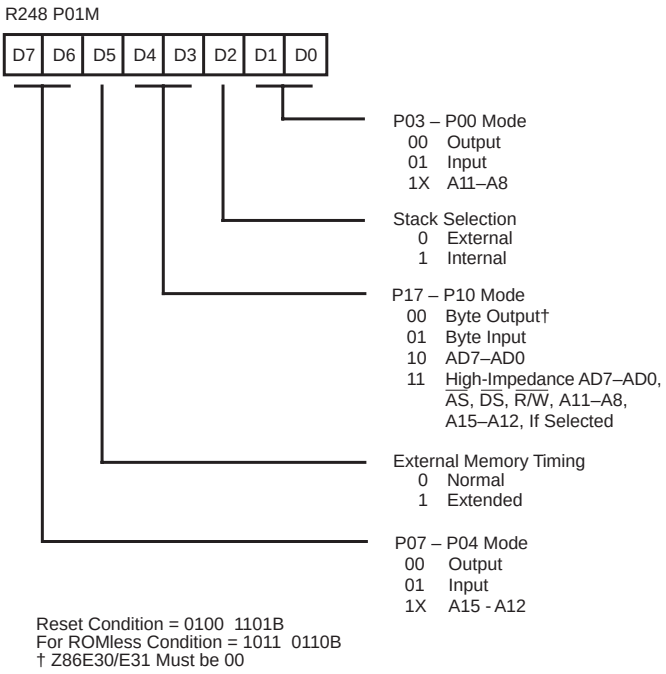


Figure 53. Port 0 and 1 Mode Register
F8H: Write Only
Z86E30/E31 Only

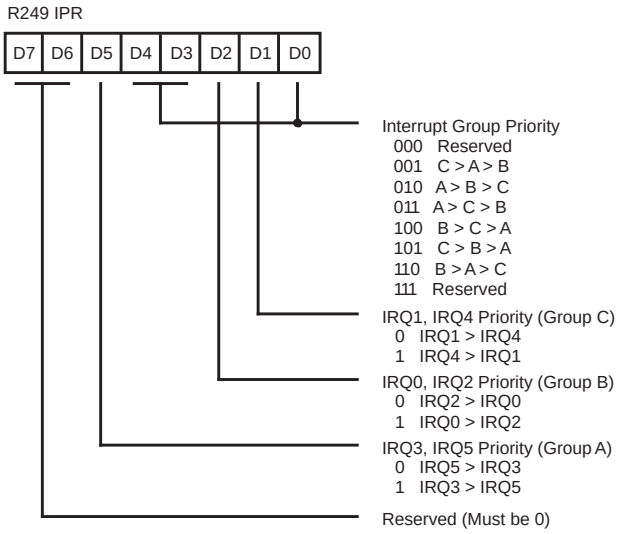


Figure 54. Interrupt Priority Register
F9H: Write Only

Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.