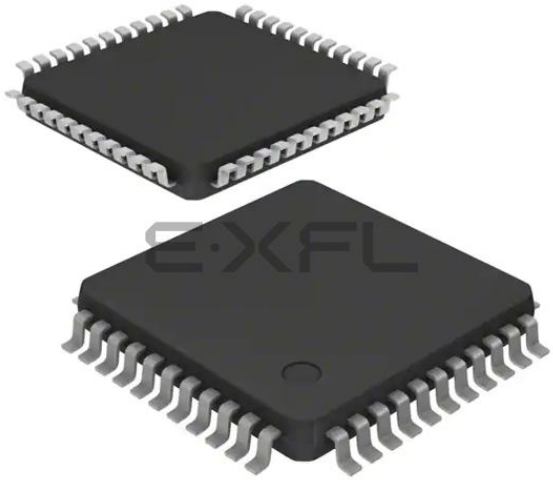

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e4016feg

PIN IDENTIFICATION

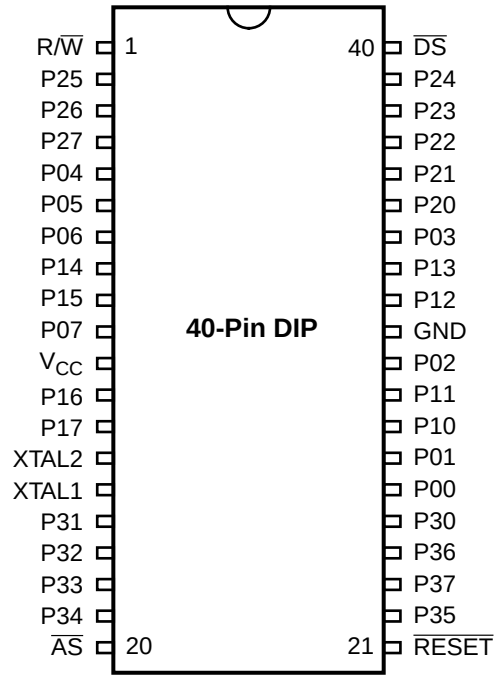


Figure 3. 40-Pin DIP Pin Configuration Standard Mode

Table 1. 40-Pin DIP Pin Identification Standard Mode

Pin #	Symbol	Function	Direction
1	R/$\overline{W}$	Read/Write	Output
2–4	P25–P27	Port 2, Pins 5,6,7	In/Output
5–7	P04–P06	Port 0, Pins 4,5,6	In/Output
8–9	P14–P15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V_{CC}	Power Supply	
12–13	P16–P17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal Oscillator	Output
15	XTAL1	Crystal Oscillator	Input
16–18	P31–P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	$\overline{AS}$	Address Strobe	Output
21	$\overline{RESET}$	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26–27	P00–P01	Port 0, Pins 0,1	In/Output
28–29	P10–P11	Port 1, Pins 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground	
32–33	P12–P13	Port 1, Pins 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35–39	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output
40	$\overline{DS}$	Data Strobe	Output

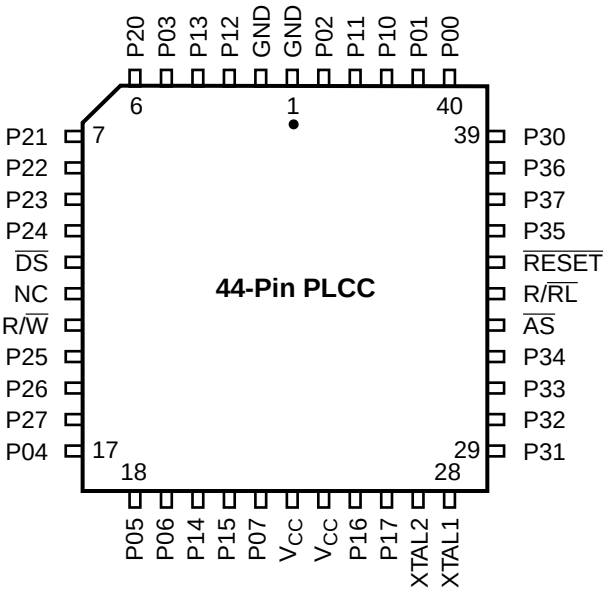


Figure 4. 44-Pin PLCC Pin Configuration
Standard Mode

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1–2	GND	Ground	
3–4	P12–P13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6–10	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output
11	$\overline{DS}$	Data Strobe	Output
12	NC	No Connection	
13	R/$\overline{W}$	Read/Write	Output
14–16	P25–P27	Port 2, Pins 5,6,7	In/Output
17–19	P04–P06	Port 0, Pins 4,5,6	In/Output
20–21	P14–P15	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23–24	V_{CC}	Power Supply	
25–26	P16–P17	Port 1, Pins 6,7	In/Output
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29–31	P31–P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
33	$\overline{AS}$	Address Strobe	Output
34	R/$\overline{RL}$	ROM/ROMless select	Input
35	$\overline{RESET}$	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40–41	P00–P01	Port 0, Pins 0,1	In/Output
42–43	P10–P11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

PIN IDENTIFICATION (Continued)

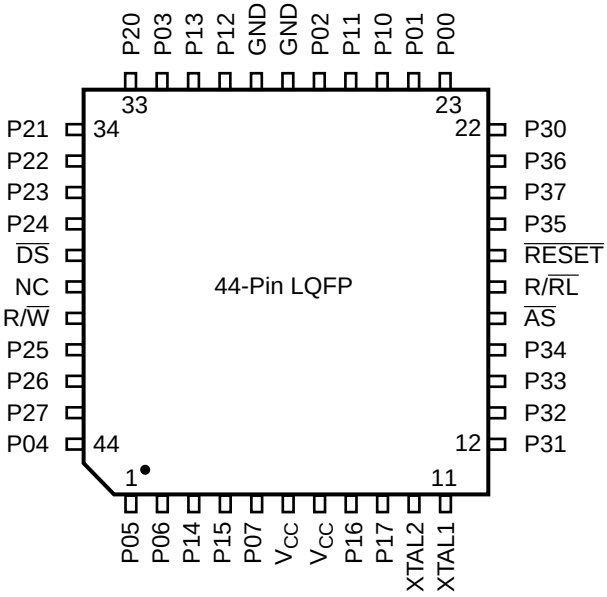


Figure 5. 44-Pin LQFP Pin Configuration
Standard Mode

Table 3. 44-Pin LQFP Pin Identification

Pin #	Symbol	Function	Direction
1–2	P05–P06	Port 0, Pins 5,6	In/Output
3–4	P14–P15	Port 1, Pins 4,5	In/Output
5	P07	Port 0, Pin 7	In/Output
6–7	V_{CC}	Power Supply	
8–9	P16–P17	Port 1, Pins 6,7	In/Output
10	XTAL2	Crystal Oscillator	Output
11	XTAL1	Crystal Oscillator	Input
12–14	P31–P33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	$\overline{AS}$	Address Strobe	Output
17	R/$\overline{RL}$	ROM/ROMless select	Input
18	$\overline{RESET}$	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23–24	P00–P01	Port 0, Pin 0,1	In/Output
25–26	P10–P11	Port 1, Pins 0,1	In/Output

Table 3. 44-Pin LQFP Pin Identification

Pin #	Symbol	Function	Direction
27	P02	Port 0, Pin 2	In/Output
28–29	GND	Ground	
30–31	P12–P13	Port 1, Pins 2,3	In/Output
32	P03	Port 0, Pin 3	In/Output
33–37	P20–4	Port 2, Pins 0,1,2,3,4	In/Output
38	$\overline{DS}$	Data Strobe	Output
39	NC	No Connection	
40	R/$\overline{W}$	Read/Write	Output
41–43	P25–P27	Port 2, Pins 5,6,7	In/Output
44	P04	Port 0, Pin 4	In/Output

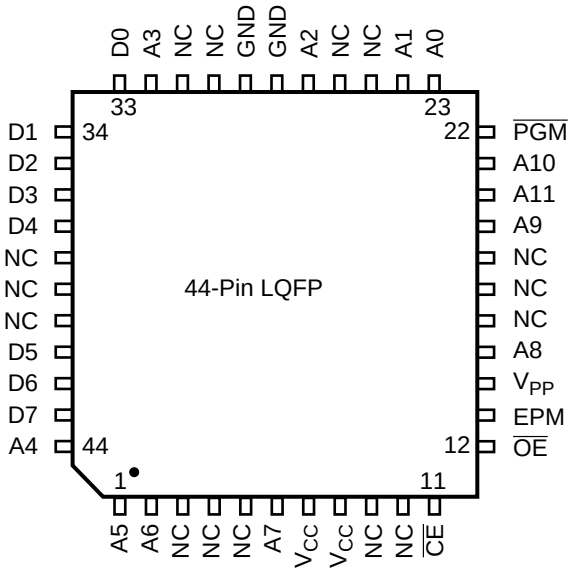


Figure 8. 44-Pin LQFP Pin Configuration EPROM Programming Mode

Table 6. 44-Pin LQFP Pin Configuration EPROM Programming Mode

Pin #	Symbol	Function	Direction
1–2	A5–A6	Address 5,6	Input
3–4	NC	No Connection	
5	A7	Address 7	Input
6–7	V_{CC}	Power Supply	
8–10	NC	No Connection	
11	$\overline{CE}$	Chip Select	Input
12	$\overline{OE}$	Output Enable	Input
13	EPM	EPROM Prog. Mode	Input
14	V_{PP}	Prog. Voltage	Input
15	A8	Address 8	Input
16–18	NC	No Connection	
19	A9	Address 9	Input
20	A11	Address 11	Input
21	A10	Address 10	Input
22	$\overline{PGM}$	Prog. Mode	Input

Table 6. 44-Pin LQFP Pin Configuration EPROM Programming Mode

Pin #	Symbol	Function	Direction
23–24	A0,A1	Address 0,1	Input
25–26	NC	No Connection	
27	A2	Address 2	Input
28–29	GND	Ground	
30–31	NC	No Connection	
32	A3	Address 3	Input
33–37	D0–D4	Data 0,1,2,3,4	In/Output
38–40	NC	No Connection	
41–43	D5–D7	Data 5,6,7	In/Output
44	A4	Address 4	Input

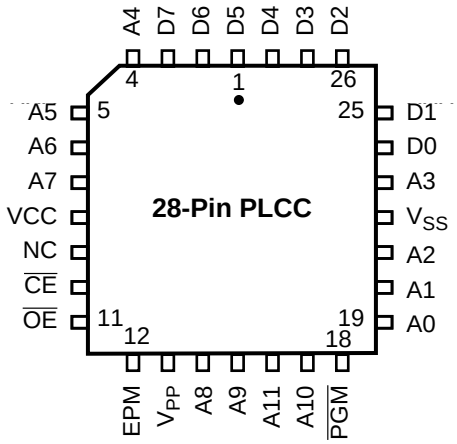


Figure 12. EPROM Programming Mode 28-Pin PLCC Pin Configuration

Table 8. 28-Pin EPROM Pin Identification

Pin #	Symbol	Function	Direction
1–3	D5–D7	Data 5,6,7	In/Output
4–7	A4–A7	Address 4,5,6,7	Input
8	V_{CC}	Power Supply	
9	NC	No connection	
10	$\overline{CE}$	Chip Select	Input
11	$\overline{OE}$	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V_{PP}	Prog. Voltage	Input
14–15	A8–A9	Address 8,9	Input
16	A11	Address 11	Input
17	A10	Address 10	Input
18	$\overline{PGM}$	Prog. Mode	Input
19–21	A0–A2	Address 0,1,2	Input
22	V_{SS}	Ground	
23	A3	Address 3	Input
24–28	D0–D4	Data 0,1,2,3,4	In/Output

DC ELECTRICAL CHARACTERISTICS (Continued)

			T_A=–40 °C to +105 °C					
Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{ALH}	Auto Latch High Current	4.5V	-1.0	-10	-3.8	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V	-1.0	-10	-3.8	µA	$0V < V_{IN} < V_{CC}$	9
T_{POR}	Power On Reset	4.5V	2.0	14	4	mS		
		5.5V	2.0	14	4	mS		
V_{LV}	Auto Reset Voltage		2.0	3.3	2.9	V		1

1. Device does function down to the Auto Reset voltage.
2. GND=0V
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1= CL2 = 22 pF
6. Same as note [4] except inputs at V_{CC}.
7. Maximum temperature is 70°C
8. STD Mode (not Low EMI Mode)
9. Auto Latch (mask option) selected
10. For analog comparator inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.
12. Typicals are at V_{CC} = 5.0V
13. Z86E40 only
14. WDT is not running.

Additional Timing Table (Divide-By-One Mode)

				T_A = 0 °C to +70 °C		T_A = -40 °C to +105 °C			
				4 MHz		4 MHz			
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.5V	250	DC	250	DC	ns	1,7,8
			5.5V	250	DC	250	DC	ns	1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		25		25	ns	1,7,8
			5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	3.5V	100		100		ns	1,7,8
			5.5V	100		100		ns	1,7,8
4	TwTinL	Timer Input Low Width	3.5V	100		100		ns	1,7,8
			5.5V	70		70		ns	1,7,8
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC			1,7,8
			5.5V	5TpC		5TpC			1,7,8
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC			1,7,8
			5.5V	8TpC		8TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns	1,7,8
			5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low Time	3.5V	100		100		ns	1,2,7,8
			5.5V	70		70		ns	1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC			1,3,7,8
			5.5V	5TpC		5TpC			1,3,7,8
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC			1,2,7,8
			5.5V	5TpC		5TpC			1,2,7,8
10	Twsm	STOP Mode Recovery Width Spec	3.5V	12		12		ns	4,8
			5.5V	12		12		ns	4,8
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC		4,8,9
			5.5V		5TpC				

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31–P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 1, POR STOP Mode Delay is on.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V and the V_{CC} voltage specification of 3.5V guarantees 3.5V only.
7. SMR D1 = 0.
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

FUNCTIONAL DESCRIPTION

The MCU incorporates the following special functions to enhance the standard Z8 architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of three ways:

1. Power-On Reset
2. Watch-Dog Timer
3. STOP-Mode Recovery Source

Note: Having the Auto Power-On Reset circuitry built-in, the MCU does not need to be connected to an external power-on reset circuit. The reset time is 5 ms (typical). The MCU does not reinitialize WDTMR, SMR, P2M, and P3M registers to their reset values on a STOP-Mode Recovery operation.

Note: The device V_{CC} must rise up to the operating V_{CC} specification before the TPOR expires.

Program Memory. The MCU can address up to 4 KB of Internal Program Memory (Figure 22). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 12 (000CH) to address 4095 (0FFFH) consists of programmable EPROM. After reset, the program counter points at the address 000CH, which is the starting address of the user program.

In ROMless mode, the Z86E40 can address up to 64 KB of External Program Memory. The ROM/ROMless option is only available on the 44-pin devices.

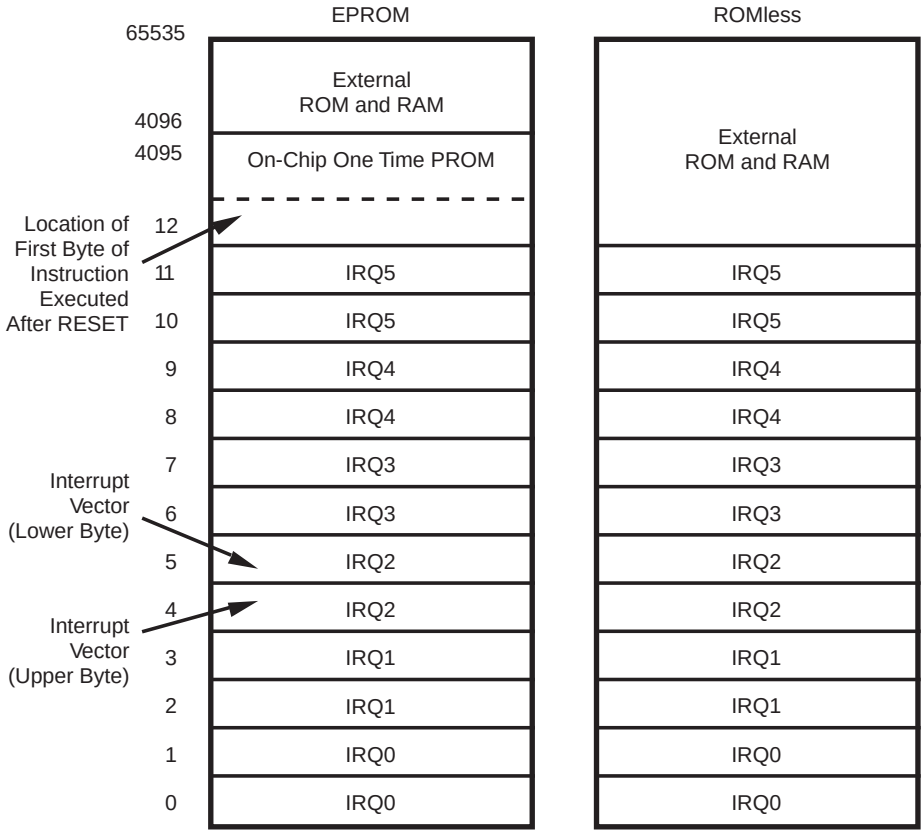


Figure 22. Program Memory Map (ROMless Z86E40 Only)

EPROM Protect. When in ROM Protect Mode, and executing out of External Program Memory, instructions LDC, LDCI, LDE, and LDEI cannot read Internal Program Memory.

When in ROM Protect Mode and executing out of Internal Program Memory, instructions LDC, LDCI, LDE, and LDEI can read Internal Program Memory.

FUNCTIONAL DESCRIPTION (Continued)

Data Memory ($\overline{DM}$). In EPROM Mode, the Z86E40 can address up to 60 KB of external data memory beginning at location 4096. In ROMless mode, the Z86E40 can address up to 64 KB of data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 23). The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory.

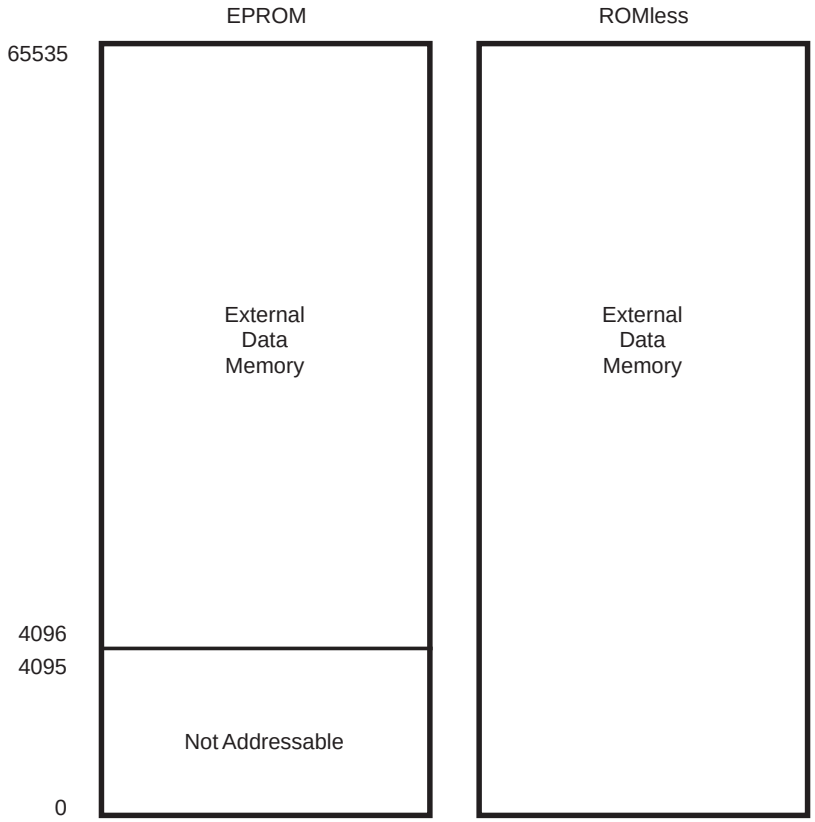


Figure 23. Data Memory Map

Register File. The register file consists of three I/O port registers, 236/125 general-purpose registers, 15 control and status registers, and three system configuration registers in the expanded register group. The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 24). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Bank E0–EF can only be accessed through working register and indirect addressing modes. (This bank is available in Z86E30/E40 only.)

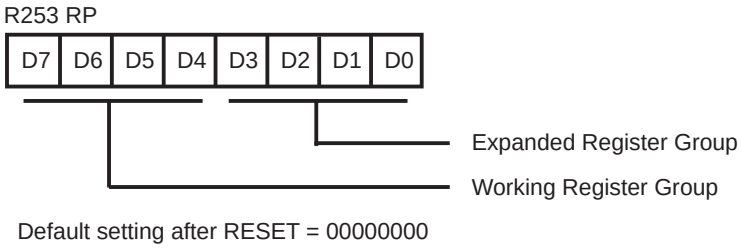


Figure 24. Register Pointer Register

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 26). These register groups are known as the Expanded Register File (ERF).

The low nibble (D3–D0) of the Register Pointer (RP) select the active ERF group, and the high nibble (D7–D4) of register RP select the working register group. Three system configuration registers reside in the Expanded Register File at bank FH: PCON, SMR, and WDTMR. The rest of the Expanded Register is not physically implemented and is reserved for future expansion.

Comparator Output Port 3 (D0). Bit 0 controls the comparator output in Port 3. A “1” in this location brings the comparator outputs to P34 and P37, and a “0” releases the Port to its standard I/O configuration. The default value is 0.

Port 1 Open-Drain (D1). Port 1 can be configured as an open-drain by resetting this bit (D1=0) or configured as push-pull active by setting this bit (D1=1). The default value is 1.

Port 0 Open-Drain (D2). Port 0 can be configured as an open-drain by resetting this bit (D2=0) or configured as push-pull active by setting this bit (D2=1). The default value is 1.

Low EMI Port 0 (D3). Port 0 can be configured as a Low EMI Port by resetting this bit (D3=0) or configured as a Standard Port by setting this bit (D3=1). The default value is 1.

Low EMI Port 1 (D4). Port 1 can be configured as a Low EMI Port by resetting this bit (D4=0) or configured as a Standard Port by setting this bit (D4=1). The default value is 1. **Note:** The emulator does not support Port 1 low EMI mode and must be set D4 = 1.

Low EMI Port 2 (D5). Port 2 can be configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting this bit (D5=1). The default value is 1.

Low EMI Port 3 (D6). Port 3 can be configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting this bit (D6=1). The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A “1” in this location configures the oscillator with standard drive. While a “0” configures the oscillator with low noise drive, however, it does not affect the relationship of SCLK and XTAL. The low EMI mode will reduce the drive of the oscillator (OSC). The default value is 1. **Note:** 4 MHz is the maximum external clock frequency when running in the low EMI oscillator mode.

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 31). All bits are Write Only except bit 7 which is a Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power-on cycle. Bit 6 controls whether a low or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the Stop-Mode Recovery Source. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

FUNCTIONAL DESCRIPTION (Continued)

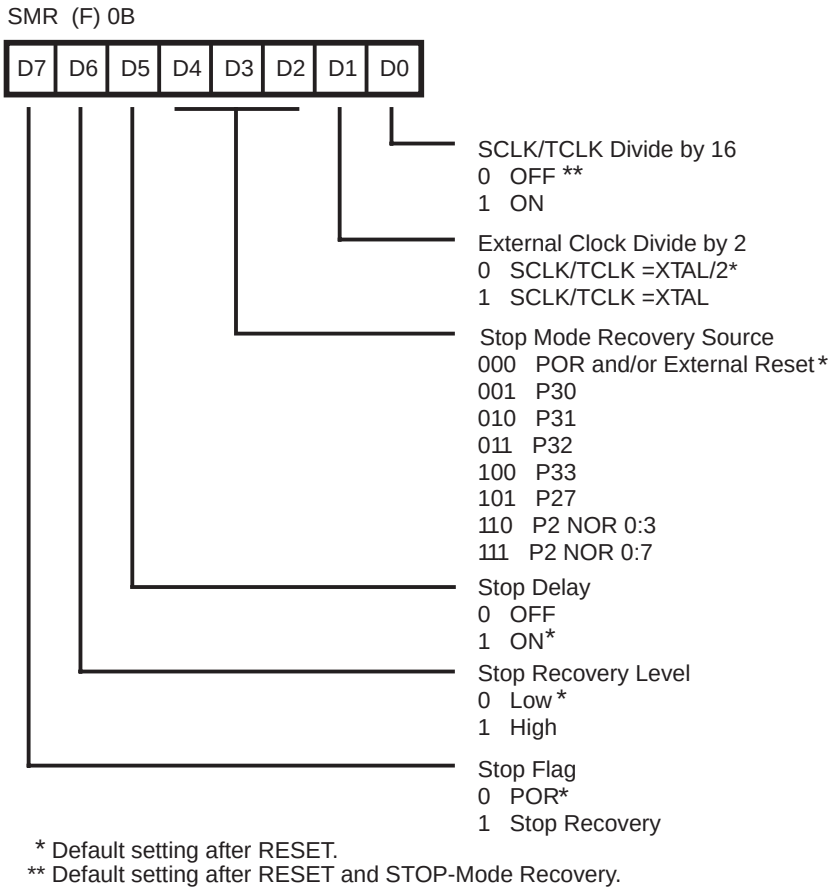
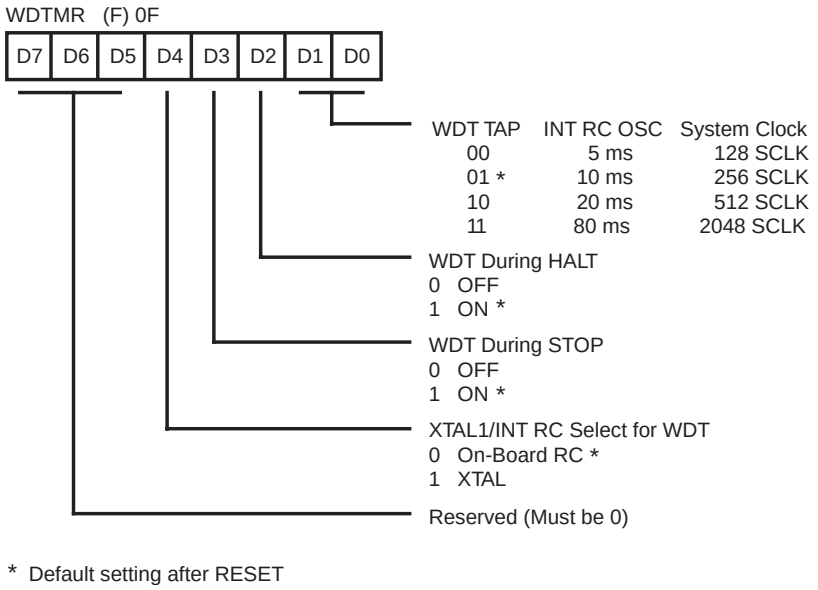


Figure 31. STOP-Mode Recovery Register (Write-Only Except Bit D7, Which is Read-Only)

cycles from the execution of the first instruction after Power-On Reset, Watch-Dog reset or a STOP-Mode Recovery (Figures 33 and 34). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH.



* Default setting after RESET

Figure 33. Watch-Dog Timer Mode Register Write Only

FUNCTIONAL DESCRIPTION (Continued)

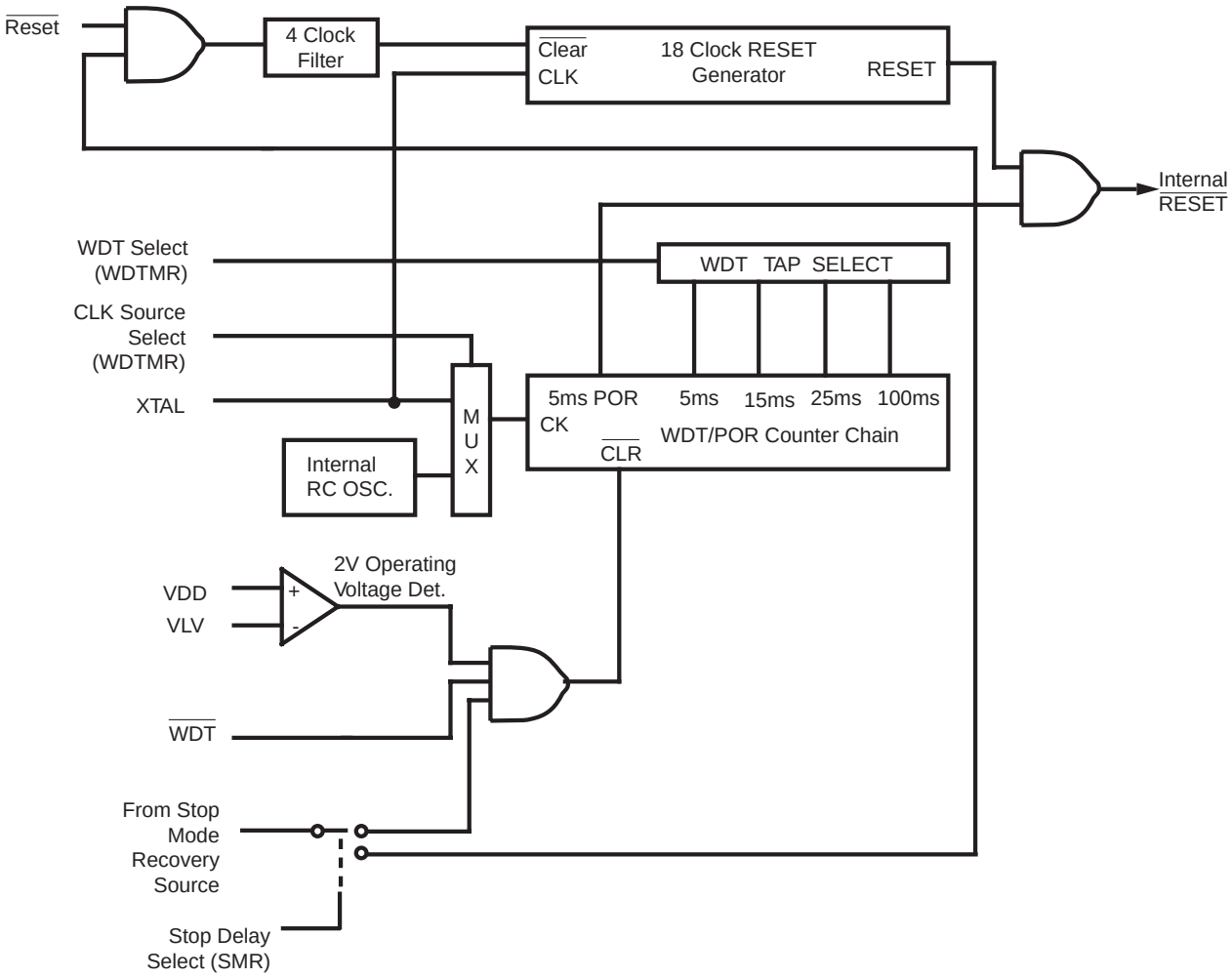


Figure 34. Resets and WDT

FUNCTIONAL DESCRIPTION (Continued)

EPROM MODE

Table 14 shows the programming voltages of each programming mode. Table 15, and figures that follow show the programming timing of each programming mode. Figure 38 shows the circuit diagram of a Z86E40 programming adapter, which adapts from 2764A to Z86E40 and Figure 39 shows the Z86E30/E31 Programming Adapter Circuitry. Figure 40 shows the flowchart of an Intelligent Programming Algorithm, which is compatible with 2764A EPROM (Z86E40 is 4K EPROM, 2764A is 8K EPROM). Since the EPROM size of Z86E30/E31/E40 differs from 2764A, the programming address range has to be set from 0000H to 0FFFH for the Z86E30/E40 and 0000H to 07FFH for Z86E31. Otherwise, the upper portion of EPROM data will overwrite the lower portion of EPROM data. Figure 39 shows the adaptation from the 2764A to Z86E30/E31.

Note: EPROM Protect feature allows the LDC, LDCI, LDE, and LDEI instructions from internal program memory. A ROM lookup table can be used with this feature.

During programming, the V_{PP} input pin supplies the programming voltage and current to the EPROM. This pin is also used to latch which EPROM mode is to be used (R/W EPROM or R/W Option bits). The mode is set by placing the correct mode number on the least significant bits of the address and raising the EPM pin above V. After a setup time, the V_{PP} pin can then be raised or lowered. The latched EPROM mode will remain until the EPM pin is reduced below V_H.

Mode Name	Mode #	LSB Addr
EPROM R/W	0	0000
Option Bit R/W	3	0011

EPROM R/W mode allows the programming of the user mode program ROM.

Option Bit R/W allows the programming of the Z8 option bits. When the device is latched into Option Bit R/W mode, the address must then be changed to 63 decimals (000000111111 Binary). The Options are mapped into this address as follows:

Bit	Option
7	Unused
6	Unused
5	32 KHz XTAL Option
4	Permanent WDT
3	Auto Latch Disable
2	RC Oscillator Option
1	RAM Protect
0	ROM Protect

Table 14 gives the proper conditions for EPROM R/W operations, once the mode is latched.

Table 14. EPROM Programming Table

Programming Modes	V_{PP}	EPM	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	ADDR	DATA	V_{CC}*
EPROM READ1	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	4.5V†
EPROM READ2	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.5V†
PROGRAM	V_H	V_H	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.4V
PROGRAM VERIFY	V_H	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.0V
OPTION BIT PGM	V_H	V_H	V_{IL}	V_{IH}	V_{IL}	63	IN	6.4V
OPTION BIT READ	X	V_H	V_{IL}	V_{IL}	V_{IH}	63	OUT	6.0V

Notes:
V_H = 13.0 V ± 0.1 V
V_{IH} = As per specific Z8 DC specification
VIL= As per specific Z8 DC specification
X=Not used, but must be set to V_H, V_{IH}, or V_{IL} level.
NU = Not used, but must be set to either V_{IH} or V_{IL} level.
I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum.
*V_{CC} has a tolerance of ±0.25V.
† Zilog recommends an EPROM read at V_{CC} = 4.5 V and 5.5 V to ensure proper device operations during the V_{CC} after programming, but V_{CC} = 5.0 V is acceptable.

Table 15. EPROM Programming Timing

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95	1.05	ms
7	Data Hold Time	2		µs
8	$\overline{OE}$ Setup Time	2		µs
9	Data Access Time	200		ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width/Option Program Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	$\overline{PGM}$ Setup Time	2		µs
14	Address to $\overline{OE}$ Setup Time	2		µs
15	$\overline{OE}$ Width	250		ns
16	Address to $\overline{OE}$ Low	125		ns

FUNCTIONAL DESCRIPTION (Continued)

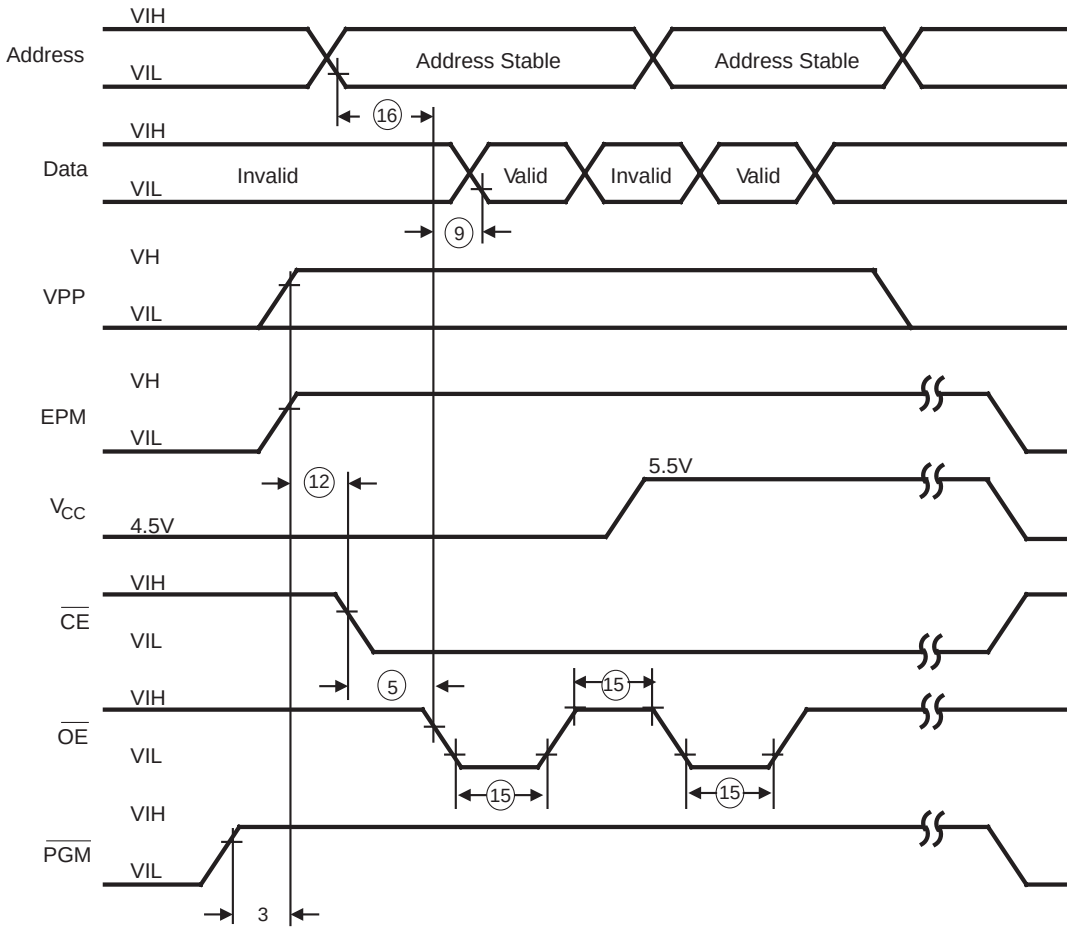


Figure 36. EPROM Read Mode Timing Diagram

Z86E40 TIMING DIAGRAMS

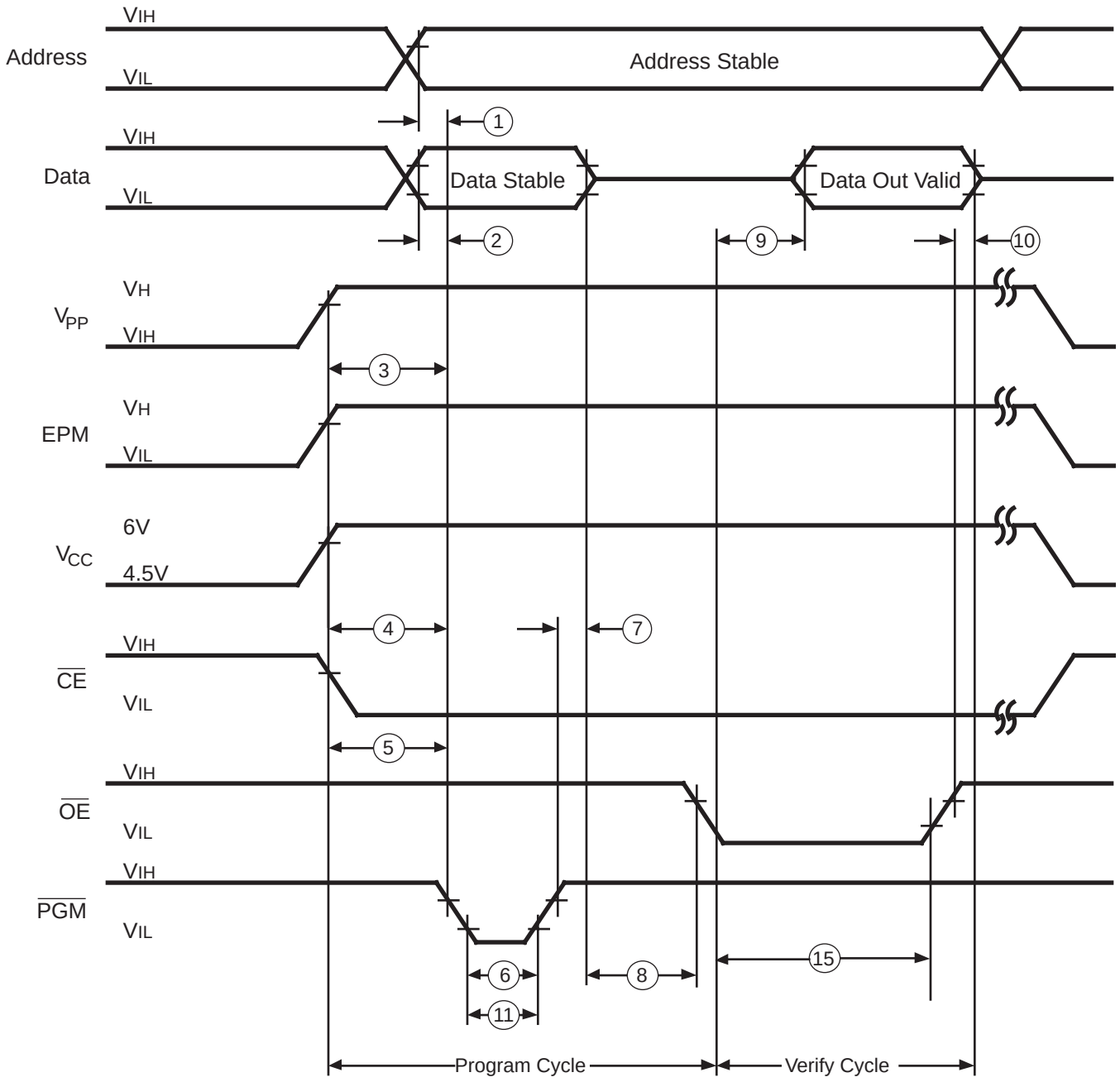


Figure 37. Timing Diagram of EPROM Program and Verify Modes

Z8 CONTROL REGISTER DIAGRAMS

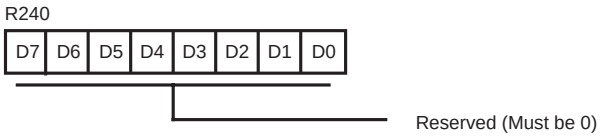


Figure 45. Reserved

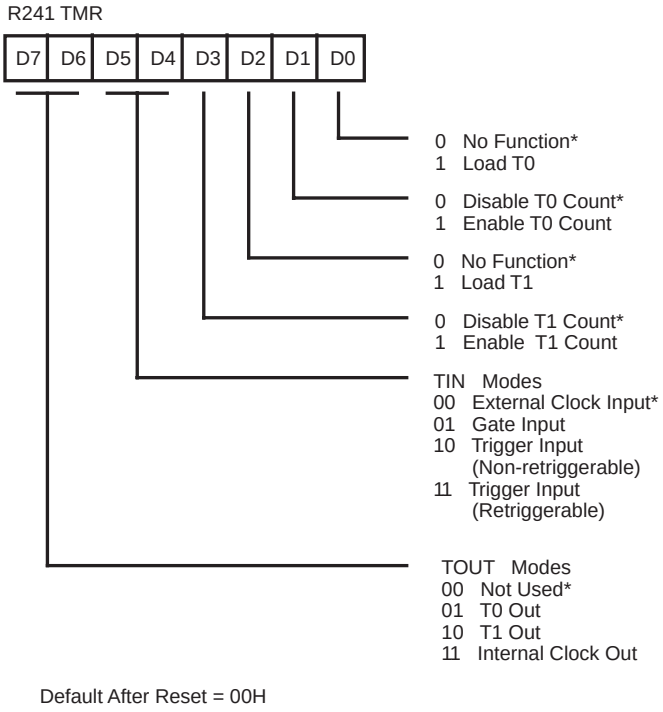


Figure 46. Timer Mode Register
F1H: Read/Write

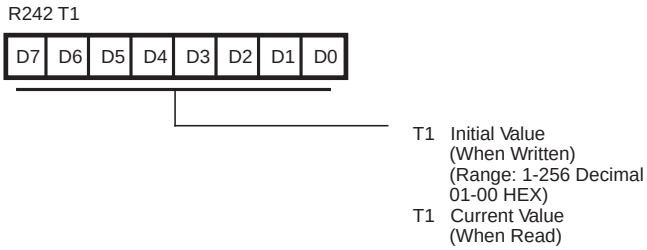


Figure 47. Counter/Timer 1 Register
F2H: Read/Write

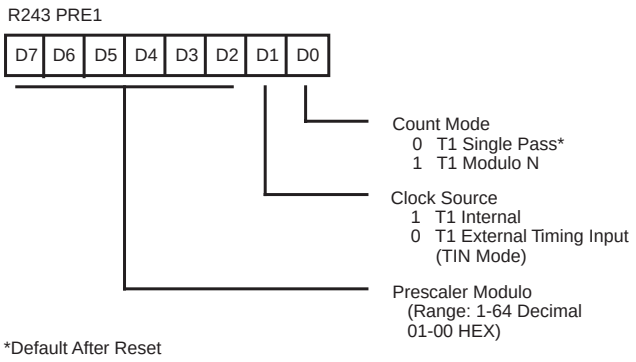


Figure 48. Prescaler 1 Register
F3H: Write Only

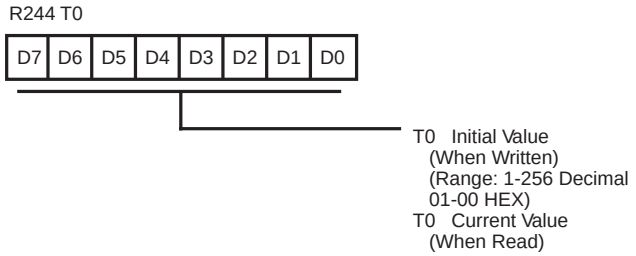


Figure 49. Counter/Timer 0 Register
F4H; Read/Write

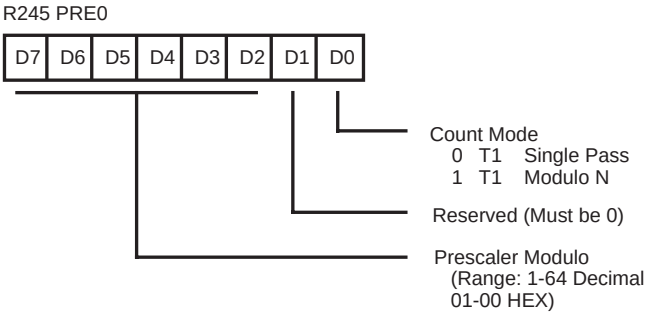


Figure 50. Prescaler 0 Register
F5H: Write Only

Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.