What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

| Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e4016fsc

PIN IDENTIFICATION
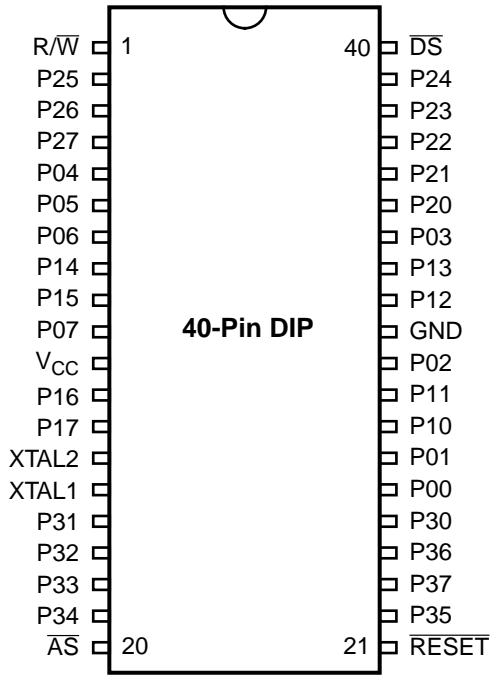
**Figure 3. 40-Pin DIP Pin Configuration
Standard Mode**

**Table 1. 40-Pin DIP Pin Identification
Standard Mode**

Pin #	Symbol	Function	Direction
1	R/$\overline{W}$	Read/Write	Output
2–4	P25–P27	Port 2, Pins 5,6,7	In/Output
5–7	P04–P06	Port 0, Pins 4,5,6	In/Output
8–9	P14–P15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V_{CC}	Power Supply	
12–13	P16–P17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal Oscillator	Output
15	XTAL1	Crystal Oscillator	Input
16–18	P31–P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	$\overline{AS}$	Address Strobe	Output
21	$\overline{RESET}$	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26–27	P00–P01	Port 0, Pins 0,1	In/Output
28–29	P10–P11	Port 1, Pins 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground	
32–33	P12–P13	Port 1, Pins 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35–39	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output
40	$\overline{DS}$	Data Strobe	Output
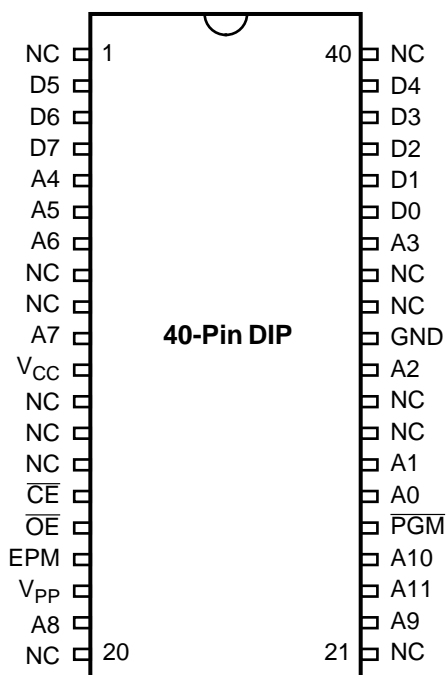
Figure 6. 40-Pin DIP Pin Configuration
EPROM Mode

Table 4. 40-Pin DIP Package Pin Identification
EPROM Mode

Pin #	Symbol	Function	Direction
1	NC	No Connection	
2–4	D5–D7	Data 5,6,7	In/Output
5–7	A4–A6	Address 4,5,6	Input
8–9	NC	No Connection	
10	A7	Address 7	Input
11	V_{CC}	Power Supply	
12–14	NC	No Connection	
15	$\overline{CE}$	Chip Select	Input
16	$\overline{OE}$	Output Enable	Input
17	EPM	EPROM Prog. Mode	Input
18	V_{PP}	Prog. Voltage	Input
19	A8	Address 8	Input
20–21	NC	No Connection	
22	A9	Address 9	Input
23	A11	Address 11	Input
24	A10	Address 10	Input
25	$\overline{PGM}$	Prog. Mode	Input
26–27	A0–A1	Address 0,1	Input
28–29	NC	No Connection	
30	A2	Address 2	Input
31	GND	Ground	
32–33	NC	No Connection	
34	A3	Address 3	Input
35–39	D0–D4	Data 0,1,2,3,4	In/Output
40	NC	No Connection	

PIN IDENTIFICATION (Continued)

```
        ┌────────┐
P25  1  │        │  28  P24
P26     │        │      P23
P27     │        │      P22
P04     │        │      P21
P05     │        │      P20
P06     │        │      P03
P07     │ 28-Pin │      V_SS
V_CC    │  DIP   │      P02
XTAL2   │        │      P01
XTAL1   │        │      P00
P31     │        │      P30
P32     │        │      P36
P33     │        │      P37
P34  14 │        │  15  P35
        └────────┘
```
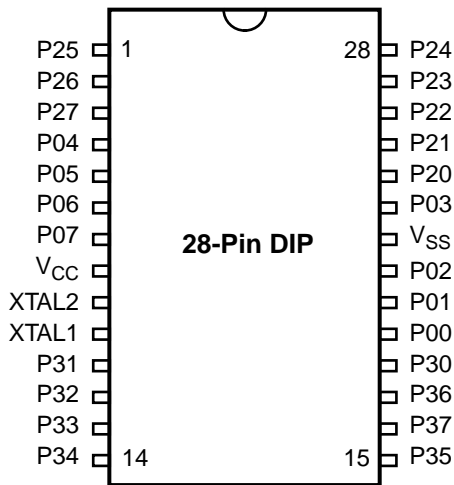
**Figure 9. Standard Mode
28-Pin DIP/SOIC Pin Configuration**

```
        ┌────────┐
D5   1  │        │  28  D4
D6      │        │      D3
D7      │        │      D2
A4      │        │      D1
A5      │        │      D0
A6      │        │      A3
A7      │ 28-Pin │      V_SS
V_CC    │  DIP   │      A2
NC      │        │      A1
CE      │        │      A0
OE      │        │      PGM
EPM     │        │      A10
V_PP    │        │      A11
A8   14 │        │  15  A9
        └────────┘
```
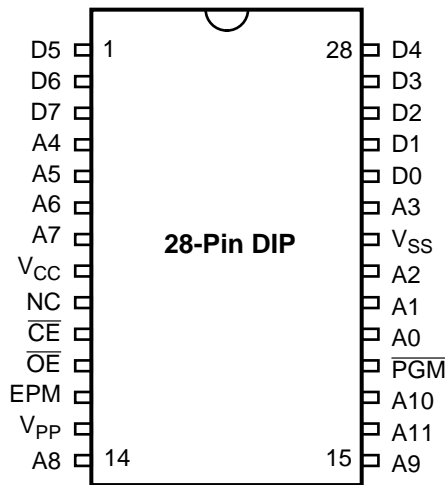
**Figure 10. EPROM Programming Mode
28-Pin DIP/SOIC Pin Configuration**

**Table 7. 28-Pin DIP/SOIC/PLCC
Pin Identification***

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Pins 5,6,	In/Output
4–7	P04–P07	Port 0, Pins 4,5,6,7	In/Output
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11–13	P31–P33	Port 3, Pins 1,2,3	Input
14–15	P34–P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19–21	P00–P02	Port 0, Pins 0,1,2	In/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24–28	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output

```
           P04 P27 P26 P25 P24 P23 P22
            │   │   │   │   │   │   │
           ┌─────────────────────────┐
          /  4       1          26    \
P05   5  │                          25 │  P21
P06      │                             │  P20
P07      │                             │  P03
V_CC     │        28-Pin PLCC          │  V_SS
XT2      │                             │  P02
XT1      │                             │  P01
P31  11  │ 12                    19    │  P00
          \         18               /
           └─────────────────────────┘
            │   │   │   │   │   │   │
           P32 P33 P34 P35 P37 P36 P30
```
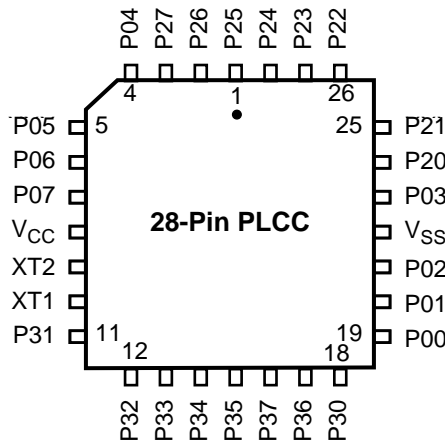
**Figure 11. Standard Mode
28-Pin PLCC Pin Configuration**

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	−40	+105	C
Storage Temperature	−65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	−0.6	+7	V
Voltage on V_{DD} Pin with Respect to V_{SS}	−0.3	+7	V
Voltage on XTAL1 and $\overline{RESET}$ Pins with Respect to V_{SS} [Note 2]	−0.6	V_{DD}+1	V
Total Power Dissipation		1.21	W
Maximum Allowable Current out of V_{SS}		220	mA
Maximum Allowable Current into V_{DD}		180	mA
Maximum Allowable Current into an Input Pin [Note 3]	−600	+600	µA
Maximum Allowable Current into an Open-Drain Pin [Note 4]	−600	+600	µA
Maximum Allowable Output Current Sinked by Any I/O Pin		25	mA
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA
Maximum Allowable Output Current Sinked by $\overline{RESET}$ Pin		3 mA	

Notes:
1. This applies to all pins except XTAL pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 1.2 W for the package. Power dissipation is calculated as follows:

Total Power Dissipation = V_{DD} x [I_{DD} − (sum of I_{OH})]
+ sum of [(V_{DD} − V_{OH}) x I_{OH}]
+ sum of (V_{0L} x I_{0L})

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Test Load).
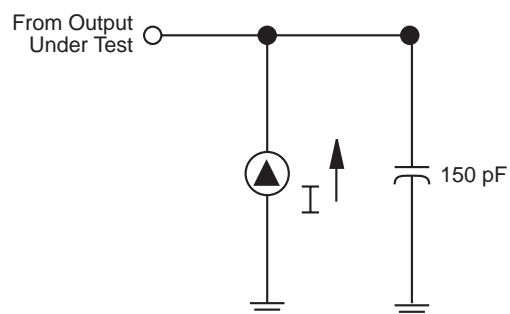

Figure 13. Test Load Diagram

T_A=–40 °C to +105 °C

Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	$0.7\,V_{CC}$	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
		5.5V	$0.7\,V_{CC}$	V_{CC}+0.3	2.5	V		
V_{CL}	Clock Input Low Voltage	4.5V	GND-0.3	$0.2\,V_{CC}$	1.5	V	Driven by External Clock Generator	
		5.5V	GND-0.3	$0.2\,V_{CC}$	1.5	V		
V_{IH}	Input High Voltage	4.5V	$0.7\,V_{CC}$	V_{CC}+0.3	2.5	V		
		5.5V	$0.7\,V_{CC}$	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	4.5V	GND-0.3	$0.2\,V_{CC}$	1.5	V		
		5.5V	GND-0.3	$0.2\,V_{CC}$	1.5	V		
V_{OH}	Output High Voltage Low EMI Mode	4.5V	V_{CC} -0.4		4.8	V	I_{OH} = – 0.5 mA	8
		5.5V	V_{CC} -0.4		4.8	V	I_{OH} = – 0.5 mA	8
V_{OH1}	Output High Voltage	4.5V	V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	8
		4.5V	V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	8
V_{OL}	Output Low Voltage Low EMI Mode	4.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
		5.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = + 4.0 mA	8
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	8
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I_{OL} = + 12 mA	8
		5.5V		1.2	0.5	V	I_{OL} = + 12 mA	8
V_{RH}	Reset Input High Voltage	3.5V	$.8\,V_{CC}$	V_{CC}	1.7	V		13
		5.5V	$.8\,V_{CC}$	V_{CC}	2.1	V		13
V_{OLR}	Reset Output Low Voltage	3.5V		0.6	0.3	V	I_{OL} = 1.0 mA	13
		5.5V		0.6	0.2	V	I_{OL} = 1.0 mA	13
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25	10	mV		
		5.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	4.5V	0	V_{CC}-1.5V		V		10
		5.5V	0	V_{CC}-1.5V		V		10
I_{IL}	Input Leakage	4.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	4.5V	-18	-180	-112	µA		
		5.5V	-18	-180	-112	µA		
I_{CC}	Supply Current	4.5V		25	20	mA	@ 16 MHz	4,5
		5.5V		25	20	mA	@ 16 MHz	4,5
I_{CC1}	Standby Current Halt Mode	4.5V		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4,5
		5.5V		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4,5
I_{CC2}	Standby Current (Stop Mode)	4.5V		10	2	µA	V_{IN} = 0V, V_{CC}	6,11,14
		5.5V		10	3	µA	V_{IN} = 0V, V_{CC}	6,11,14
I_{ALL}	Auto Latch Low Current	4.5V	1.4	20	4.7	µA	0V < V_{IN} < V_{CC}	9
		5.5V	1.4	20	4.7	µA	0V < V_{IN} < V_{CC}	9
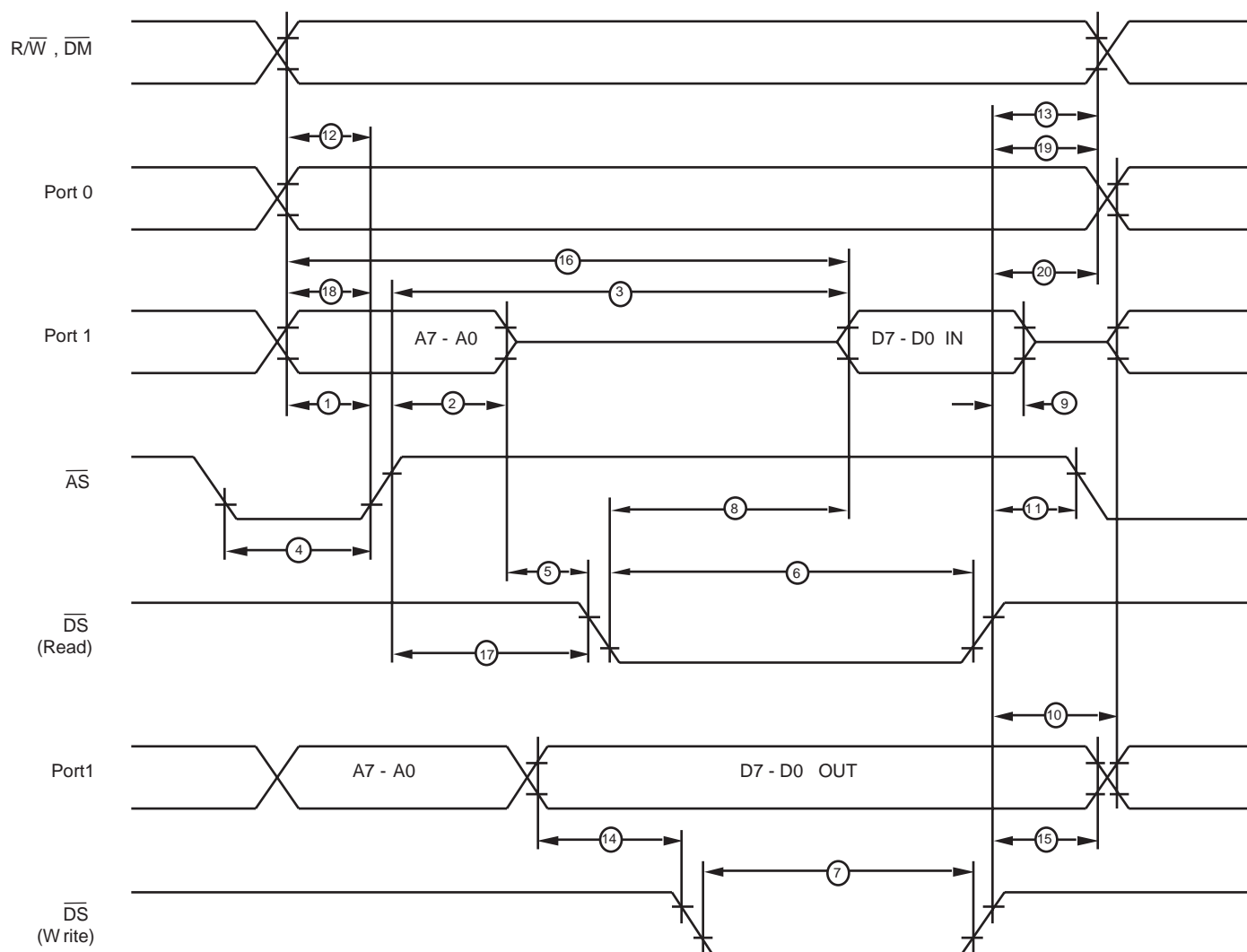
Figure 14. External I/O or Memory Read/Write Timing
Z86E40 Only

No	Symbol	Parameter	V_{CC} Note [3]	Min	Max	Units	Notes
			TA = -40°C to 105°C				
			16 MHz				
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	4.5V	25		ns	2
			5.5V	25		ns	
2	TdAS(A)	$\overline{AS}\overline{AS}$ Rise to Address Float Delay	4.5V	35		ns	2
			5.5V	35		ns	
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	4.5V		180	ns	1,2
			5.5V		180	ns	
4	TwAS	$\overline{AS}$ Low Width	4.5V	40		ns	2
			5.5V	40		ns	
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	4.5V	0		ns	
			5.5V	0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	4.5V	135		ns	1,2
			5.5V	135		ns	
7	TwDSW	$\overline{DS}$ (Write) Low Width	4.5V	80		ns	1,2
			5.5V	80		ns	
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid	4.5V		75	ns	1,2
			5.5V		75	ns	
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	4.5V	0		ns	2
			5.5V	0		ns	
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	4.5V	50		ns	2
			5.5V	50		ns	
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	4.5V	35		ns	2
			5.5V	35		ns	
12	TdR/W(AS)	$R/\overline{W}$ Valid to $\overline{AS}$ Rise Delay	4.5V	25		ns	2
			5.5V	25		ns	
13	TdDS(R/W)	$\overline{DS}$ Rise to $R/\overline{W}$ Not Valid	4.5V	35		ns	2
			5.5V	35		ns	
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	4.5V	55	25	ns	2
			5.5V	55	25	ns	
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	4.5V	35		ns	2
			5.5V	35		ns	
16	TdA(DR)	Address Valid to Read Data Req'd Valid	4.5V		230	ns	1,2
			5.5V		230	ns	
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	4.5V	45		ns	2
			5.5V	45		ns	
18	TdDM(AS)	/DM Valid to $\overline{AS}$ Fall Delay	4.5V	30		ns	2
			5.5V	30		ns	
20	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	4.5V	35		ns	
			5.5V	35		ns	

Notes:
1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.
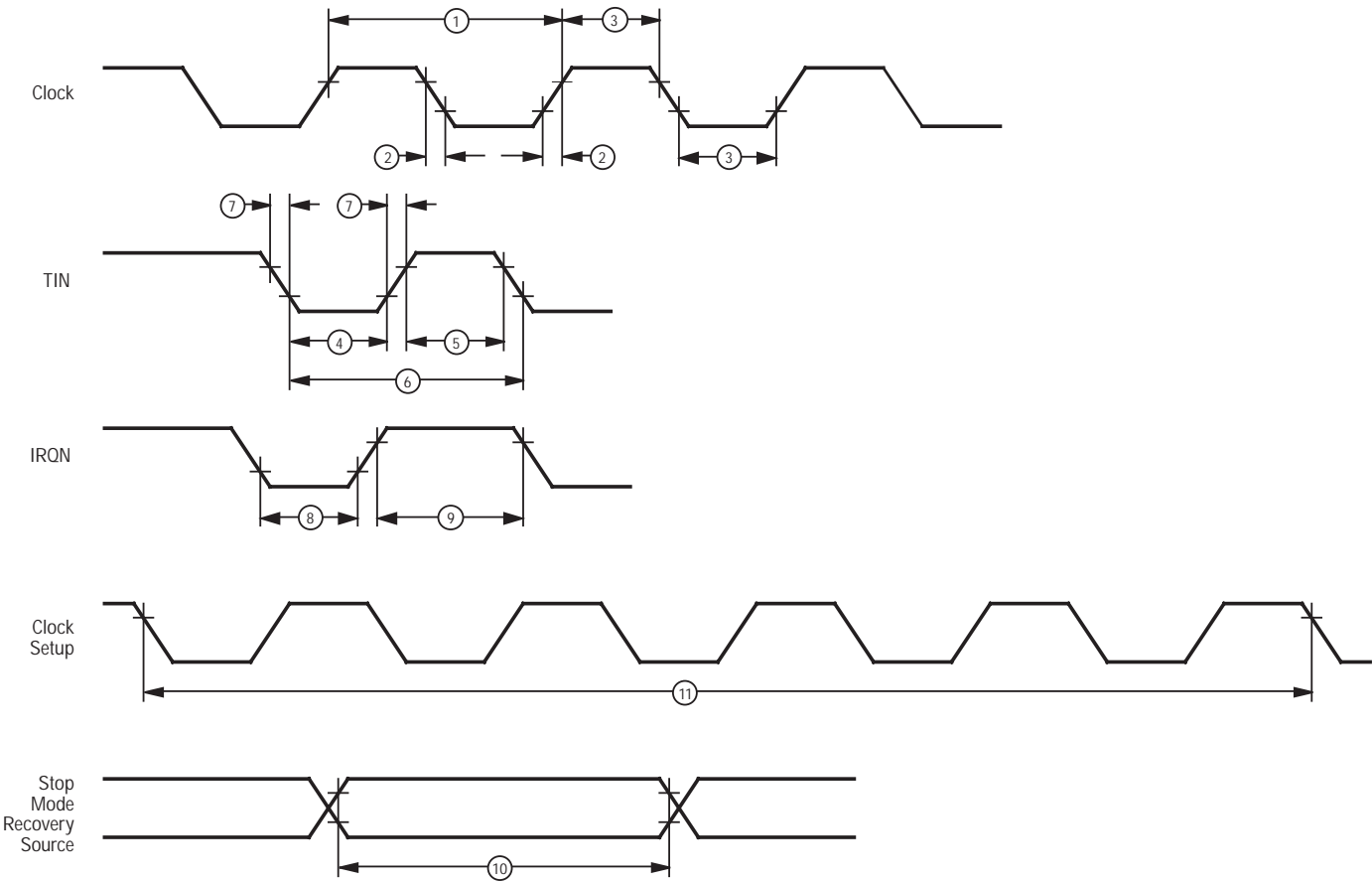
DC ELECTRICAL CHARACTERISTICS (Continued)

Figure 15. Additional Timing Diagram

DC ELECTRICAL CHARACTERISTICS (Continued)
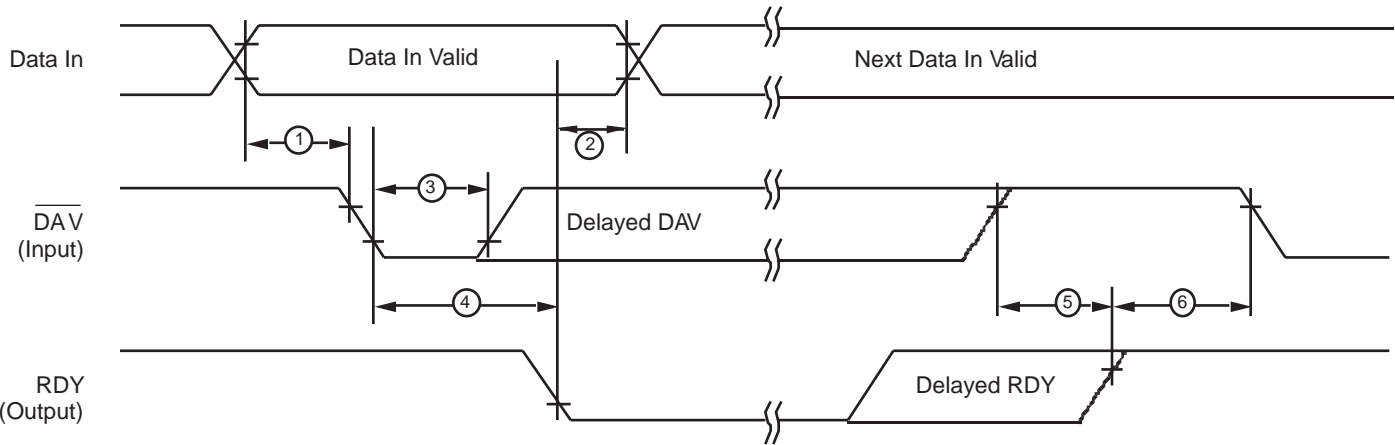
Handshake Timing Diagrams

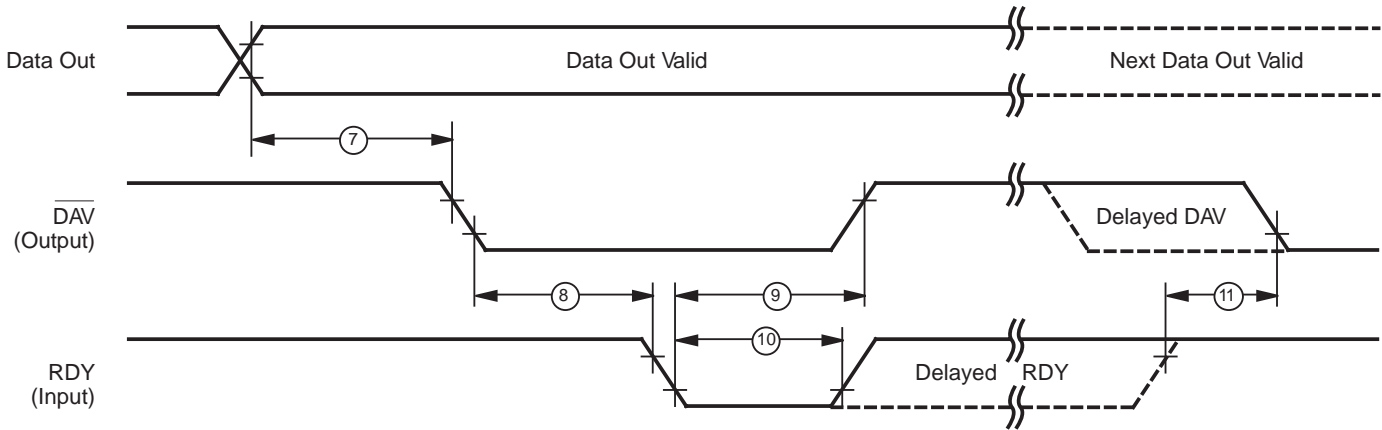**Figure 16. Input Handshake Timing**

Figure 17. Output Handshake Timing

PIN FUNCTIONS (Continued)

Port 1 (P17–P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7–A0) and Data (D7–D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls

RDY1 and /DAV1 (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (Figure 19).

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z86E40 to share common resources in multiprocessor and DMA applications.
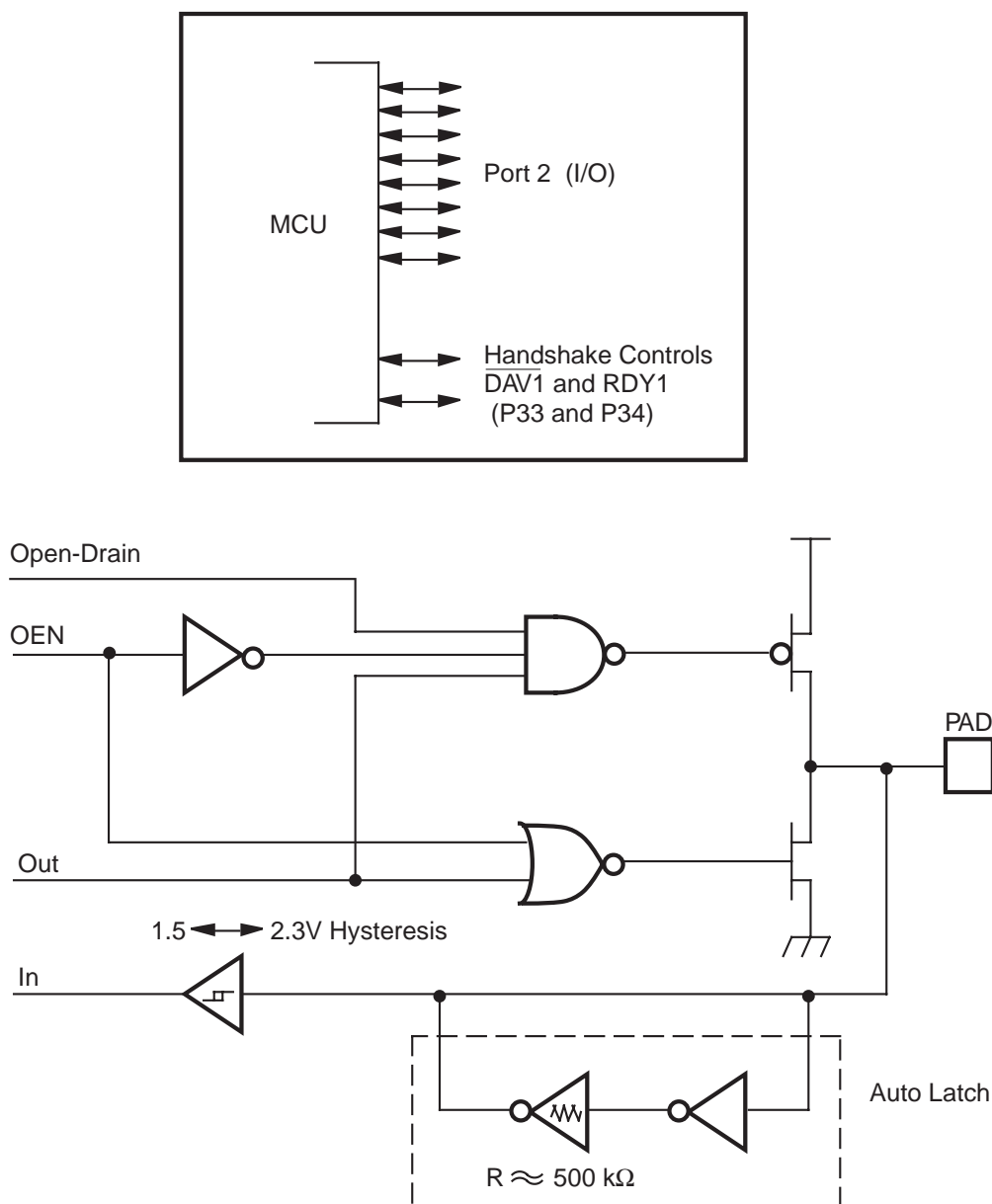

Figure 19. Port 1 Configuration (Z86E40 Only)

Port 2 (P27–P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control.

In Handshake Mode, Port 3 lines P31 and P36 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2 (Figure 20).
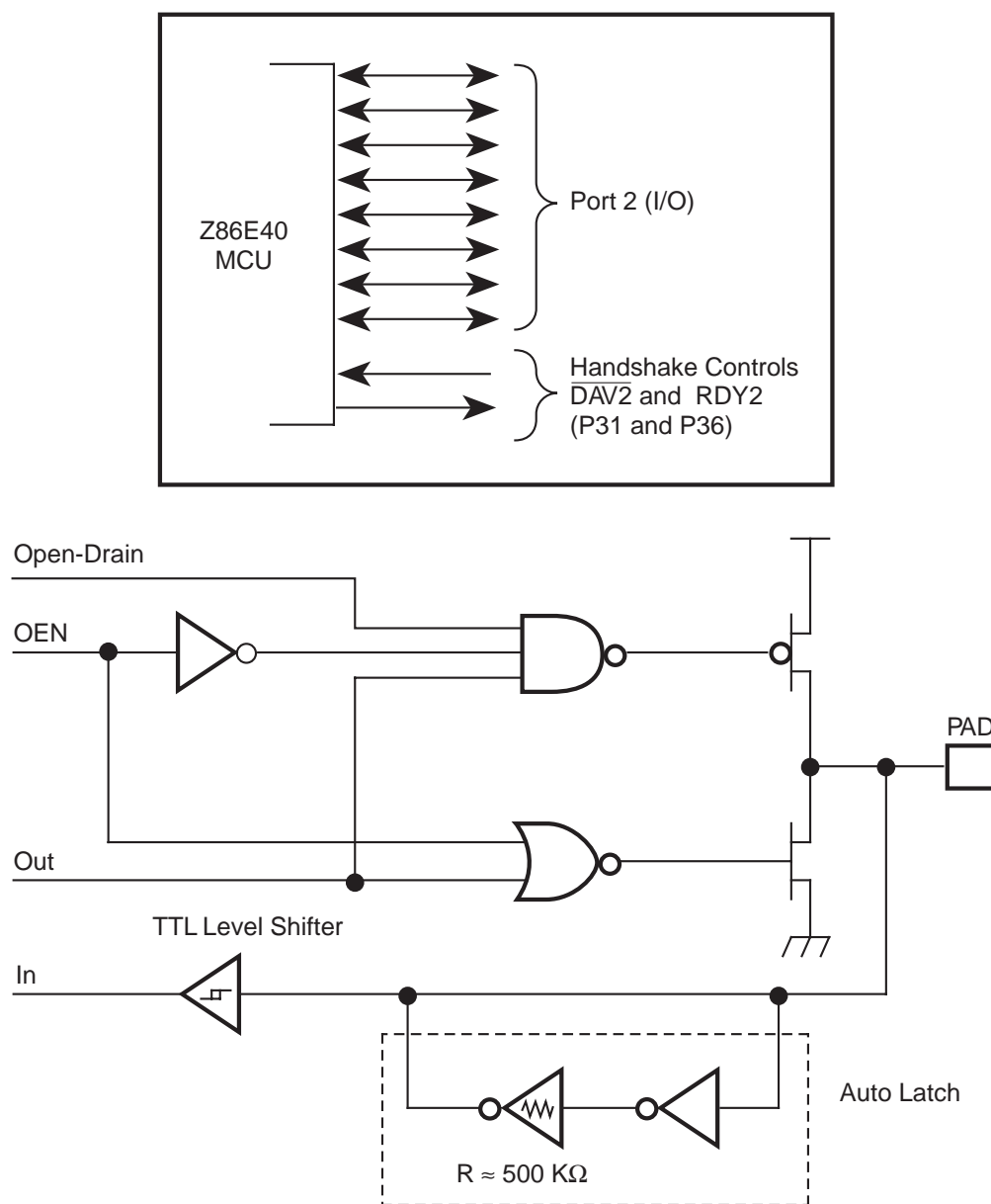
Figure 20. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37–P30). Port 3 is an 8-bit, CMOS-compatible port with four fixed inputs (P33–P30) and four fixed outputs (P37–P34). These eight lines can be configured by software for interrupt and handshake control functions. Port 3, Pin 0 is Schmitt- triggered. P31, P32, and P33 are standard CMOS inputs with single trip point (no Auto Latches) and P34, P35, P36, and P37 are push-pull output lines. Low EMI output buffers can be globally programmed by the software. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by setting the D1 of Port 3 Mode Register (P3M). The comparator output can be outputted from P34 and P37, respectively, by setting PCON register Bit D0 to 1 state. For the interrupt function, P30 and P33 are falling edge triggered interrupt inputs. P31 and P32 can be programmed as falling, rising or both edges triggered interrupt inputs (Figure 21). Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Port 0, Port 1, and Port 2 are also available on Port 3 (Table 9).

Note: When enabling/ or disabling analog mode, the following is recommended:

1. Allow two NOP delays before reading this comparator output.

2. Disable global interrupts, switch to analog mode, clear interrupts, and then re-enable interrupts.

3. IRQ register bits 3 to 0 must be cleared after enabling analog mode.

Note: P33–P30 differs from the Z86C30/C31/C40 in that there is no clamping diode to V_{CC} due to the EPROM high-voltage circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode.

FUNCTIONAL DESCRIPTION (Continued)

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status

2. Stop-Mode Recovery (if D5 of SMR=0)

3. WDT time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP mode Register (SMR) determines whether the POR timer is bypassed after STOP-Mode Recovery (typical for an external clock and RC/LC oscillators with fast start up times).

HALT. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (Opcode=FFH) immediately before the appropriate sleep instruction, that is:

FF	NOP	; clear the pipeline
6F	STOP	; enter STOP Mode
	or	
FF	NOP	; clear the pipeline
7F	HALT	; enter HALT Mode

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. STOP Mode is terminated by one of the following resets: either by WDT time-out, POR, a Stop-Mode Recovery Source, which is defined by the SMR register or external reset. This causes the processor to restart the application program at address 000CH.

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2 and 3, and low EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00 (Figure 30).
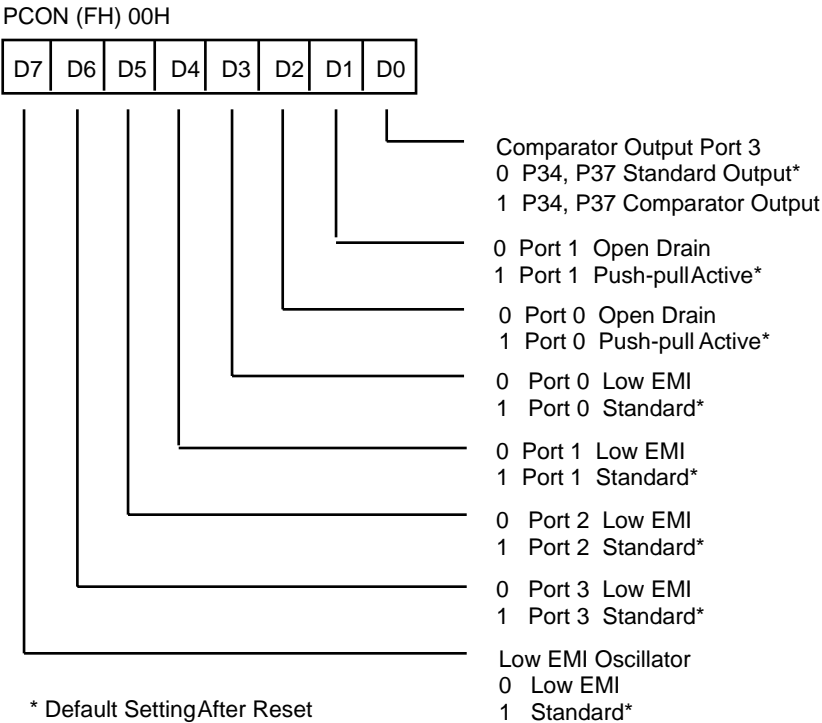

Figure 30. Port Configuration Register (PCON)
(Write Only)

FUNCTIONAL DESCRIPTION (Continued)

Table 12. Stop-Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0–3
1	1	1	Logical NOR of Port 2 bits 0–7

Stop-Mode Recovery Delay Select (D5). The 5 ms RESET delay after Stop-Mode Recovery is disabled by programming this bit to a zero. A "1" in this bit will cause a 5 ms RESET delay after Stop-Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the Stop-Mode Recovery source needs to be kept active for at least 5TpC.

Stop-Mode Recovery Level Select (D6). A "1" in this bit defines that a high level on any one of the recovery sources wakes the MCU from STOP Mode. A 0 defines low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A "0" in this bit indicates that the device has been reset by POR (cold). A "1" in this bit indicates the device was awakened by a SMR source (warm).

Stop-Mode Recovery Register 2 (SMR2). This register contains additional Stop-Mode Recovery sources. When the Stop-Mode Recovery sources are selected in this register then SMR Register. Bits D2, D3, and D4 must be 0.

SMR:10		Operation
D1	**D0**	**Description of Action**
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is disabled after Power-On Reset and initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT is driven either by an on-board RC oscillator or an external oscillator from XTAL1 pin. The

POR clock source is selected with bit 4 of the WDT register.

Note: Execution of the WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags.

WDT Time-Out Period (D0 and D1). Bits 0 and 1 control a tap circuit that determines the time-out periods that can be obtained (Table 13). The default value of D0 and D1 are 1 and 0, respectively.

Table 13. Time-out Period of WDT

D1	D0	Time-out of the Internal RC OSC	Time-out of the System Clock
0	0	5 ms	128 SCLK
0	1	10 ms*	256 SCLK*
1	0	20 ms	512 SCLK
1	1	80 ms	2048 SCLK

Notes:
 *The default setting is 10 ms.

WDT During HALT Mode (D2). This bit determines whether or not the WDT is active during HALT Mode. A "1" indicates that the WDT is active during HALT. A "0" disables the WDT in HALT Mode. The default value is "1".

WDT During STOP Mode (D3). This bit determines whether or not the WDT is active during STOP mode. A "1" indicates active during STOP. A "0" disables the WDT during STOP Mode. This is applicable only when the WDT clock source is the internal RC oscillator.

Clock Source For WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1, and the WDT is stopped in STOP Mode. The default configuration of this bit is 0, which selects the RC oscillator.

Permanent WDT. When this feature is enabled, the WDT is enabled after reset and will operate in Run and Halt Mode. The control bits in the WDTMR do not affect the WDT operation. If the clock source of the WDT is the internal RC oscillator, then the WDT will run in STOP mode. If the clock source of the WDT is the XTAL1 pin, then the WDT will not run in STOP mode.

Note: WDT time-out in STOP Mode will not reset SMR,SMR2,PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers.

WDTMR Register Accessibility. The WDTMR register is accessible only during the **first 60** internal system clock
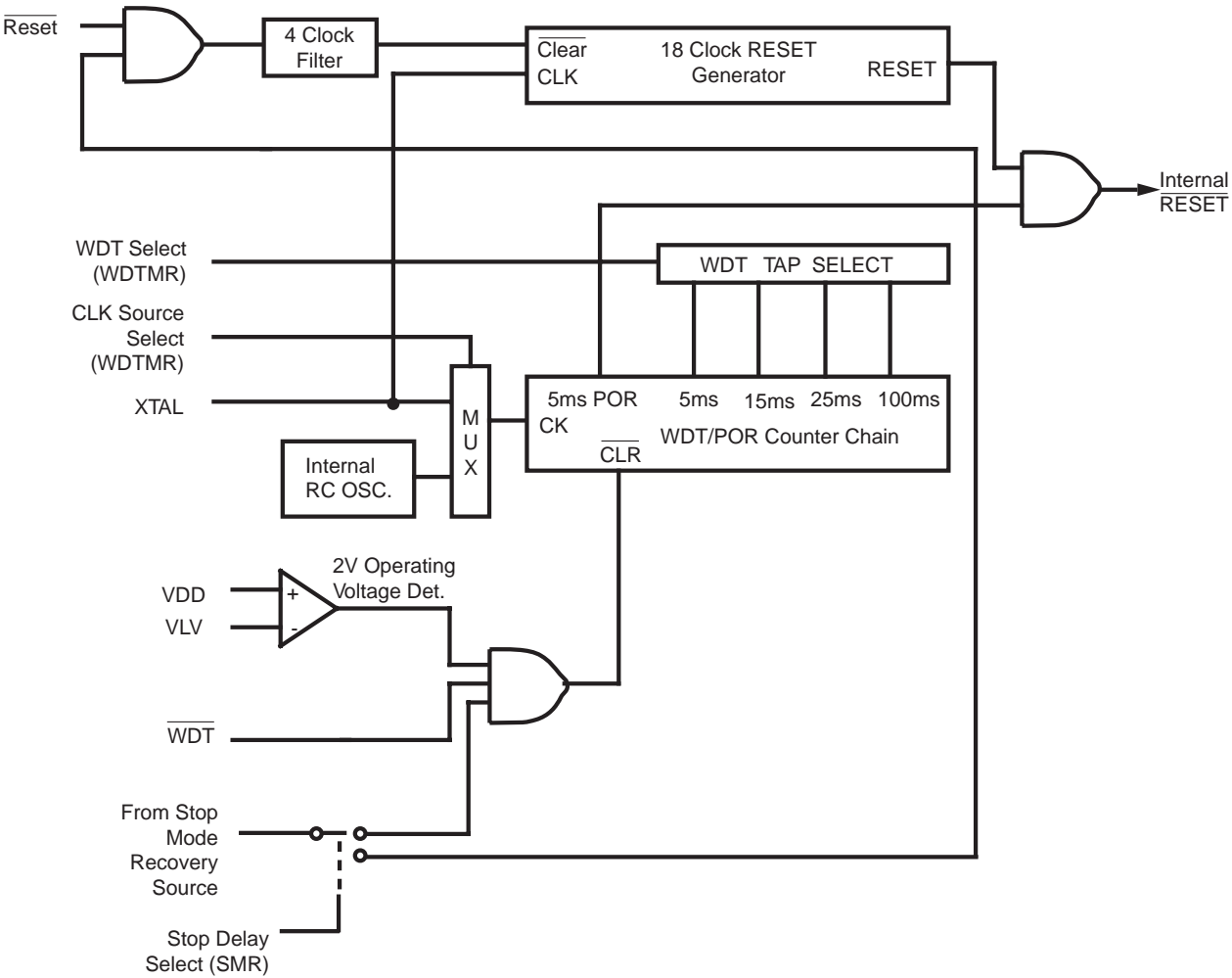
FUNCTIONAL DESCRIPTION (Continued)

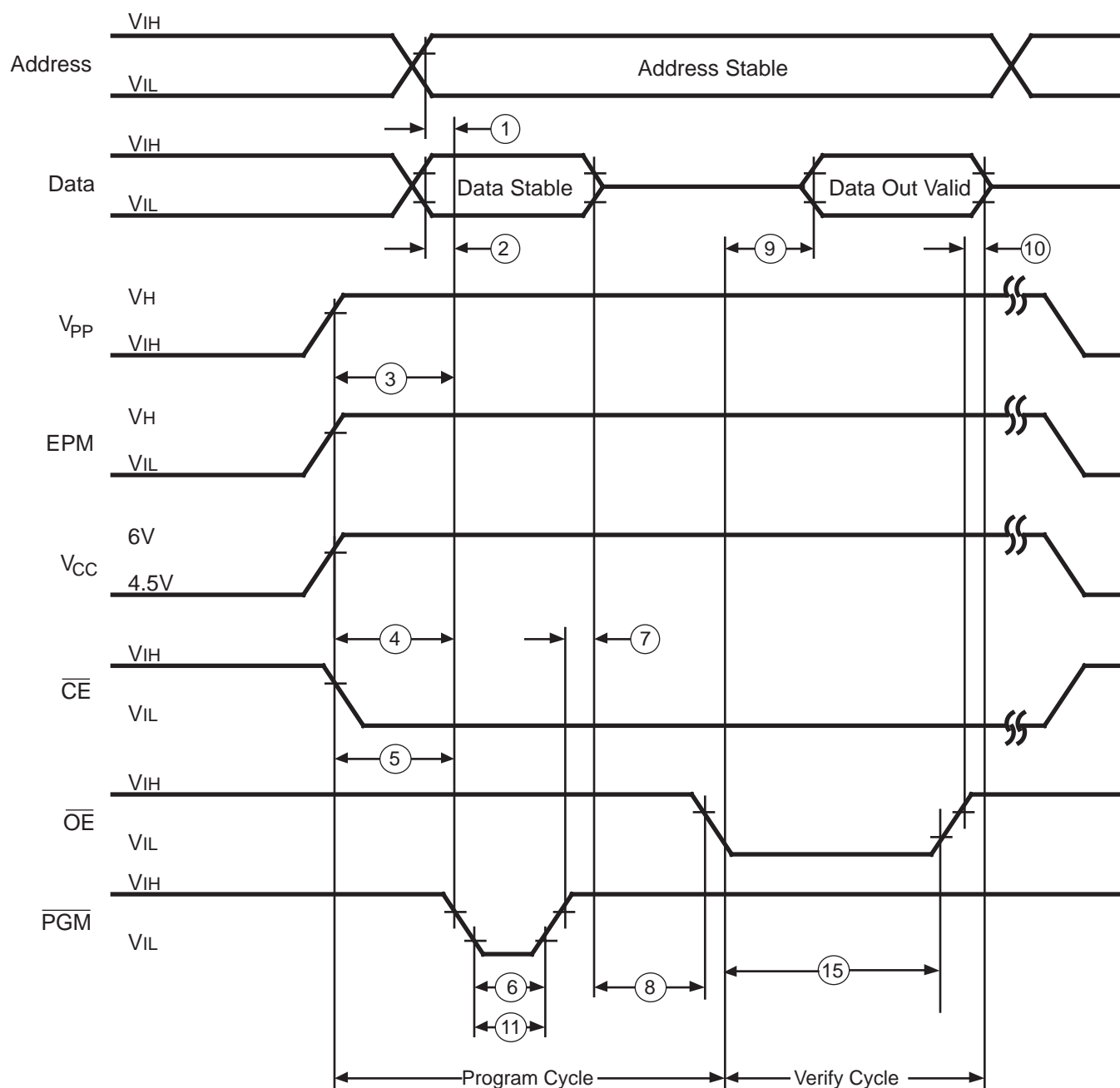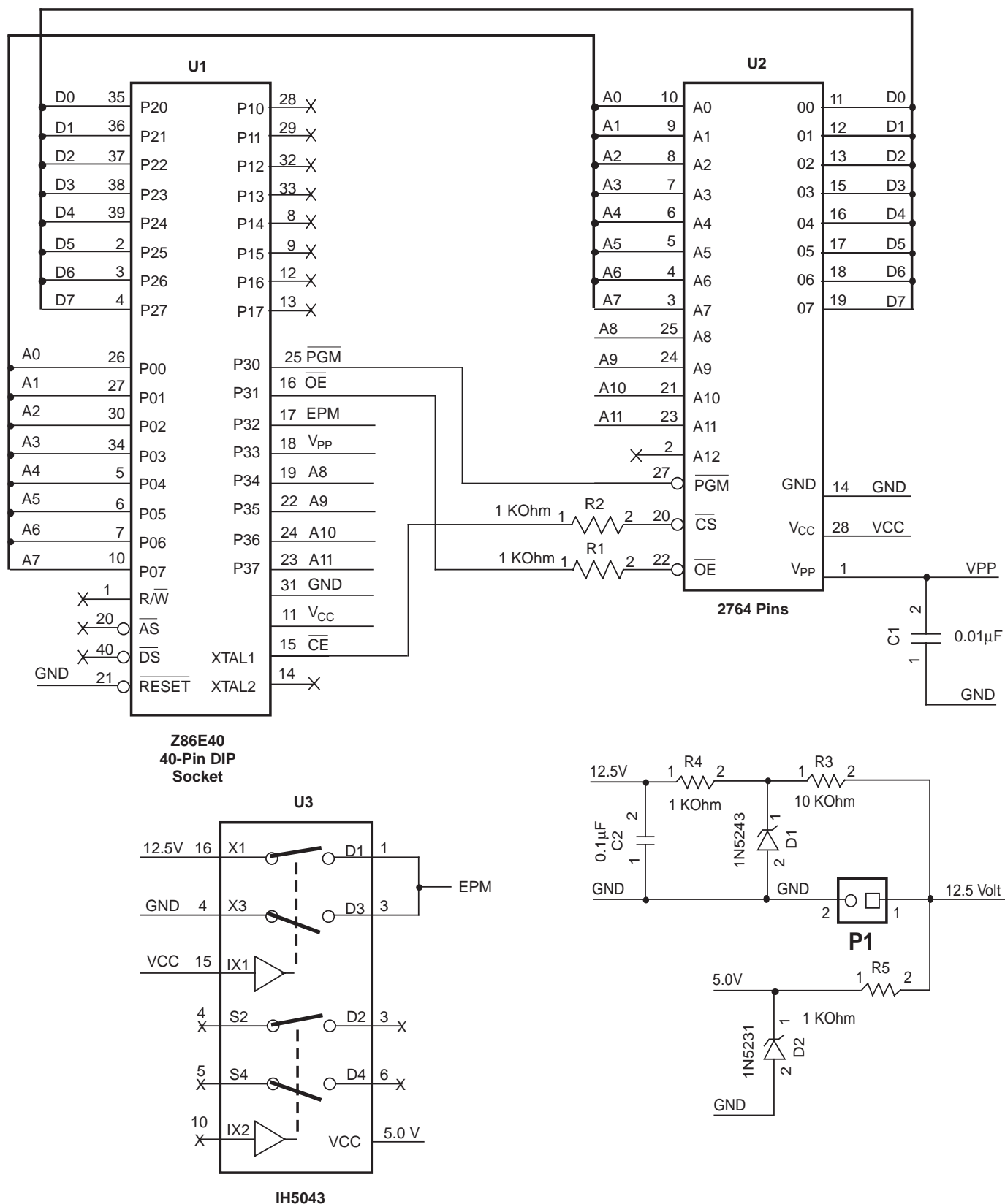**Figure 34. Resets and WDT**

Z86E40 TIMING DIAGRAMS

Figure 37. Timing Diagram of EPROM Program and Verify Modes

Z86E40 TIMING DIAGRAMS (Continued)

Figure 38. Z86E40 Z8 OTP Programming Adapter
For use with Standard EPROM Programmers
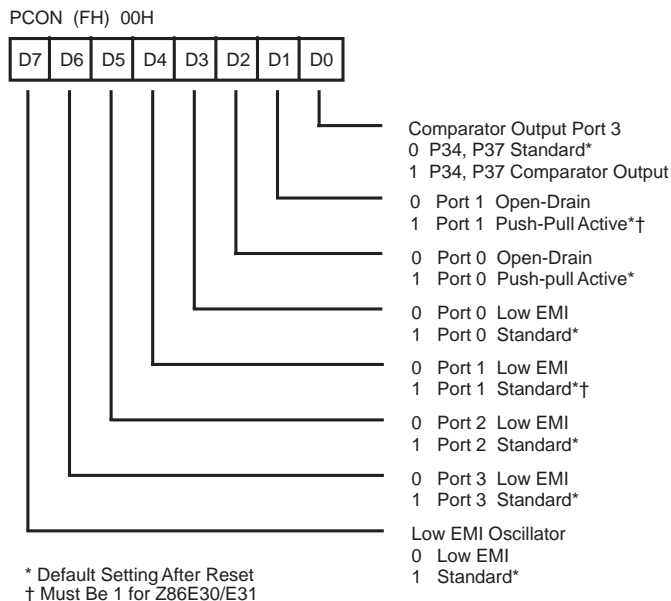
EXPANDED REGISTER FILE CONTROL REGISTERS

PCON (FH) 00H

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Comparator Output Port 3
0 P34, P37 Standard*
1 P34, P37 Comparator Output

0 Port 1 Open-Drain
1 Port 1 Push-Pull Active*†

0 Port 0 Open-Drain
1 Port 0 Push-pull Active*

0 Port 0 Low EMI
1 Port 0 Standard*

0 Port 1 Low EMI
1 Port 1 Standard*†

0 Port 2 Low EMI
1 Port 2 Standard*

0 Port 3 Low EMI
1 Port 3 Standard*

Low EMI Oscillator
0 Low EMI
1 Standard*

* Default Setting After Reset
† Must Be 1 for Z86E30/E31

Figure 41. Port Configuration Register
Write Only

SMR (FH) 0B

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

SCLK/TCLK Divide-by-16
0 OFF **
1 ON

External Clock Divide by 2
0 SCLK/TCLK =XTAL/2*
1 SCLK/TCLK =XTAL

Stop Mode Recovery Source
 000 POR Only and/or External Reset*
 001 P30
 010 P31
 011 P32
 100 P33
 101 P27
 110 P2 NOR 0-3
 111 P2 NOR 0-7

Stop Delay
0 OFF
1 ON*

Stop Recovery Level
0 Low*
1 High

Stop Flag
0 POR*
1 Stop Recovery

* Default setting after RESET.
** Default setting after RESET and STOP-Mode Recovery.

Figure 42. STOP-Mode Recovery Register
Write Only Except Bit D7, Which is Read Only

WDTMR (F) 0F

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

WDT TAP	INT RC OSC	System Clock
00	5 ms	128 SCLK
01 *	10 ms	256 SCLK
10	20 ms	512 SCLK
11	80 ms	2048 SCLK

WDT During HALT
0 OFF
1 ON *

WDT During STOP
0 OFF
1 ON *

XTAL1/INT RC Select for WDT
0 On-Board RC *
1 XTAL

Reserved (Must be 0)

* Default setting after RESET

Figure 43. Watch-Dog Timer Mode Register
Write Only

SMR2 (0F) DH

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Stop-Mode Recovery Source 2
00 POR only*
01 AND P20,P21,P22,P23
10 AND P20,P21,P22,P23,P24,
     P25,P26,P27

Reserved (Must be 0)

Note: Not used in conjunction with SMR Source

Figure 44. STOP-Mode Recovery Register 2
Write Only

R250 IRQ

D7	D6	D5	D4	D3	D2	D1	D0

IRQ0 = P32 Input
IRQ1 = P33 Input
IRQ2 = P31 Input
IRQ3 = P30 Input
IRQ4 = T0
IRQ5 = T1

Inter Edge
P31 ↓ P32 ↓ = 00
P31 ↓ P32 ↑ = 01
P31 ↑ P32 ↓ = 10
P31 ↑↓ P32 ↑↓ = 11

Default After Reset = 00H
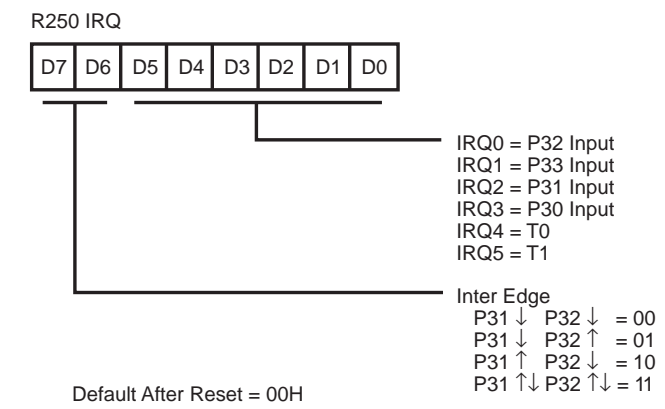
Figure 55. Interrupt Request Register
FAH: Read/Write

R251 IMR

D7	D6	D5	D4	D3	D2	D1	D0

1 Enables IRQ5-IRQ0
   (D0 = IRQ0)

1 Enables RAM Protect †

1 Enables Interrupts

† This option must be selected when ROM code is
submitted for ROM Masking, otherwise this control bit
is disabled permanently.
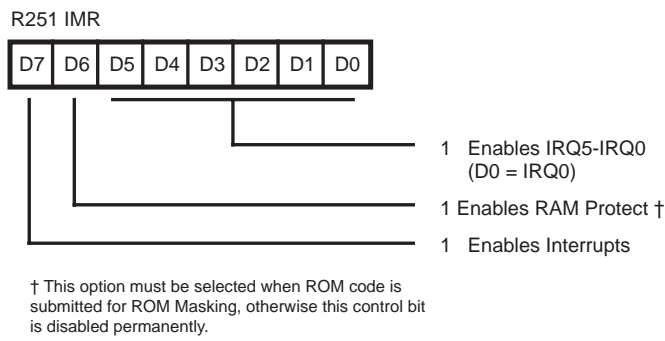
Figure 56. Interrupt Mask Register
FBH: Read/Write

R252 FLAGS

D7	D6	D5	D4	D3	D2	D1	D0

User Flag F1

User Flag F2

Half Carry Flag

Decimal Adjust Flag

Overflow Flag

Sign Flag

Zero Flag

Carry Flag
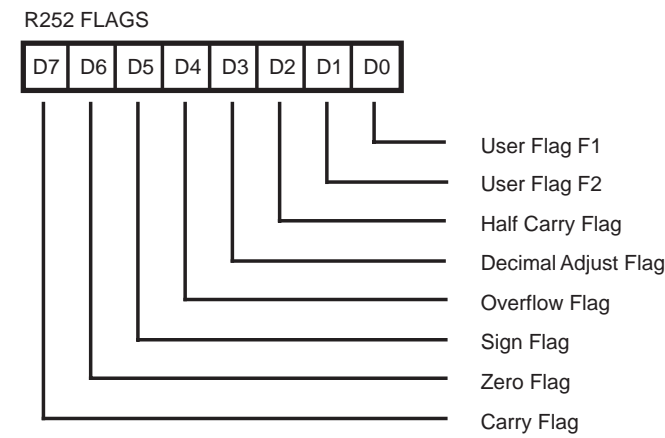
Figure 57. Flag Register
FCH: Read/Write

R253 RP

D7	D6	D5	D4	D3	D2	D1	D0

Expanded Register File

Working Register Pointer

Default After Reset = 00H
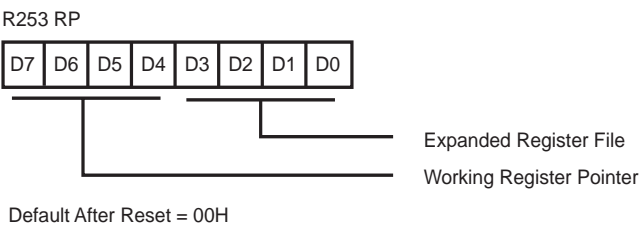
Figure 58. Register Pointer
FDH: Read/Write

R254 SPH

D7	D6	D5	D4	D3	D2	D1	D0

(Z86E40)
Stack Pointer Upper
Byte (SP8 - SP15)

(Z86E30/E31)
0 = 0 State
1 = 1 State
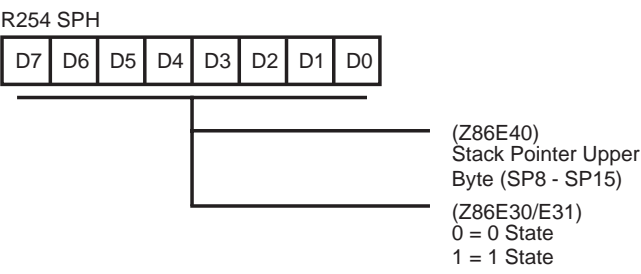
Figure 59. Stack Pointer High
FEH: Read/Write

R255 SPL

D7	D6	D5	D4	D3	D2	D1	D0

Stack Pointer Lower
Byte (SP0 - SP7)
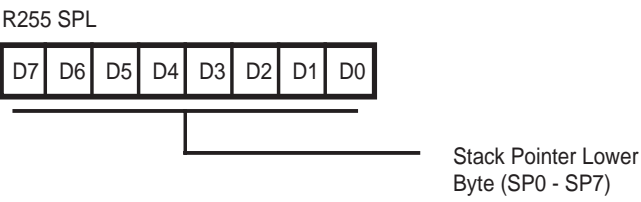
Figure 60. Stack Pointer Low
FFH: Read/Write

PACKAGE INFORMATION (Continued)

PACKAGE INFORMATION

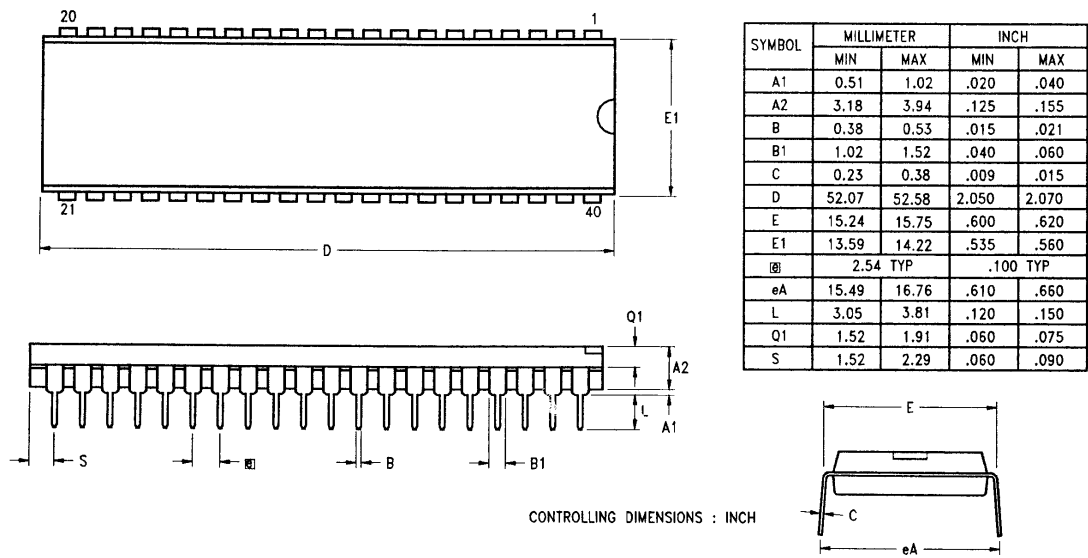| SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
⌾	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

Figure 61. 40-Pin DIP Package Diagram