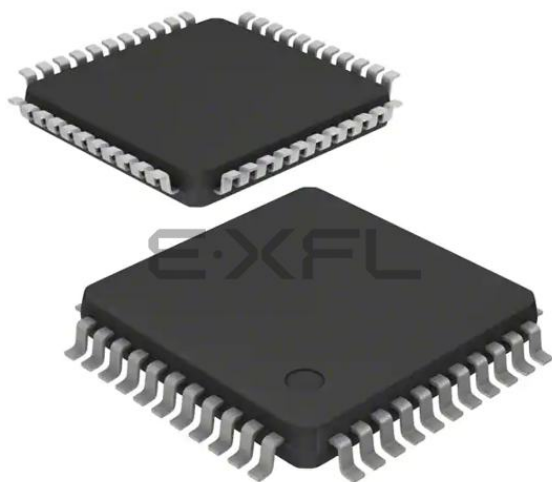




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e4016fsc00tr

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}



Figure 1. Z86E30/E31/E40 Functional Block Diagram

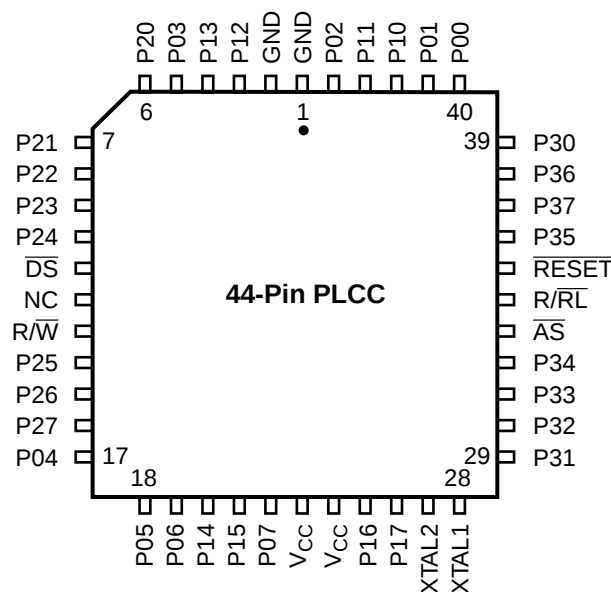


Figure 4. 44-Pin PLCC Pin Configuration Standard Mode

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1–2	GND	Ground	
3–4	P12–P13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6–10	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output
11	$\overline{DS}$	Data Strobe	Output
12	NC	No Connection	
13	R/ $\overline{W}$	Read/Write	Output
14–16	P25–P27	Port 2, Pins 5,6,7	In/Output
17–19	P04–P06	Port 0, Pins 4,5,6	In/Output
20–21	P14–P15	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23–24	V _{CC}	Power Supply	
25–26	P16–P17	Port 1, Pins 6,7	In/Output
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29–31	P31–P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
33	$\overline{AS}$	Address Strobe	Output
34	R/ $\overline{RL}$	ROM/ROMless select	Input
35	$\overline{RESET}$	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40–41	P00–P01	Port 0, Pins 0,1	In/Output
42–43	P10–P11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

PIN IDENTIFICATION (Continued)

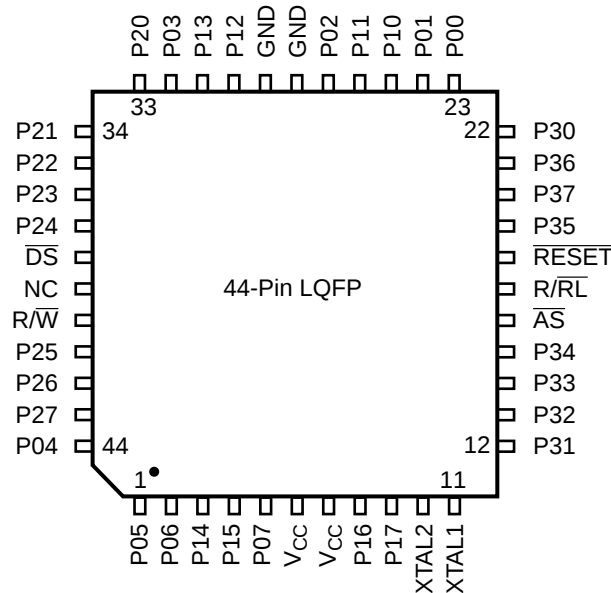


Figure 5. 44-Pin LQFP Pin Configuration
Standard Mode

Table 3. 44-Pin LQFP Pin Identification

Pin #	Symbol	Function	Direction
1–2	P05–P06	Port 0, Pins 5,6	In/Output
3–4	P14–P15	Port 1, Pins 4,5	In/Output
5	P07	Port 0, Pin 7	In/Output
6–7	V _{CC}	Power Supply	
8–9	P16–P17	Port 1, Pins 6,7	In/Output
10	XTAL2	Crystal Oscillator	Output
11	XTAL1	Crystal Oscillator	Input
12–14	P31–P33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	AS	Address Strobe	Output
17	R/RL	ROM/ROMless select	Input
18	RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23–24	P00–P01	Port 0, Pin 0,1	In/Output
25–26	P10–P11	Port 1, Pins 0,1	In/Output

Table 3. 44-Pin LQFP Pin Identification

Pin #	Symbol	Function	Direction
27	P02	Port 0, Pin 2	In/Output
28–29	GND	Ground	
30–31	P12–P13	Port 1, Pins 2,3	In/Output
32	P03	Port 0, Pin 3	In/Output
33–37	P20–4	Port 2, Pins 0,1,2,3,4	In/Output
38	DS	Data Strobe	Output
39	NC	No Connection	
40	R/W	Read/Write	Output
41–43	P25–P27	Port 2, Pins 5,6,7	In/Output
44	P04	Port 0, Pin 4	In/Output

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	-40	+105	C
Storage Temperature	-65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	-0.6	+7	V
Voltage on V_{DD} Pin with Respect to V_{SS}	-0.3	+7	V
Voltage on XTAL1 and $\overline{RESET}$ Pins with Respect to V_{SS} [Note 2]	-0.6	$V_{DD}+1$	V
Total Power Dissipation		1.21	W
Maximum Allowable Current out of V_{SS}		220	mA
Maximum Allowable Current into V_{DD}		180	mA
Maximum Allowable Current into an Input Pin [Note 3]	-600	+600	μ A
Maximum Allowable Current into an Open-Drain Pin [Note 4]	-600	+600	μ A
Maximum Allowable Output Current Sunked by Any I/O Pin		25	mA
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA
Maximum Allowable Output Current Sunked by $\overline{RESET}$ Pin		3 mA	

Notes:

1. This applies to all pins except XTAL pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD} .
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 1.2 W for the package. Power dissipation is calculated as follows:

$$\begin{aligned} \text{Total Power Dissipation} = & V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] \\ & + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] \\ & + \text{sum of } (V_{OL} \times I_{OL}) \end{aligned}$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Test Load).

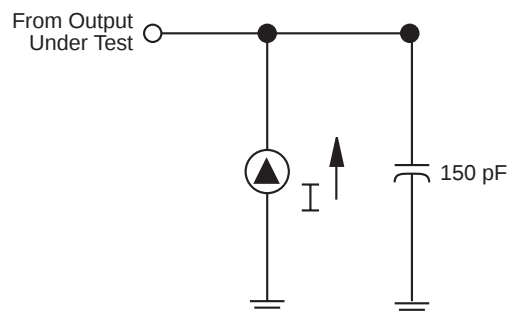


Figure 13. Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{ MHz}$; unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

$T_A = 0^\circ\text{C to } +70^\circ\text{C}$								
Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	1.8	V	Driven by External Clock Generator	
		5.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V		
V_{CL}	Clock Input Low Voltage	3.5V	$\text{GND} - 0.3$	$0.2 V_{CC}$	0.9	V	Driven by External Clock Generator	
		4.5V	$\text{GND} - 0.3$	$0.2 V_{CC}$	1.5	V		
V_{IH}	Input High Voltage	3.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V		
		5.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V		
V_{IL}	Input Low Voltage	3.5V	$\text{GND} - 0.3$	$0.2 V_{CC}$	1.5	V		
		5.5V	$\text{GND} - 0.3$	$0.2 V_{CC}$	1.5	V		
V_{OH}	Output High Voltage Low EMI Mode	3.5V	$V_{CC} - 0.4$		3.3	V	$I_{OH} = -0.5\text{ mA}$	
		5.5V	$V_{CC} - 0.4$		4.8	V		
V_{OH1}	Output High Voltage	3.5V	$V_{CC} - 0.4$		3.3	V	$I_{OH} = -2.0\text{ mA}$ $I_{OH} = -2.0\text{ mA}$	
		5.5V	$V_{CC} - 0.4$		4.8	V		
V_{OL}	Output Low Voltage Low EMI Mode	3.5V		0.4	0.2	V	$I_{OL} = 1.0\text{ mA}$ $I_{OL} = 1.0\text{ mA}$	
		4.5V		0.4	0.2	V		
V_{OL1}	Output Low Voltage	3.5V		0.4	0.1	V	$I_{OL} = +4.0\text{ mA}$ $I_{OL} = +4.0\text{ mA}$	8
		4.5V		0.4	0.1	V		
V_{OL2}	Output Low Voltage	3.5V		1.2	0.5	V	$I_{OL} = +12\text{ mA}$ $I_{OL} = +12\text{ mA}$	8
		4.5V		1.2	0.5	V		
V_{RH}	Reset Input High Voltage	3.5V	$.8 V_{CC}$	V_{CC}	1.7	V		
		5.5V	$.8 V_{CC}$	V_{CC}	2.1	V		
V_{RL}	Reset Input Low Voltage	3.5V	$\text{GND} - 0.3$	$0.2 V_{CC}$	1.3	V		13
		5.5V	$\text{GND} - 0.3$	$0.2 V_{CC}$	1.7	V		
V_{OLR}	Reset Output Low Voltage	3.5V		0.6	0.3	V	$I_{OL} = 1.0\text{ mA}$ $I_{OL} = 1.0\text{ mA}$	
		5.5V		0.6	0.2	V		
V_{OFFSET}	Comparator Input Offset Voltage	3.5V		25	10	mV		
		4.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	3.5V	0	$V_{CC} - 1.0\text{V}$		V		10
		5.5V	0	$V_{CC} - 1.0\text{V}$		V		
I_{IL}	Input Leakage	3.5V	-1	2	0.032	μA	$V_{IN} = 0\text{V}$, V_{CC} $V_{IN} = 0\text{V}$, V_{CC}	
		4.5V	-1	2	0.032	μA		
I_{OL}	Output Leakage	3.5V	-1	2	0.032	μA	$V_{IN} = 0\text{V}$, V_{CC} $V_{IN} = 0\text{V}$, V_{CC}	
		4.5V	-1	2	0.032	μA		
I_{IR}	Reset Input Current	3.5V	-20	-130	-65	μA		
		4.5V	-20	-180	-112	μA		

DC ELECTRICAL CHARACTERISTICS (Continued)

Handshake Timing Diagrams

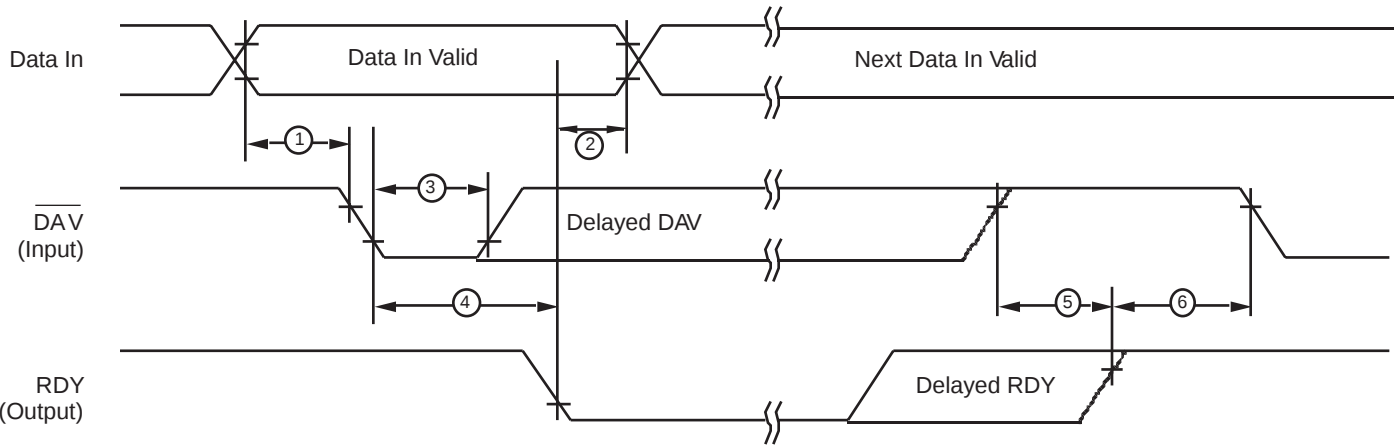


Figure 16. Input Handshake Timing

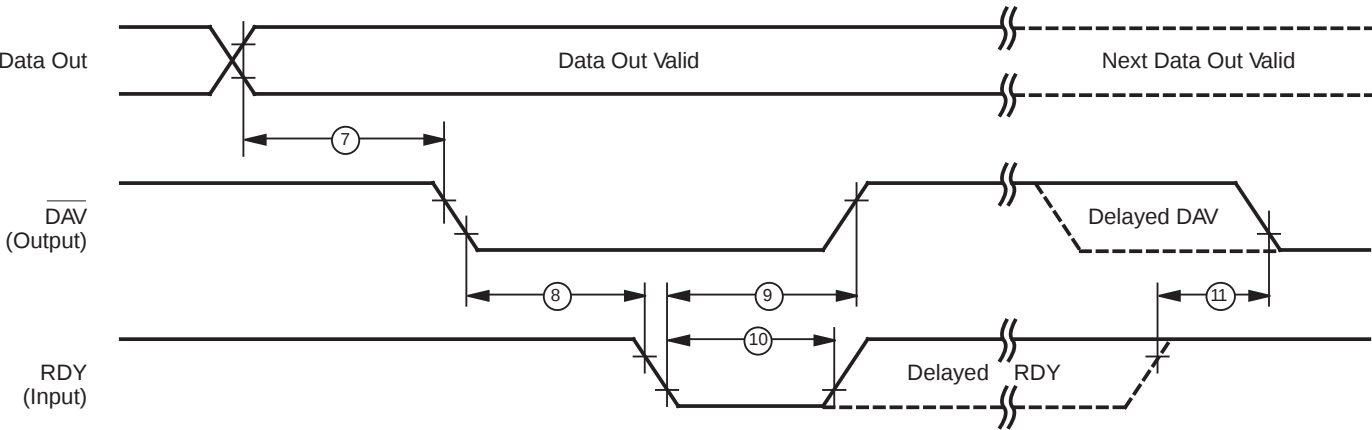


Figure 17. Output Handshake Timing

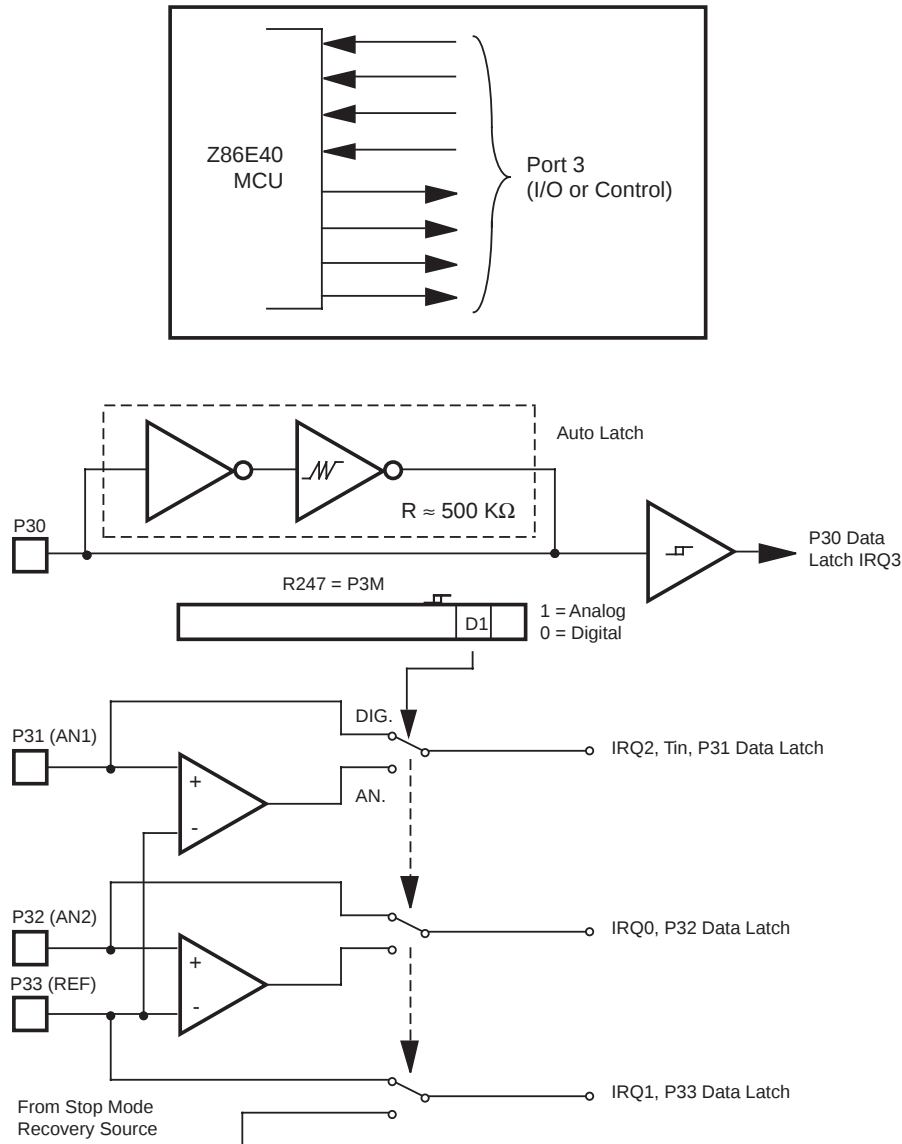


Figure 21. Port 3 Configuration

Table 9. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Interrupt	P0 HS	P1 HS	P2 HS	Ext
P30	IN			IRQ3				
P31	IN	T _{IN}	AN1	IRQ2		D/R		
P32	IN		AN2	IRQ0	D/R			
P33	IN		REF	IRQ1		D/R		
P34	OUT		AN1-Out			R/D		/DM
P35	OUT				R/D			
P36	OUT	T _{OUT}				R/D		
P37	OUT		An2-Out					

FUNCTIONAL DESCRIPTION (Continued)

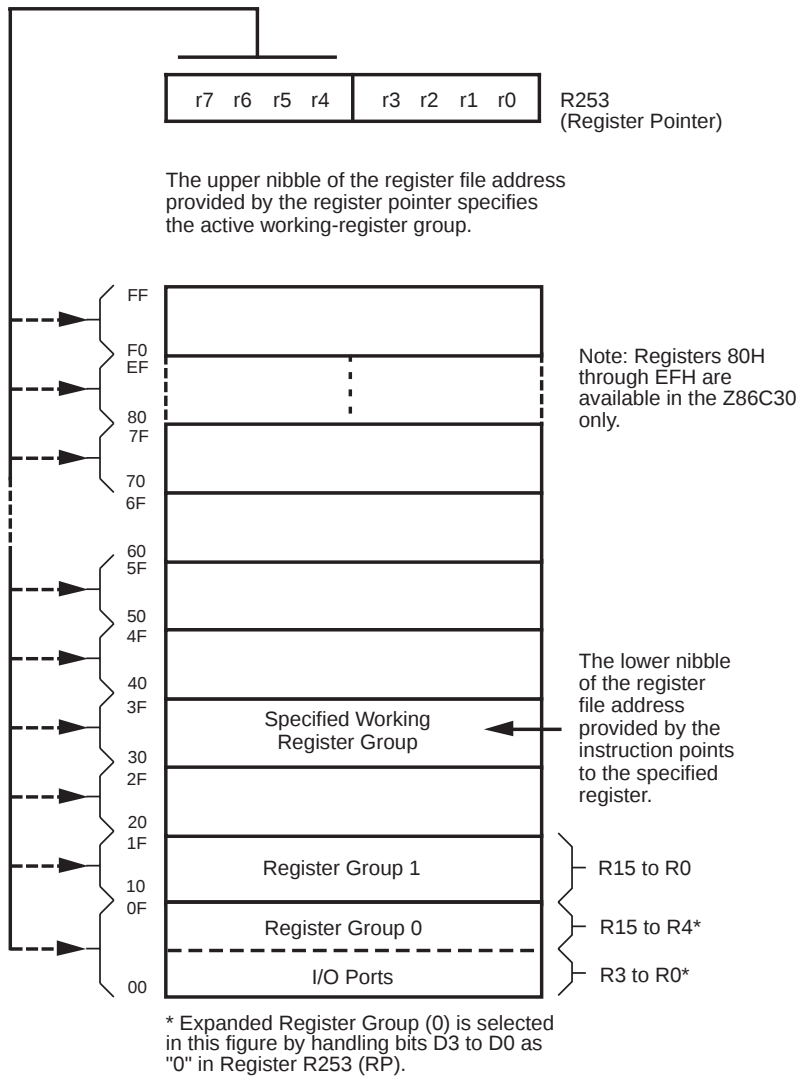


Figure 25. Register Pointer



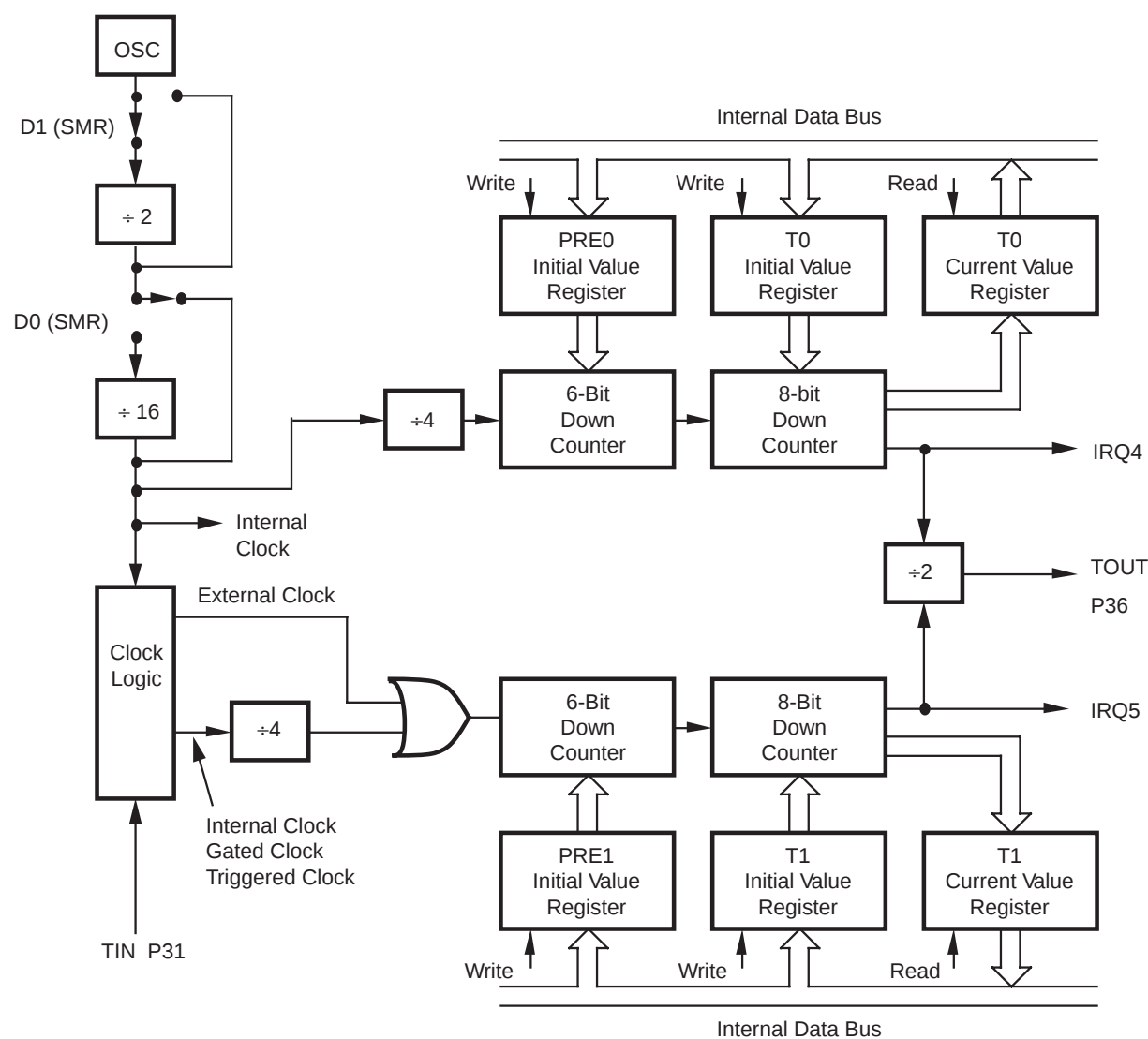


Figure 27. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

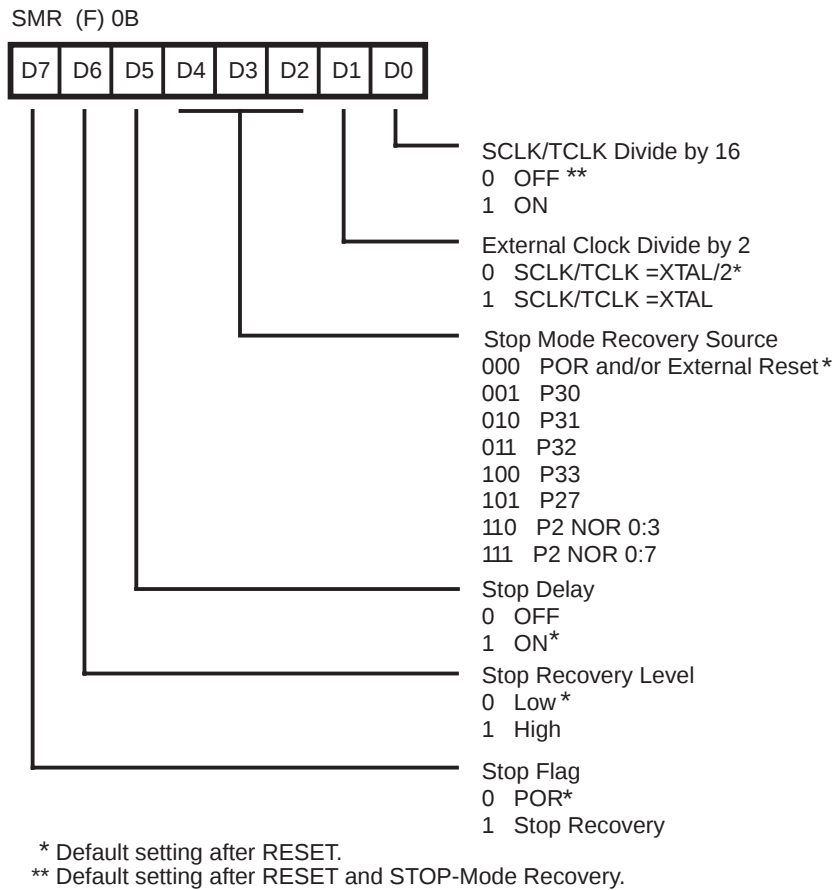


Figure 31. STOP-Mode Recovery Register
(Write-Only Except Bit D7, Which is Read-Only)

SCLK/TCLK Divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of

PCON further helps lower EMI (i.e., D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake up source of the STOP-Mode Recovery (Figure 32). Table 12 shows the SMR source selected with the setting of D2 to D4. P33–P31 cannot be used to wake up from STOP mode when programmed as analog inputs. When the STOP-Mode Recovery sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: If the Port2 pin is configured as an output, this output level will be read by the SMR circuitry.

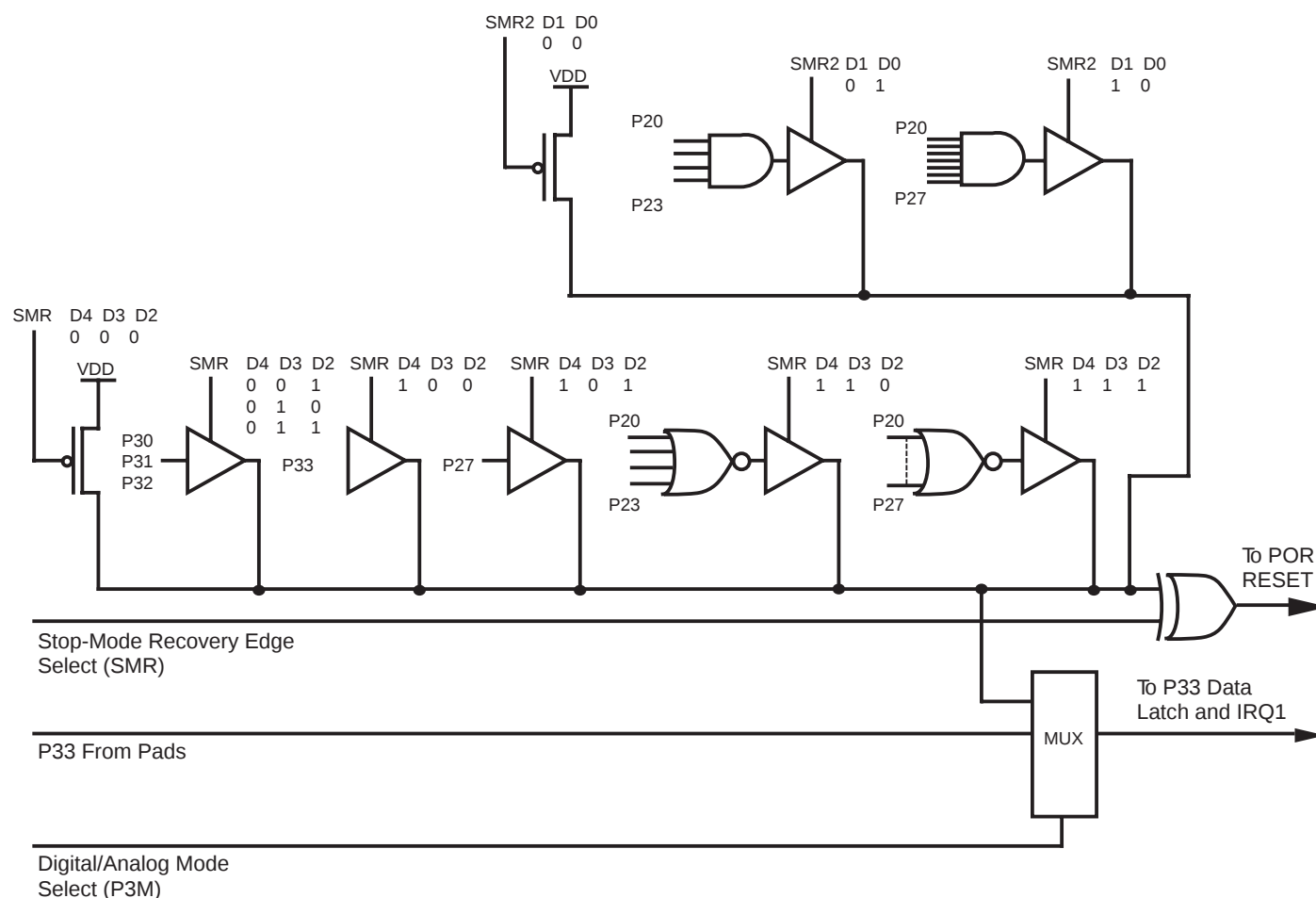


Figure 32. Stop-Mode Recovery Source

FUNCTIONAL DESCRIPTION (Continued)

EPROM MODE

Table 14 shows the programming voltages of each programming mode. Table 15, and figures that follow show the programming timing of each programming mode. Figure 38 shows the circuit diagram of a Z86E40 programming adapter, which adapts from 2764A to Z86E40 and Figure 39 shows the Z86E30/E31 Programming Adapter Circuitry. Figure 40 shows the flowchart of an Intelligent Programming Algorithm, which is compatible with 2764A EPROM (Z86E40 is 4K EPROM, 2764A is 8K EPROM). Since the EPROM size of Z86E30/E31/E40 differs from 2764A, the programming address range has to be set from 0000H to 0FFFH for the Z86E30/E40 and 0000H to 07FFH for Z86E31. Otherwise, the upper portion of EPROM data will overwrite the lower portion of EPROM data. Figure 39 shows the adaptation from the 2764A to Z86E30/E31.

Note: EPROM Protect feature allows the LDC, LDCI, LDE, and LDEI instructions from internal program memory. A ROM lookup table can be used with this feature.

During programming, the V_{PP} input pin supplies the programming voltage and current to the EPROM. This pin is also used to latch which EPROM mode is to be used (R/W EPROM or R/W Option bits). The mode is set by placing the correct mode number on the least significant bits of the address and raising the EPM pin above V . After a setup time, the V_{PP} pin can then be raised or lowered. The latched EPROM mode will remain until the EPM pin is reduced below V_H .

Mode Name	Mode #	LSB Addr
EPROM R/W	0	0000
Option Bit R/W	3	0011

EPROM R/W mode allows the programming of the user mode program ROM.

Option Bit R/W allows the programming of the Z8 option bits. When the device is latched into Option Bit R/W mode, the address must then be changed to 63 decimals (000000111111 Binary). The Options are mapped into this address as follows:

Bit	Option
7	Unused
6	Unused
5	32 KHz XTAL Option
4	Permanent WDT
3	Auto Latch Disable
2	RC Oscillator Option
1	RAM Protect
0	ROM Protect

Table 14 gives the proper conditions for EPROM R/W operations, once the mode is latched.

Table 14. EPROM Programming Table

Programming Modes	V _{PP}	EPM	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	ADDR	DATA	V _{CC} *
EPROM READ1	X	V _H	V _{IL}	V _{IL}	V _{IH}	ADDR	Out	4.5V†
EPROM READ2	X	V _H	V _{IL}	V _{IL}	V _{IH}	ADDR	Out	5.5V†
PROGRAM	V _H	V _H	V _{IL}	V _{IH}	V _{IL}	ADDR	In	6.4V
PROGRAM VERIFY	V _H	V _H	V _{IL}	V _{IL}	V _{IH}	ADDR	Out	6.0V
OPTION BIT PGM	V _H	V _H	V _{IL}	V _{IH}	V _{IL}	63	IN	6.4V
OPTION BIT READ	X	V _H	V _{IL}	V _{IL}	V _{IH}	63	OUT	6.0V

Notes:V_H = 13.0 V ± 0.1 VV_{IH} = As per specific Z8 DC specificationV_{IL} = As per specific Z8 DC specificationX=Not used, but must be set to V_H, V_{IH}, or V_{IL} level.NU = Not used, but must be set to either V_{IH} or V_{IL} level.I_{PP} during programming = 40 mA maximum.I_{CC} during programming, verify, or read = 40 mA maximum.*V_{CC} has a tolerance of ±0.25V.

† Zilog recommends an EPROM read at V_{CC} = 4.5 V and 5.5 V to ensure proper device operations during the V_{CC} after programming, but V_{CC} = 5.0 V is acceptable.

Table 15. EPROM Programming Timing

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		μs
2	Data Setup Time	2		μs
3	V _{PP} Setup	2		μs
4	V _{CC} Setup Time	2		μs
5	Chip Enable Setup Time	2		μs
6	Program Pulse Width	0.95	1.05	ms
7	Data Hold Time	2		μs
8	$\overline{OE}$ Setup Time	2		μs
9	Data Access Time	200		ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width/Option Program Pulse Width	2.85		ms
12	EPM Setup Time	2		μs
13	$\overline{PGM}$ Setup Time	2		μs
14	Address to $\overline{OE}$ Setup Time	2		μs
15	$\overline{OE}$ Width	250		ns
16	Address to $\overline{OE}$ Low	125		ns

Z86E40 TIMING DIAGRAMS

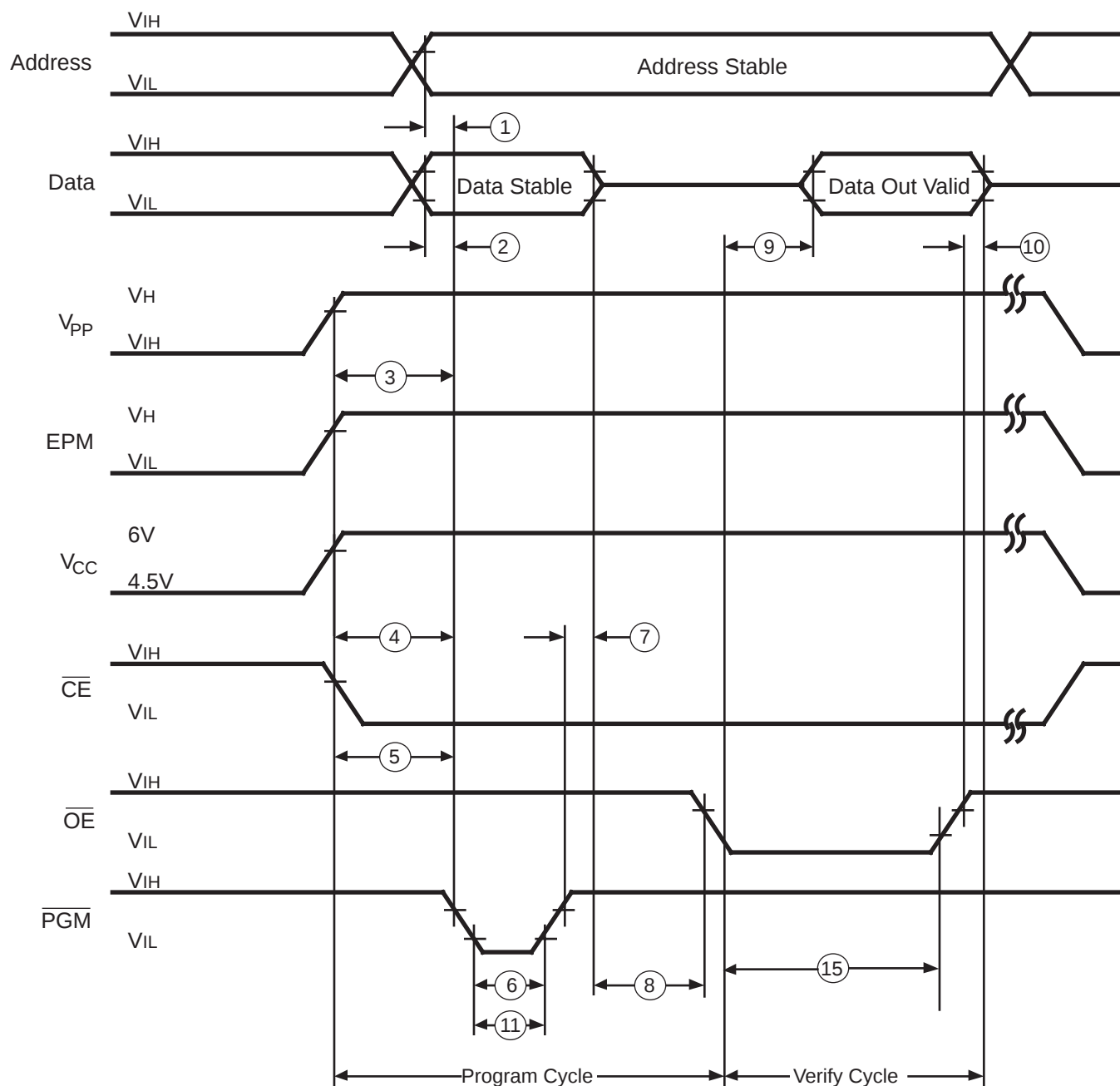


Figure 37. Timing Diagram of EPROM Program and Verify Modes

DS97Z8X0502

EXPANDED REGISTER FILE CONTROL REGISTERS

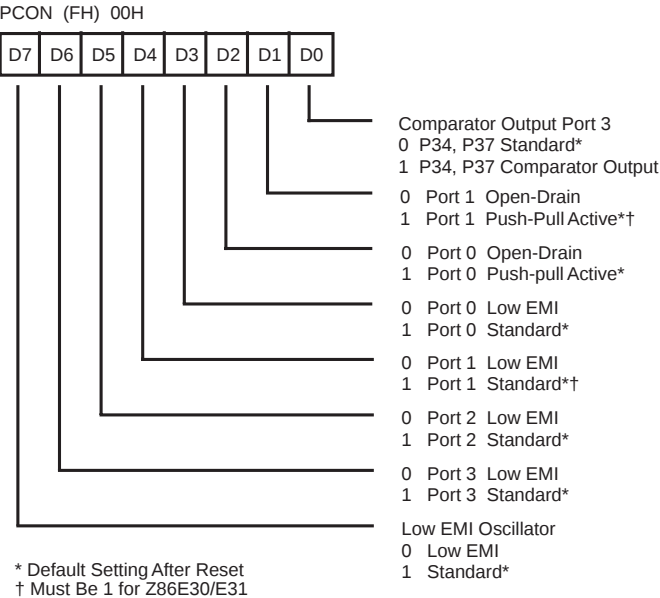


Figure 41. Port Configuration Register
Write Only

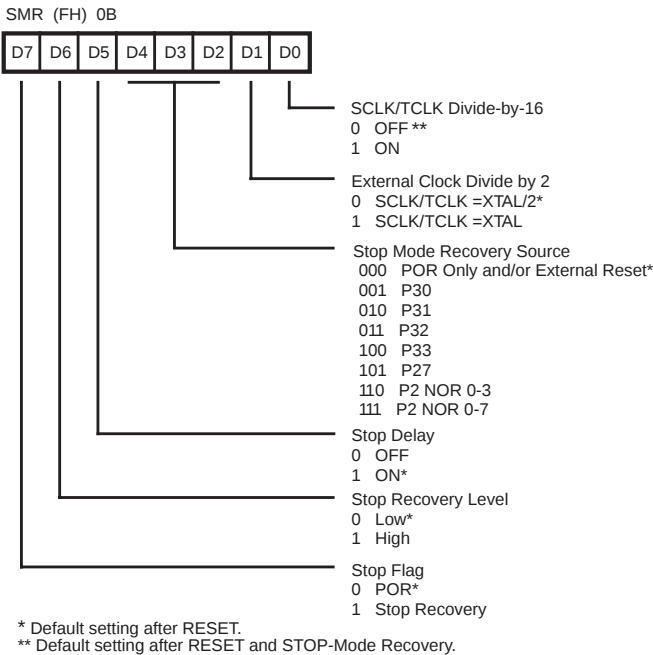


Figure 42. STOP-Mode Recovery Register
Write Only Except Bit D7, Which is Read Only

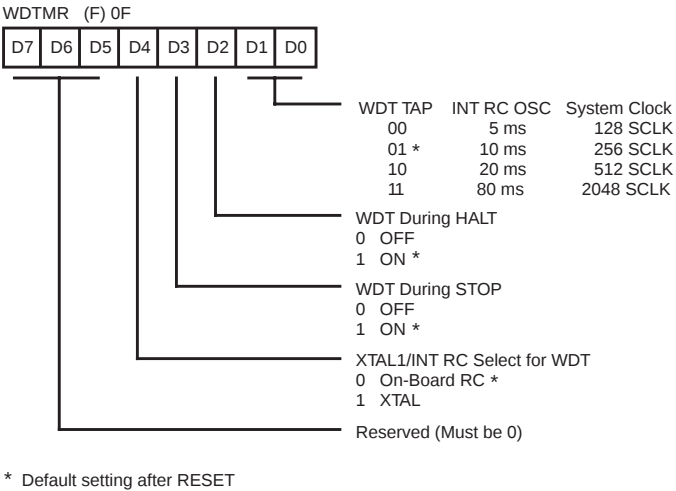


Figure 43. Watch-Dog Timer Mode Register
Write Only

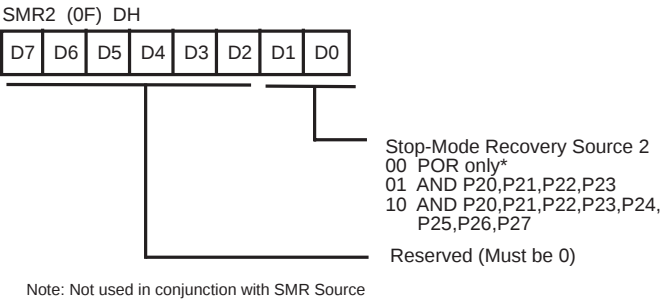


Figure 44. STOP-Mode Recovery Register 2
Write Only

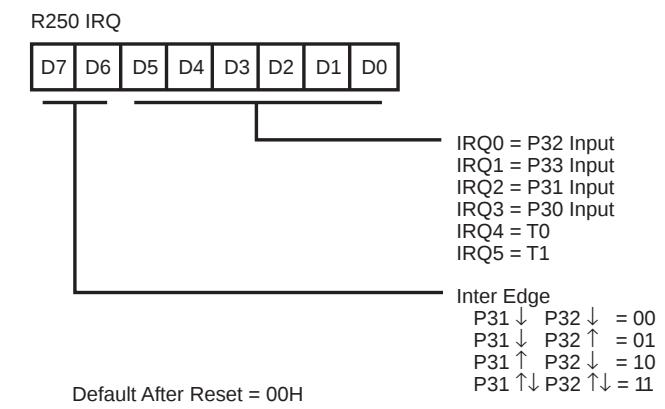


Figure 55. Interrupt Request Register
FAH: Read/Write

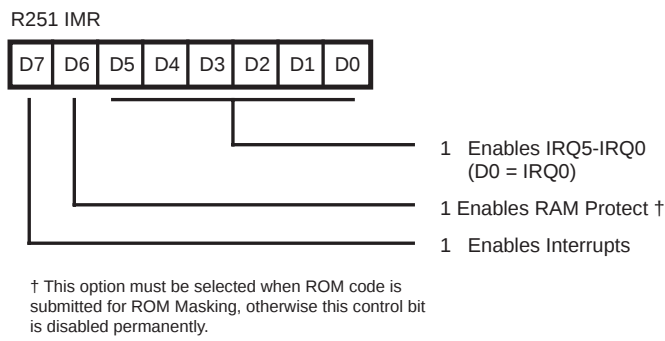


Figure 56. Interrupt Mask Register
FBH: Read/Write

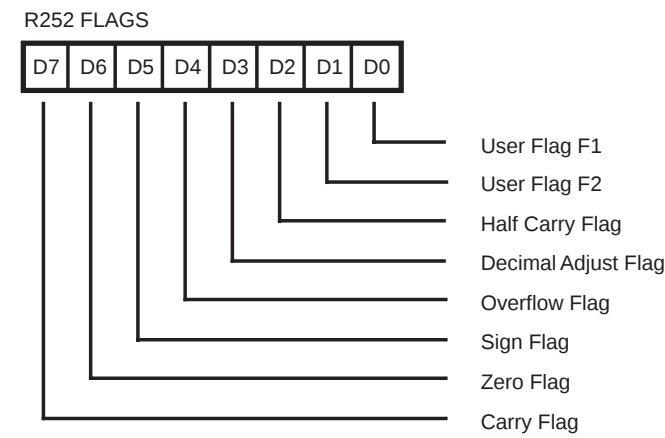


Figure 57. Flag Register
FCH: Read/Write

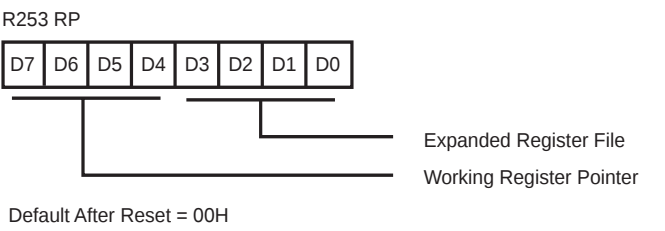


Figure 58. Register Pointer
FDH: Read/Write

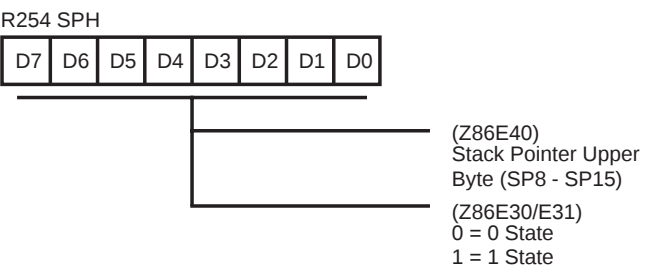


Figure 59. Stack Pointer High
FEH: Read/Write

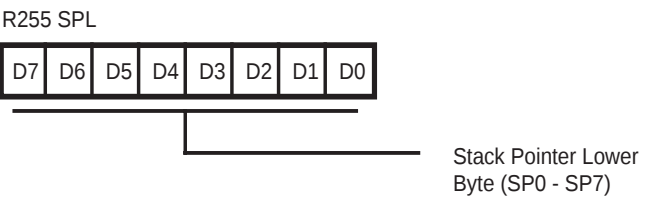


Figure 60. Stack Pointer Low
FFH: Read/Write

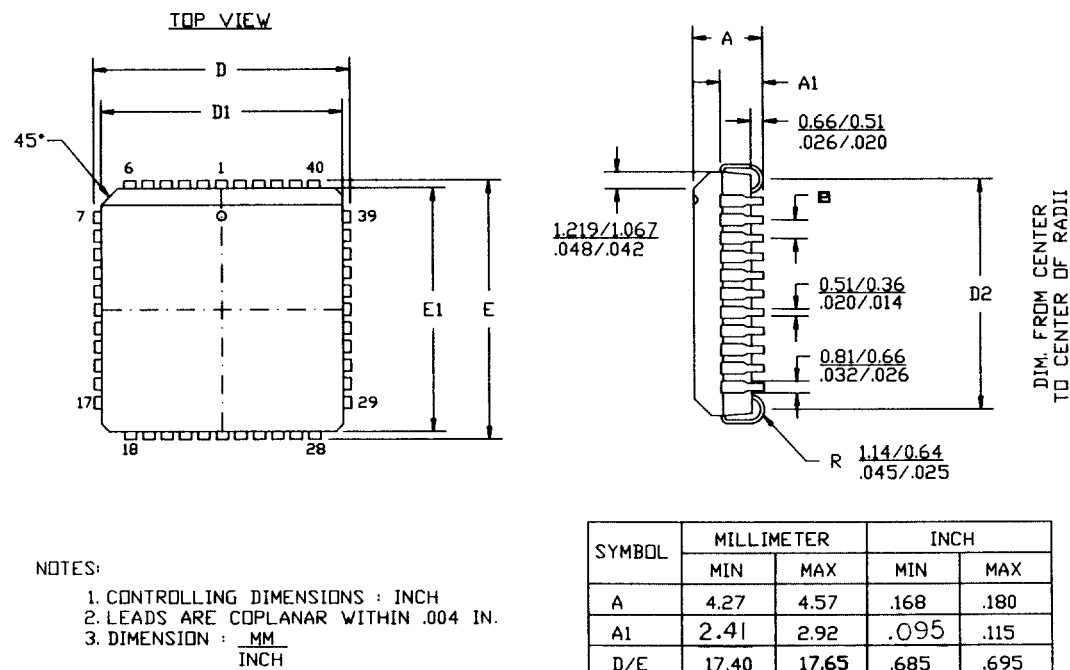


Figure 62. 44-Pin PLCC Package Diagram

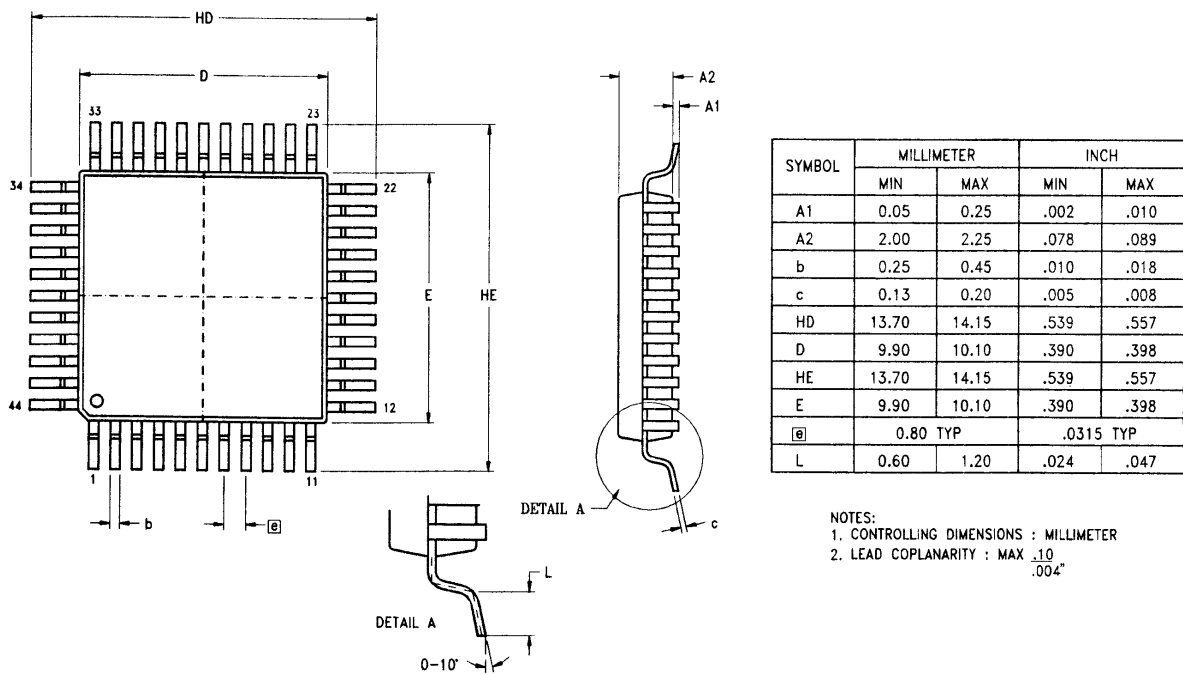


Figure 63. 44-Pin LQFP Package Diagram

ORDERING INFORMATION

Z86E40 (16 MHz)

40-Pin DIP	44-Pin PLCC	44-Pin LQFP
Z86E4016PSC	Z86E4016VSC	Z86E4016FSC
Z86E4016PEC	Z86E4016VEC	Z86E4016FEC

Z86E30 (16 MHz)

28-Pin DIP	28-Pin SOIC	28-Pin PLCC
Z86E3016PSC	Z86E3016SSC	Z86E3016VSC
Z96E3016PEC	Z86E3016SEC	Z86E3016VEC

Z86E31 (16 MHz)

28-Pin DIP	28-Pin SOIC	28-Pin PLCC
Z86E3116PSC	Z86E3116SSC	Z86E3116VSC
Z86E3116PEC	Z86E3116SEC	Z86E3116VEC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package

- P = Plastic DIP
- V = Plastic Leaded Chip Carrier
- F = Plastic Quad Flat Pack
- S = SOIC (Small Outline Integrated Circuit)

Temperature

- S = 0 °C to +70 °C
- E = -40 °C to +105 °C

Speed

- 16 = 16 MHz

Environmental

- C= Plastic Standard
- E = Hermetic Standard

Example:

