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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e4016vec00tr

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PIN IDENTIFICATION (Continued)



Figure 5. 44-Pin LQFP Pin Configuration Standard Mode

Table 3. 44-Pin LQFP Pin Identification

Pin #	Symbol	Function	Direction
1–2	P05-P06	Port 0, Pins 5,6	In/Output
3–4	P14–P15	Port 1, Pins 4,5	In/Output
5	P07	Port 0, Pin 7	In/Output
6–7	V _{CC}	Power Supply	
8–9	P16–P17	Port 1, Pins 6,7	In/Output
10	XTAL2	Crystal Oscillator	Output
11	XTAL1	Crystal Oscillator	Input
12–14	P31-P33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	ĀS	Address Strobe	Output
17	R/RL	ROM/ROMless select	Input
18	RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23–24	P00-P01	Port 0, Pin 0,1	In/Output
25–26	P10–P11	Port 1, Pins 0,1	In/Output

Table 3. 44-Pin LQFP Pin Identification

Pin #	Symbol	Function	Direction
27	P02	Port 0, Pin 2	In/Output
28–29	GND	Ground	
30–31	P12–P13	Port 1, Pins 2,3	In/Output
32	P03	Port 0, Pin 3	In/Output
33–37	P20–4	Port 2, Pins 0,1,2,3,4	In/Output
38	DS	Data Strobe	Output
39	NC	No Connection	
40	R/W	Read/Write	Output
41–43	P25–P27	Port 2, Pins 5,6,7	In/Output
44	P04	Port 0, Pin 4	In/Output



Figure 6. 40-Pin DIP Pin Configuration EPROM Mode

Table 4. 40-Pin DIP Package Pin IdentificationEPROM Mode

Pin #	Symbol	Function	Direction
1	NC	No Connection	
2–4	D5–D7	Data 5,6,7	In/Output
5–7	A4–A6	Address 4,5,6	Input
8–9	NC	No Connection	
10	A7	Address 7	Input
11	V _{CC}	Power Supply	
12–14	NC	No Connection	
15	CE	Chip Select	Input
16	OE	Output Enable	Input
17	EPM	EPROM Prog. Mode	Input
18	V _{PP}	Prog. Voltage	Input
19	A8	Address 8	Input
20–21	NC	No Connection	
22	A9	Address 9	Input
23	A11	Address 11	Input
24	A10	Address 10	Input
25	PGM	Prog. Mode	Input
26–27	A0–A1	Address 0,1	Input
28–29	NC	No Connection	
30	A2	Address 2	Input
31	GND	Ground	
32–33	NC	No Connection	
34	A3	Address 3	Input
35–39	D0–D4	Data 0,1,2,3,4	In/Output
40	NC	No Connection	



Figure 8. 44-Pin LQFP Pin Configuration EPROM Programming Mode

Table 6. 44-Pin LQFP Pin ConfigurationEPROM Programming Mode

Pin #	Symbol	Function	Direction
1–2	A5–A6	Address 5,6	Input
3–4	NC	No Connection	
5	A7	Address 7	Input
6–7	V _{CC}	Power Supply	
8–10	NC	No Connection	
11	CE	Chip Select	Input
12	ŌĒ	Output Enable	Input
13	EPM	EPROM Prog. Mode	Input
14	V _{PP}	Prog. Voltage	Input
15	A8	Address 8	Input
16–18	NC	No Connection	
19	A9	Address 9	Input
20	A11	Address 11	Input
21	A10	Address 10	Input
22	PGM	Prog. Mode	Input

Table 6. 44-Pin LQFP Pin ConfigurationEPROM Programming Mode

Pin #	Symbol	Function	Direction
23–24	A0,A1	Address 0,1	Input
25–26	NC	No Connection	
27	A2	Address 2	Input
28–29	GND	Ground	
30–31	NC	No Connection	
32	A3	Address 3	Input
33–37	D0–D4	Data 0,1,2,3,4	In/Output
38–40	NC	No Connection	
41–43	D5–D7	Data 5,6,7	In/Output
44	A4	Address 4	Input





Table 8.	28-Pin	EPROM	
Pin Identification			

Pin #	Symbol	Function	Direction
1–3	D5–D7	Data 5,6,7	In/Output
4–7	A4–A7	Address 4,5,6,7	Input
8	V _{CC}	Power Supply	
9	NC	No connection	
10	CE	Chip Select	Input
11	OE	Output Enable	Input
12	EPM	EPROM Prog.	Input
		Mode	
13	V _{PP}	Prog. Voltage	Input
14–15	A8–A9	Address 8,9	Input
16	A11	Address 11	Input
17	A10	Address 10	Input
18	PGM	Prog. Mode	Input
19–21	A0–A2	Address 0,1,2	Input
22	V _{SS}	Ground	
23	A3	Address 3	Input
24–28	D0-D4	Data 0,1,2,3,4	In/Output

DC ELECTRICAL CHARACTERISTICS (Continued)

T _A =–40 °C to +105 °C								
Sym	Parameter	V _{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
I _{ALH}	Auto Latch High Current	4.5V 5.5V	-1.0 -1.0	-10 -10	-3.8 -3.8	μΑ μΑ	$0V < V_{IN} < V_{CC}$ $0V < V_{IN} < V_{CC}$	9 9
T _{POR}	Power On Reset	4.5V 5.5V	2.0 2.0	14 14	4 4	mS mS		
V _{LV}	Auto Reset Voltage		2.0	3.3	2.9	V		1

1. Device does function down to the Auto Reset voltage.

2. GND=0V

3. The V_{CC} voltage specification of 5.5V guarantees 5.0V \pm 0.5V.

4. All outputs unloaded, I/O pins floating, inputs at rail.

- 5. CL1= CL2 = 22 pF
- 6. Same as note [4] except inputs at V_{CC} .
- 7. Maximum temperature is 70°C
- 8. STD Mode (not Low EMI Mode)
- 9. Auto Latch (mask option) selected
- 10. For analog comparator inputs when analog comparators are enabled.
- 11. Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.
- 12. Typicals are at $V_{CC} = 5.0V$
- 13. Z86E40 only
- 14. WDT is not running.



Figure 14. External I/O or Memory Read/Write Timing Z86E40 Only

Handshake Timing Diagrams







Figure 17. Output Handshake Timing

Zilog

Port 2 (P27–P20). Port 2 is an 8-bit, bidirectional, CMOScompatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control.

In Handshake Mode, Port 3 lines P31 and P36 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2 (Figure 20).



Figure 20. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS-compatible port with four fixed inputs (P33-P30) and four fixed outputs (P37–P34). These eight lines can be configured by software for interrupt and handshake control functions. Port 3, Pin 0 is Schmitt- triggered. P31, P32, and P33 are standard CMOS inputs with single trip point (no Auto Latches) and P34, P35, P36, and P37 are push-pull output lines. Low EMI output buffers can be globally programmed by the software. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by setting the D1 of Port 3 Mode Register (P3M). The comparator output can be outputted from P34 and P37, respectively, by setting PCON register Bit D0 to 1 state. For the interrupt function, P30 and P33 are falling edge triggered interrupt inputs. P31 and P32 can be programmed as falling, rising or both edges triggered interrupt inputs (Figure 21). Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Port 0, Port 1, and Port 2 are also available on Port 3 (Table 9).

Note: When enabling/ or disabling analog mode, the following is recommended:

- 1. Allow two NOP delays before reading this comparator output.
- 2. Disable global interrupts, switch to analog mode, clear interrupts, and then re-enable interrupts.
- 3. IRQ register bits 3 to 0 must be cleared after enabling analog mode.

Note: P33–P30 differs from the Z86C30/C31/C40 in that there is no clamping diode to V_{CC} due to the EPROM high-voltage circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode.

FUNCTIONAL DESCRIPTION

The MCU incorporates the following special functions to enhance the standard Z8 architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of three ways:

- 1. Power-On Reset
- 2. Watch-Dog Timer
- 3. STOP-Mode Recovery Source

Note: Having the Auto Power-On Reset circuitry built-in, the MCU does not need to be connected to an external power-on reset circuit. The reset time is 5 ms (typical). The MCU does not reinitialize WDTMR, SMR, P2M, and P3M registers to their reset values on a STOP-Mode Recovery operation.

Note: The device V_{CC} must rise up to the operating V_{CC} specification before the TPOR expires.

Program Memory. The MCU can address up to 4 KB of Internal Program Memory (Figure 22). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 12 (000CH) to address 4095 (0FFFH) consists of programmable EPROM. After reset, the program counter points at the address 000CH, which is the starting address of the user program.

In ROMless mode, the Z86E40 can address up to 64 KB of External Program Memory. The ROM/ROMless option is only available on the 44-pin devices.

65535		EPROM	ROMIess
	4096	External ROM and RAM	External
4	4095	On-Chip One Time PROM	ROM and RAM
Location of	12	✓	
Instruction	11	IRQ5	IRQ5
After RESET	10	IRQ5	IRQ5
Interrupt Vector (Lower Byte) Interrupt Vector (Upper Byte)	9	IRQ4	IRQ4
	8	IRQ4	IRQ4
	7	IRQ3	IRQ3
	6	IRQ3	IRQ3
	5	IRQ2	IRQ2
	4	IRQ2	IRQ2
	3	IRQ1	IRQ1
	2	IRQ1	IRQ1
	1	IRQ0	IRQ0
	0	IRQ0	IRQ0

Figure 22. Program Memory Map (ROMIess Z86E40 Only)

EPROM Protect. When in ROM Protect Mode, and executing out of External Program Memory, instructions LDC, LDCI, LDE, and LDEI cannot read Internal Program Memory.

When in ROM Protect Mode and executing out of Internal Program Memory, instructions LDC, LDCI, LDE, and LDEI can read Internal Program Memory.

Data Memory (DM). In EPROM Mode, the Z86E40 can address up to 60 KB of external data memory beginning at location 4096. In ROMIess mode, the Z86E40 can address up to 64 KB of data memory. External data memory may be included with, or separated from, the external program memory space. DM, an optional I/O function that can be

programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 23). The state of the \overline{DM} signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM (\overline{DM} inactive) memory, and an LDE instruction references data (\overline{DM} active Low) memory.



Figure 23. Data Memory Map

Register File. The register file consists of three I/O port registers, 236/125 general-purpose registers, 15 control and status registers, and three system configuration registers in the expanded register group. The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 24). In the 4-bit mode, the register file is divided into 16 working register groups, each

occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Bank E0–EF can only be accessed through working register and indirect addressing modes. (This bank is available in Z86E30/E40 only.)



Default setting after RESET = 00000000

Figure 24. Register Pointer Register

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 26). These register groups are known as the Expanded Register File (ERF).

The low nibble (D3–D0) of the Register Pointer (RP) select the active ERF group, and the high nibble (D7–D4) of register RP select the working register group. Three system configuration registers reside in the Expanded Register File at bank FH: PCON, SMR, and WDTMR. The rest of the Expanded Register is not physically implemented and is reserved for future expansion.



Figure 25. Register Pointer

Z8® STANDARD CONTROL REGISTERS



Figure 26. Expanded Register File Architecture

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- 1. Power fail to Power OK status
- 2. Stop-Mode Recovery (if D5 of SMR=0)
- 3. WDT time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP mode Register (SMR) determines whether the POR timer is bypassed after STOP-Mode Recovery (typical for an external clock and RC/LC oscillators with fast start up times).

HALT. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (Opcode=FFH) immediately before the appropriate sleep instruction, that is:

FF	NOP	; clear the pipeline
6F	STOP	; enter STOP Mode
	or	
FF	NOP	; clear the pipeline
7F	HALT	; enter HALT Mode

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. STOP Mode is terminated by one of the following resets: either by WDT time-out, POR, a Stop-Mode Recovery Source, which is defined by the SMR register or external reset. This causes the processor to restart the application program at address 000CH.

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2 and 3, and low EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00 (Figure 30).







* Default setting after RESET.

** Default setting after RESET and STOP-Mode Recovery.

Figure 31. STOP-Mode Recovery Register (Write-Only Except Bit D7, Which is Read-Only) cycles from the execution of the first instruction after Power-On Reset, Watch-Dog reset or a STOP-Mode Recovery (Figures 33 and 34). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH.



* Default setting after RESET



Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{LV} (Figure 35).

Note: V_{CC} must be in the allowed operating range prior to the minimum Power-On Reset time-out (T_{POR}).



Figure 35. Typical Z86E40 V_{LV} Voltage vs. Temperature

Z86E40 TIMING DIAGRAMS



Figure 37. Timing Diagram of EPROM Program and Verify Modes

PACKAGE INFORMATION



Figure 61. 40-Pin DIP Package Diagram