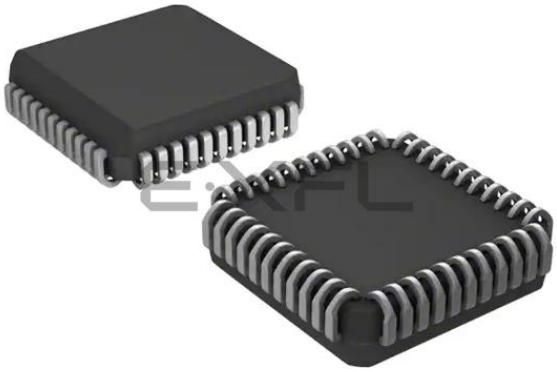

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e4016veg

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

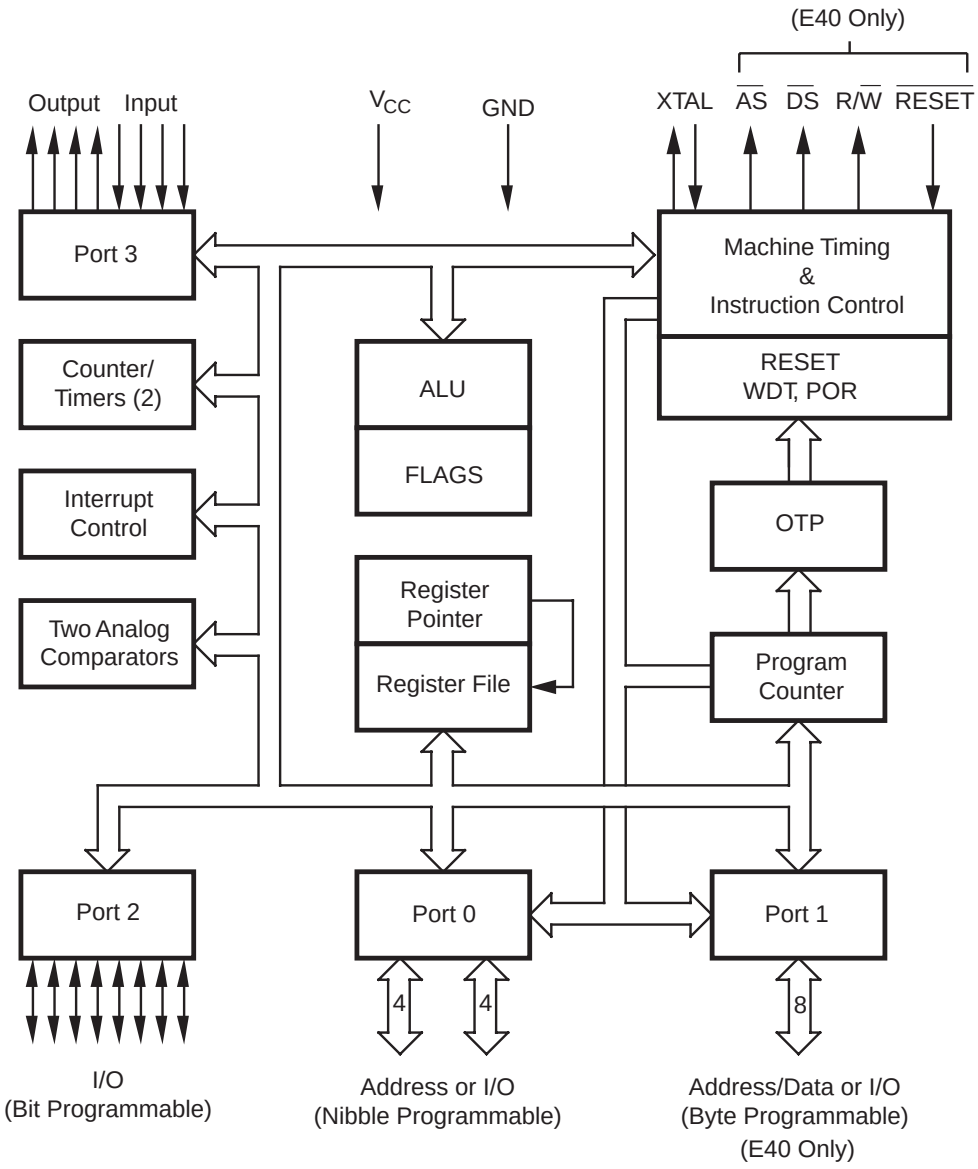


Figure 1. Z86E30/E31/E40 Functional Block Diagram

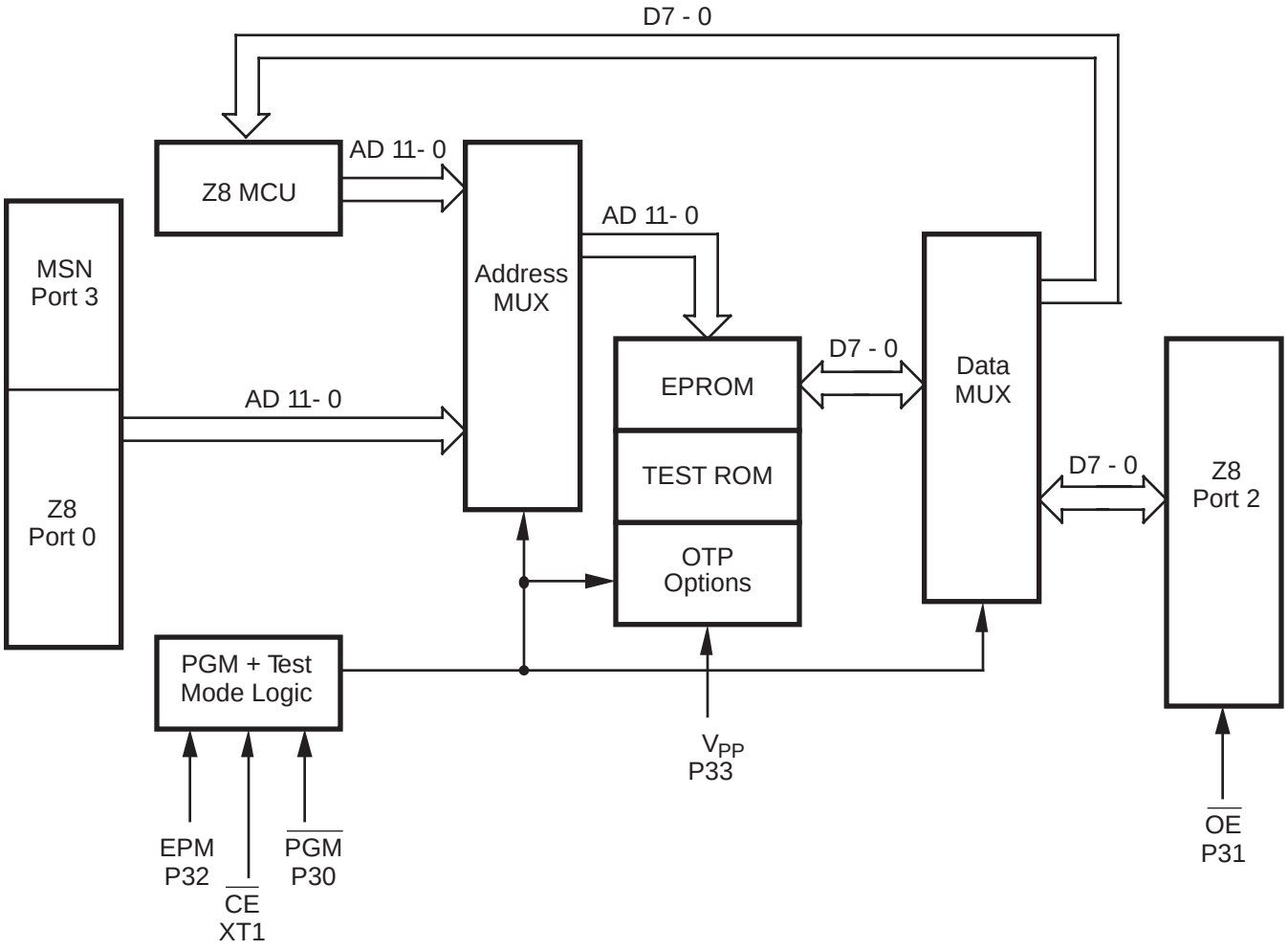


Figure 2. EPROM Programming Block Diagram

PIN IDENTIFICATION

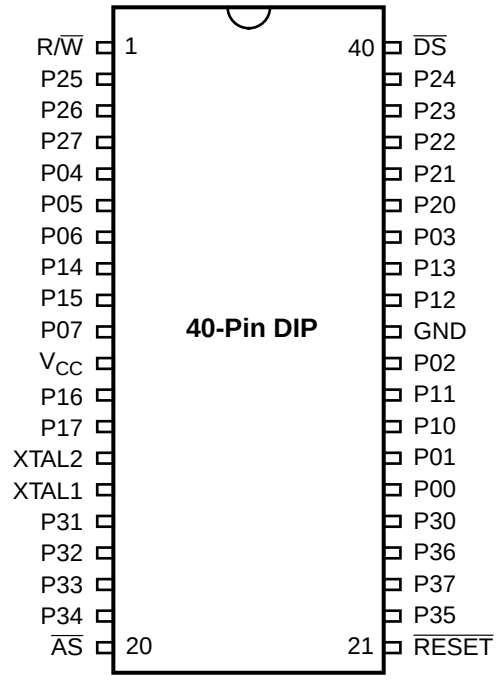


Figure 3. 40-Pin DIP Pin Configuration Standard Mode

Table 1. 40-Pin DIP Pin Identification Standard Mode

Pin #	Symbol	Function	Direction
1	R/$\overline{W}$	Read/Write	Output
2–4	P25–P27	Port 2, Pins 5,6,7	In/Output
5–7	P04–P06	Port 0, Pins 4,5,6	In/Output
8–9	P14–P15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V_{CC}	Power Supply	
12–13	P16–P17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal Oscillator	Output
15	XTAL1	Crystal Oscillator	Input
16–18	P31–P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	$\overline{AS}$	Address Strobe	Output
21	$\overline{RESET}$	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26–27	P00–P01	Port 0, Pins 0,1	In/Output
28–29	P10–P11	Port 1, Pins 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground	
32–33	P12–P13	Port 1, Pins 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35–39	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output
40	$\overline{DS}$	Data Strobe	Output

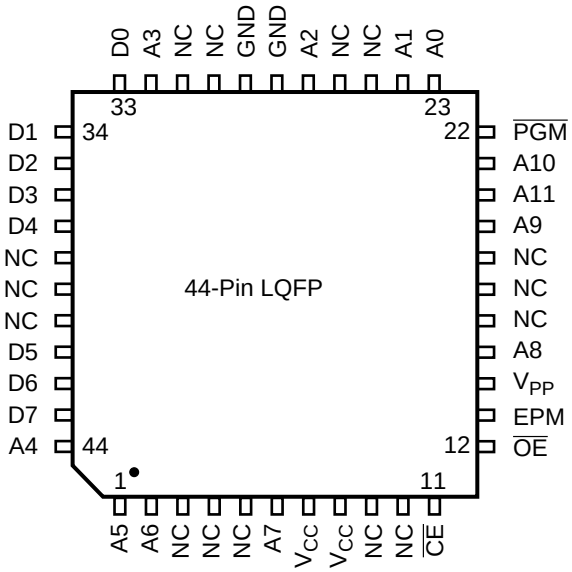


Figure 8. 44-Pin LQFP Pin Configuration EPROM Programming Mode

Table 6. 44-Pin LQFP Pin Configuration EPROM Programming Mode

Pin #	Symbol	Function	Direction
1–2	A5–A6	Address 5,6	Input
3–4	NC	No Connection	
5	A7	Address 7	Input
6–7	V_{CC}	Power Supply	
8–10	NC	No Connection	
11	$\overline{CE}$	Chip Select	Input
12	$\overline{OE}$	Output Enable	Input
13	EPM	EPROM Prog. Mode	Input
14	V_{PP}	Prog. Voltage	Input
15	A8	Address 8	Input
16–18	NC	No Connection	
19	A9	Address 9	Input
20	A11	Address 11	Input
21	A10	Address 10	Input
22	$\overline{PGM}$	Prog. Mode	Input

Table 6. 44-Pin LQFP Pin Configuration EPROM Programming Mode

Pin #	Symbol	Function	Direction
23–24	A0,A1	Address 0,1	Input
25–26	NC	No Connection	
27	A2	Address 2	Input
28–29	GND	Ground	
30–31	NC	No Connection	
32	A3	Address 3	Input
33–37	D0–D4	Data 0,1,2,3,4	In/Output
38–40	NC	No Connection	
41–43	D5–D7	Data 5,6,7	In/Output
44	A4	Address 4	Input

PIN IDENTIFICATION (Continued)

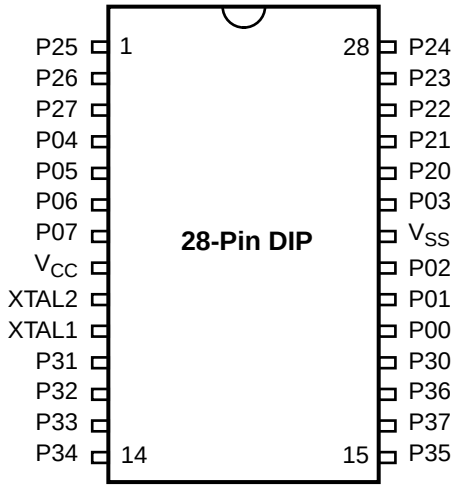


Figure 9. Standard Mode 28-Pin DIP/SOIC Pin Configuration

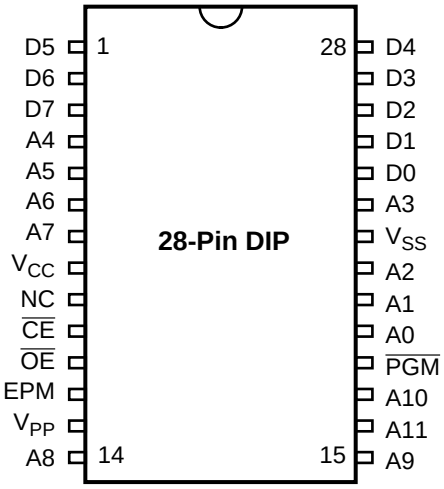


Figure 10. EPROM Programming Mode 28-Pin DIP/SOIC Pin Configuration

Table 7. 28-Pin DIP/SOIC/PLCC Pin Identification*

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Pins 5,6,	In/Output
4–7	P04–P07	Port 0, Pins 4,5,6,7	In/Output
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11–13	P31–P33	Port 3, Pins 1,2,3	Input
14–15	P34–P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19–21	P00–P02	Port 0, Pins 0,1,2	In/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24–28	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output

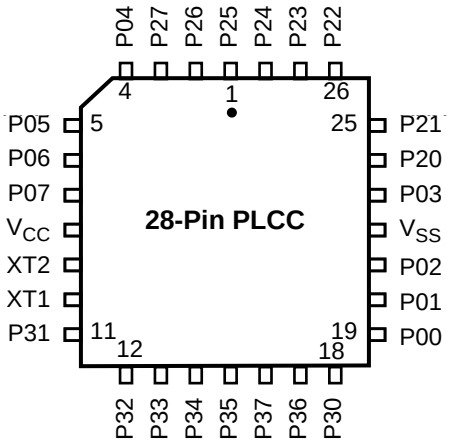


Figure 11. Standard Mode 28-Pin PLCC Pin Configuration

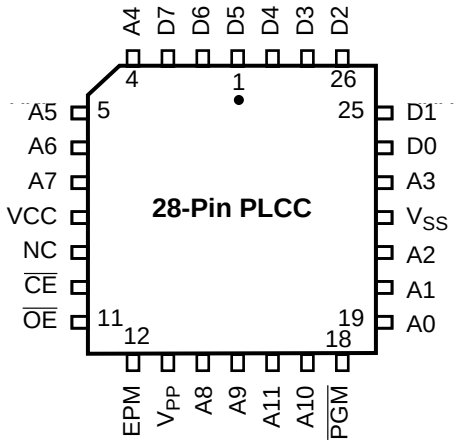


Figure 12. EPROM Programming Mode 28-Pin PLCC Pin Configuration

Table 8. 28-Pin EPROM Pin Identification

Pin #	Symbol	Function	Direction
1–3	D5–D7	Data 5,6,7	In/Output
4–7	A4–A7	Address 4,5,6,7	Input
8	V_{CC}	Power Supply	
9	NC	No connection	
10	$\overline{CE}$	Chip Select	Input
11	$\overline{OE}$	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V_{PP}	Prog. Voltage	Input
14–15	A8–A9	Address 8,9	Input
16	A11	Address 11	Input
17	A10	Address 10	Input
18	$\overline{PGM}$	Prog. Mode	Input
19–21	A0–A2	Address 0,1,2	Input
22	V_{SS}	Ground	
23	A3	Address 3	Input
24–28	D0–D4	Data 0,1,2,3,4	In/Output

DC ELECTRICAL CHARACTERISTICS (Continued)

			T_A=–40 °C to +105 °C					
Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{ALH}	Auto Latch High Current	4.5V	-1.0	-10	-3.8	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V	-1.0	-10	-3.8	µA	$0V < V_{IN} < V_{CC}$	9
T_{POR}	Power On Reset	4.5V	2.0	14	4	mS		
		5.5V	2.0	14	4	mS		
V_{LV}	Auto Reset Voltage		2.0	3.3	2.9	V		1

1. Device does function down to the Auto Reset voltage.
2. GND=0V
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1= CL2 = 22 pF
6. Same as note [4] except inputs at V_{CC}.
7. Maximum temperature is 70°C
8. STD Mode (not Low EMI Mode)
9. Auto Latch (mask option) selected
10. For analog comparator inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.
12. Typicals are at V_{CC} = 5.0V
13. Z86E40 only
14. WDT is not running.

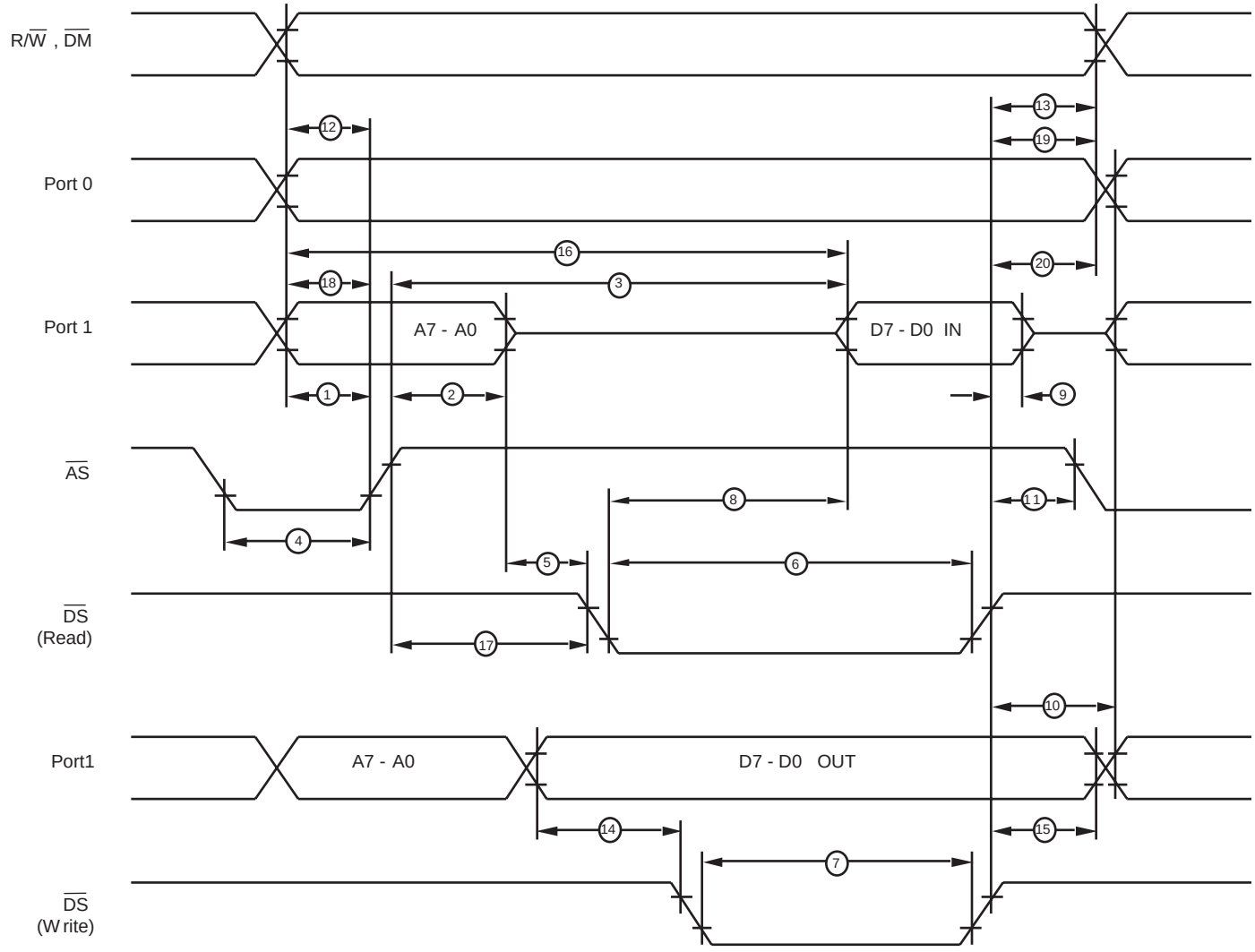


Figure 14. External I/O or Memory Read/Write Timing
Z86E40 Only

			T_A = -40°C to 105°C 16 MHz Note [3]				
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	4.5V 5.5V	25 25		ns ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	4.5V 5.5V	35 35		ns ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	4.5V 5.5V		180 180	ns ns	1,2
4	TwAS	$\overline{AS}$ Low Width	4.5V 5.5V	40 40		ns ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	4.5V 5.5V	0 0		ns ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	4.5V 5.5V	135 135		ns ns	1,2
7	TwDSW	$\overline{DS}$ (Write) Low Width	4.5V 5.5V	80 80		ns ns	1,2
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid	4.5V 5.5V		75 75	ns ns	1,2
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	4.5V 5.5V	0 0		ns ns	2
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	4.5V 5.5V	50 50		ns ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	4.5V 5.5V	35 35		ns ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	4.5V 5.5V	25 25		ns ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	4.5V 5.5V	35 35		ns ns	2
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	4.5V 5.5V	55 55	25 25	ns ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	4.5V 5.5V	35 35		ns ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	4.5V 5.5V		230 230	ns ns	1,2
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	4.5V 5.5V	45 45		ns ns	2
18	TdDM(AS)	/DM Valid to $\overline{AS}$ Fall Delay	4.5V 5.5V	30 30		ns ns	2
20	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	4.5V 5.5V	35 35		ns ns	

Notes:

1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

DC ELECTRICAL CHARACTERISTICS (Continued)

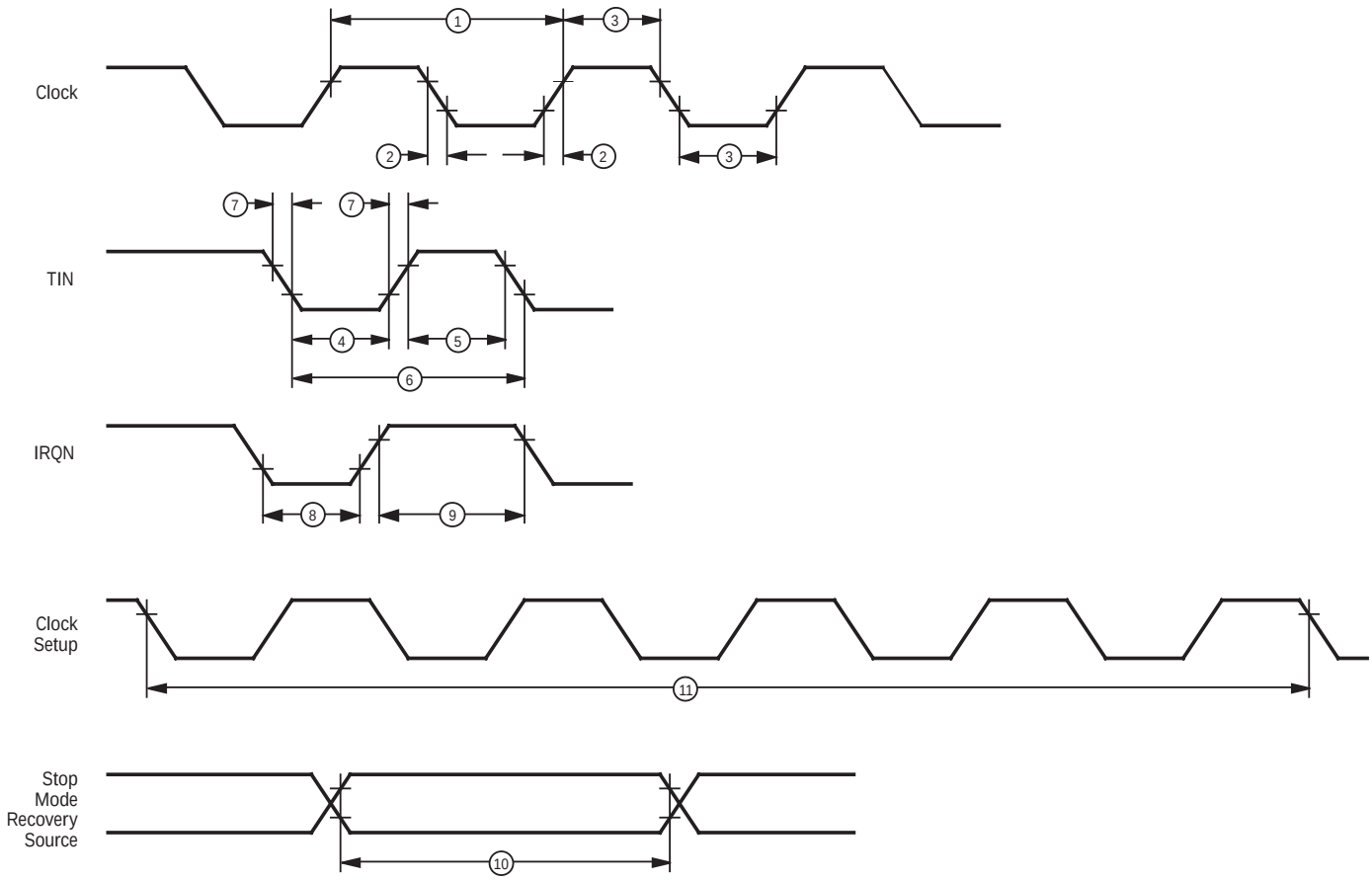


Figure 15. Additional Timing Diagram

PIN FUNCTIONS (Continued)

Port 1 (P17–P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7–A0) and Data (D7–D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and /DAV1 (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (Figure 19).

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z86E40 to share common resources in multiprocessor and DMA applications.

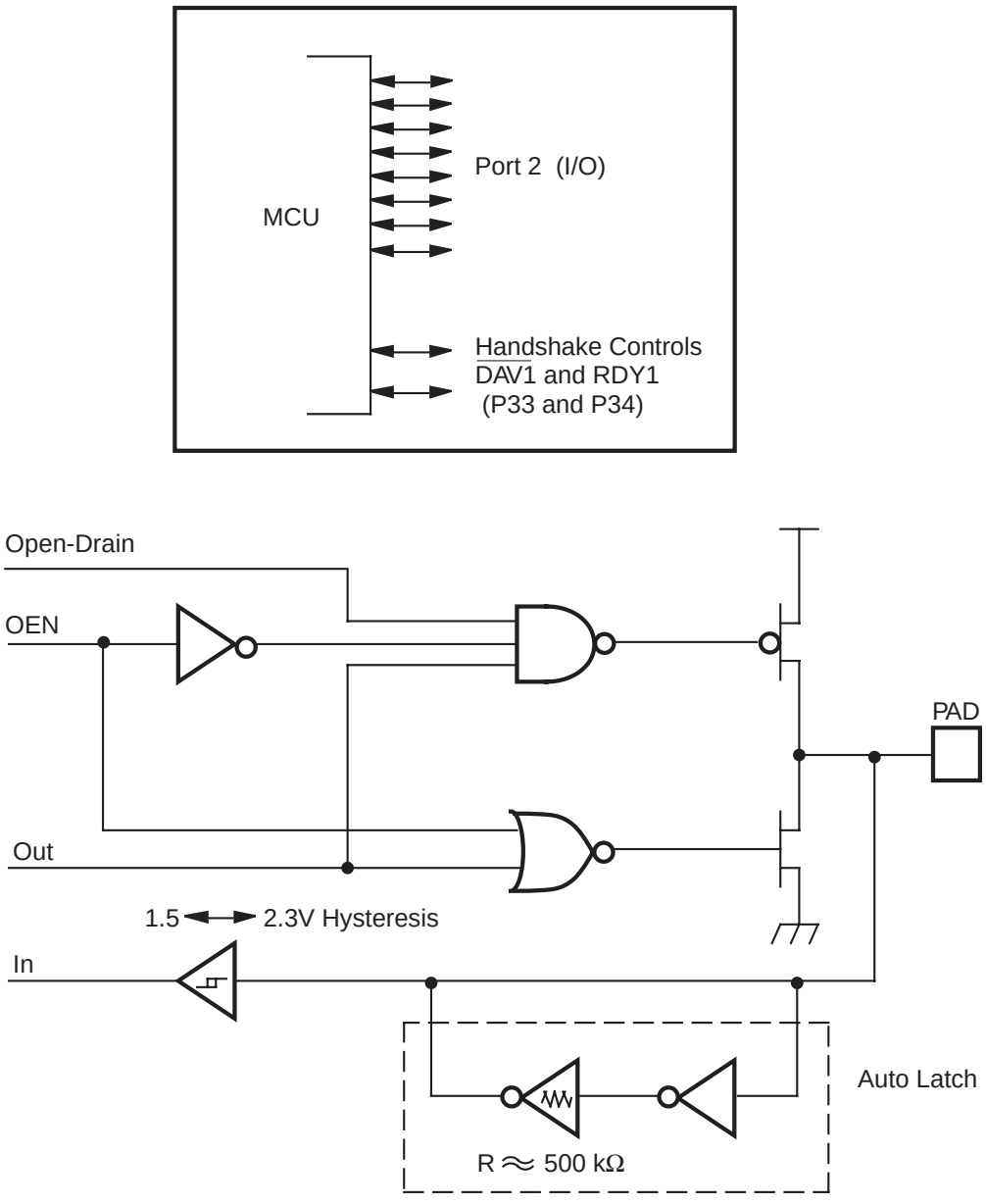


Figure 19. Port 1 Configuration (Z86E40 Only)

FUNCTIONAL DESCRIPTION (Continued)

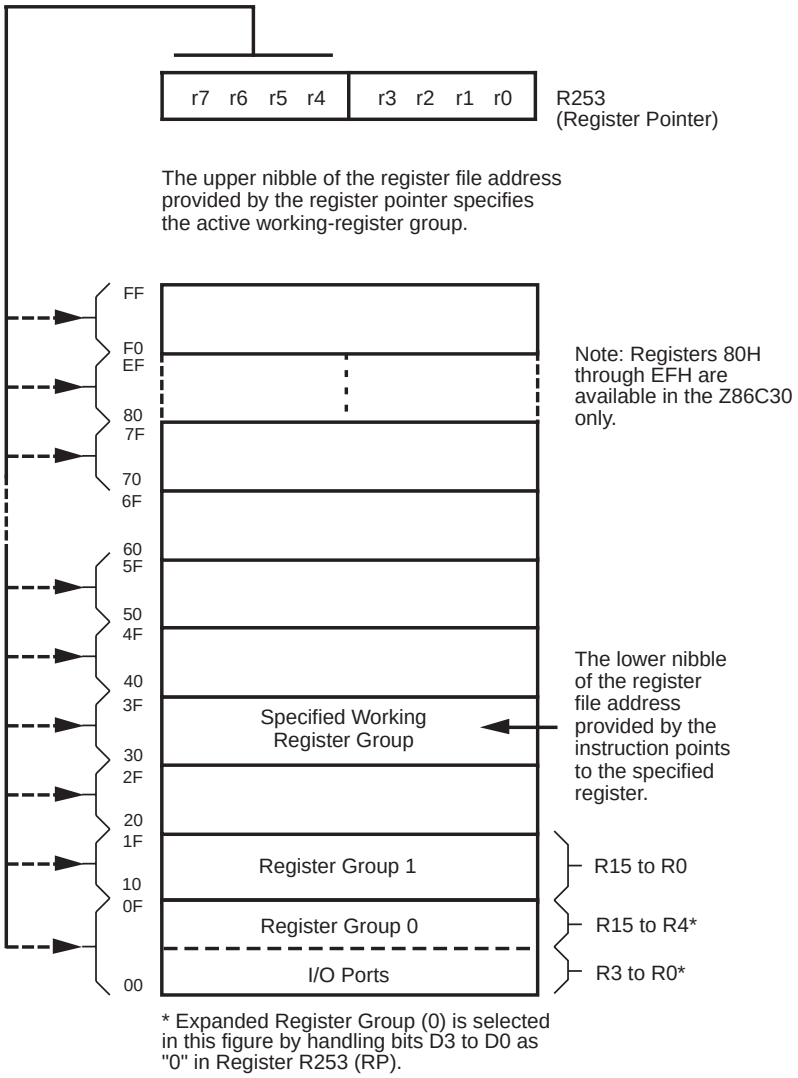


Figure 25. Register Pointer

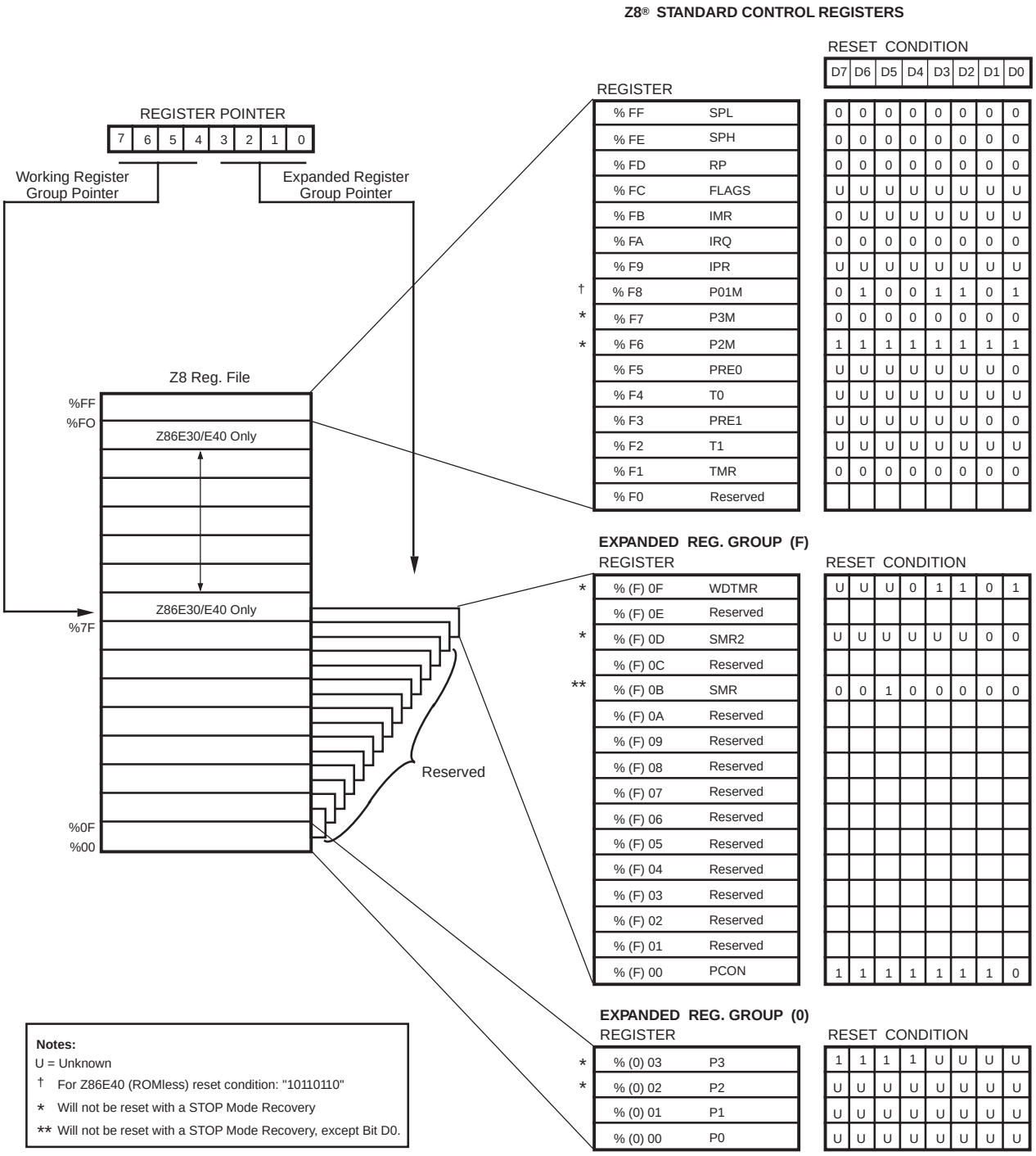


Figure 26. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The MCU has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 28). The six sources are divided as follows: four sources are claimed by Port 3 lines P33–P30) and two in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 10).

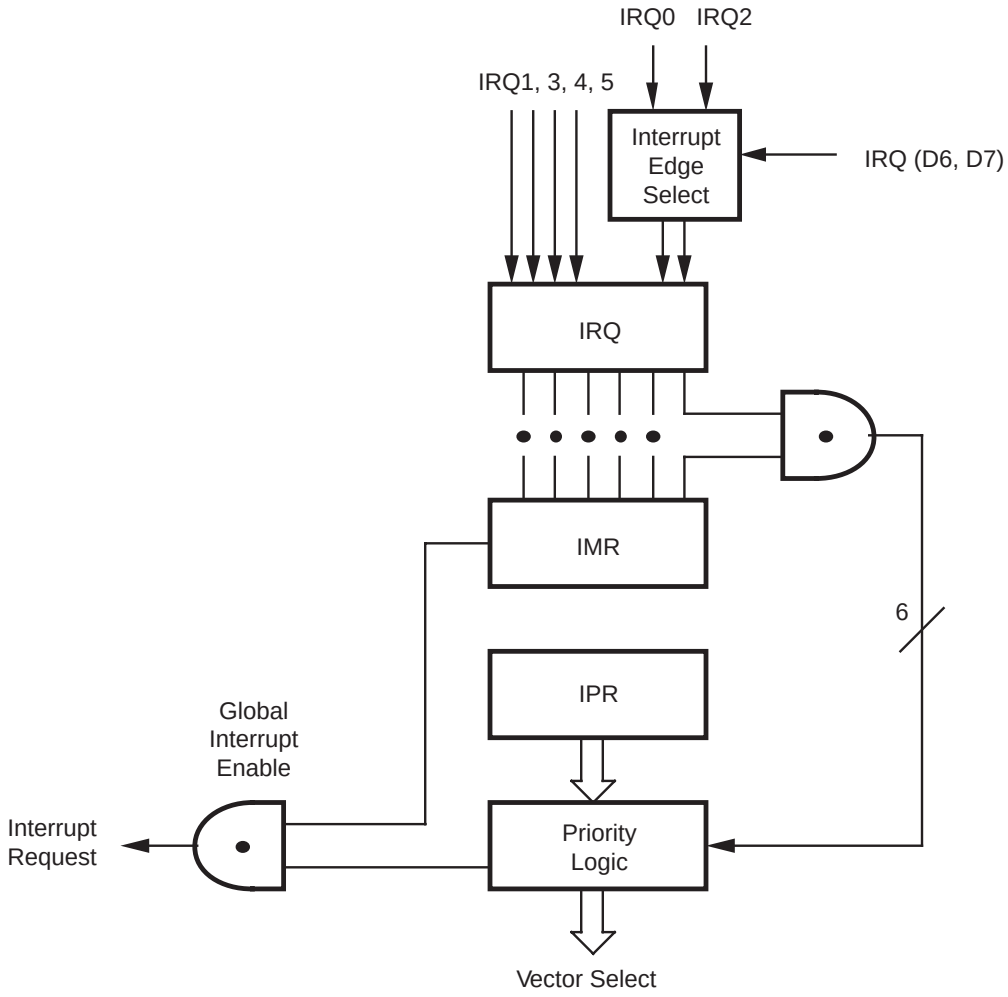


Figure 28. Interrupt Block Diagram

Table 10. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	$\overline{DAV0}$, IRQ0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	$\overline{DAV2}$, IRQ2, T_{IN}	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Falling Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	TI	10, 11	Internal

FUNCTIONAL DESCRIPTION (Continued)

Table 12. Stop-Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0–3
1	1	1	Logical NOR of Port 2 bits 0–7

Stop-Mode Recovery Delay Select (D5). The 5 ms RESET delay after Stop-Mode Recovery is disabled by programming this bit to a zero. A “1” in this bit will cause a 5 ms RESET delay after Stop-Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the Stop-Mode Recovery source needs to be kept active for at least 5TpC.

Stop-Mode Recovery Level Select (D6). A “1” in this bit defines that a high level on any one of the recovery sources wakes the MCU from STOP Mode. A 0 defines low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A “0” in this bit indicates that the device has been reset by POR (cold). A “1” in this bit indicates the device was awakened by a SMR source (warm).

Stop-Mode Recovery Register 2 (SMR2). This register contains additional Stop-Mode Recovery sources. When the Stop-Mode Recovery sources are selected in this register then SMR Register. Bits D2, D3, and D4 must be 0.

SMR:10		Operation
D1	**D0**	**Description of Action**
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is disabled after Power-On Reset and initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT is driven either by an on-board RC oscillator or an external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register.

Note: Execution of the WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags.

WDT Time-Out Period (D0 and D1). Bits 0 and 1 control a tap circuit that determines the time-out periods that can be obtained (Table 13). The default value of D0 and D1 are 1 and 0, respectively.

Table 13. Time-out Period of WDT

D1	D0	Time-out of the Internal RC OSC	Time-out of the System Clock
0	0	5 ms	128 SCLK
0	1	10 ms*	256 SCLK*
1	0	20 ms	512 SCLK
1	1	80 ms	2048 SCLK

Notes:
*The default setting is 10 ms.

WDT During HALT Mode (D2). This bit determines whether or not the WDT is active during HALT Mode. A “1” indicates that the WDT is active during HALT. A “0” disables the WDT in HALT Mode. The default value is “1”.

WDT During STOP Mode (D3). This bit determines whether or not the WDT is active during STOP mode. A “1” indicates active during STOP. A “0” disables the WDT during STOP Mode. This is applicable only when the WDT clock source is the internal RC oscillator.

Clock Source For WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1, and the WDT is stopped in STOP Mode. The default configuration of this bit is 0, which selects the RC oscillator.

Permanent WDT. When this feature is enabled, the WDT is enabled after reset and will operate in Run and Halt Mode. The control bits in the WDTMR do not affect the WDT operation. If the clock source of the WDT is the internal RC oscillator, then the WDT will run in STOP mode. If the clock source of the WDT is the XTAL1 pin, then the WDT will not run in STOP mode.

Note: WDT time-out in STOP Mode will not reset SMR,SMR2,PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers.

WDTMR Register Accessibility. The WDTMR register is accessible only during the **first 60** internal system clock

FUNCTIONAL DESCRIPTION (Continued)

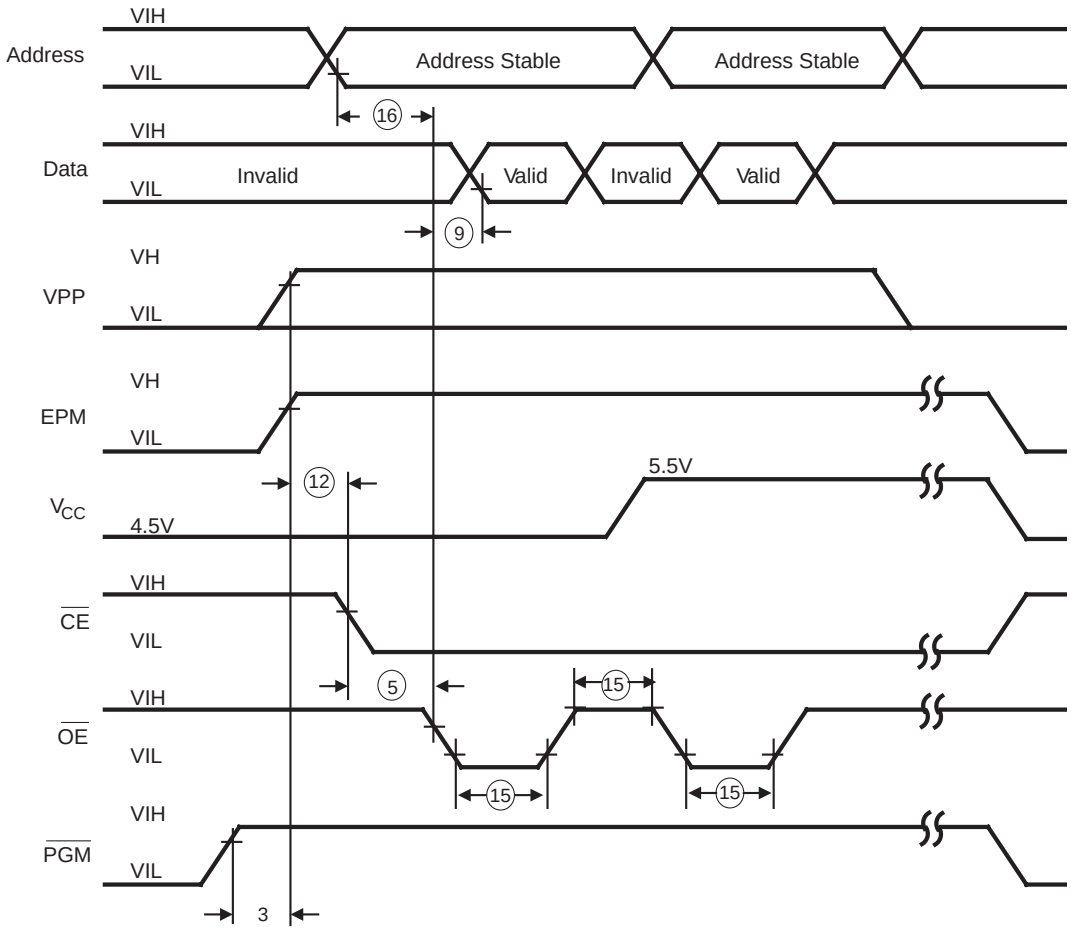


Figure 36. EPROM Read Mode Timing Diagram

Z8 CONTROL REGISTER DIAGRAMS (Continued)

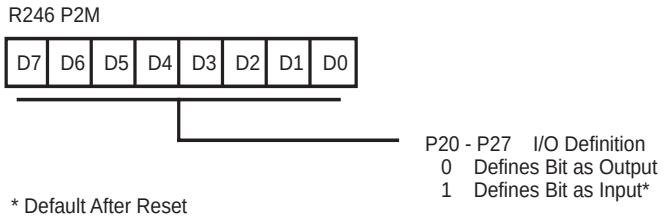


Figure 51. Port 2 Mode Register
F6H: Write Only

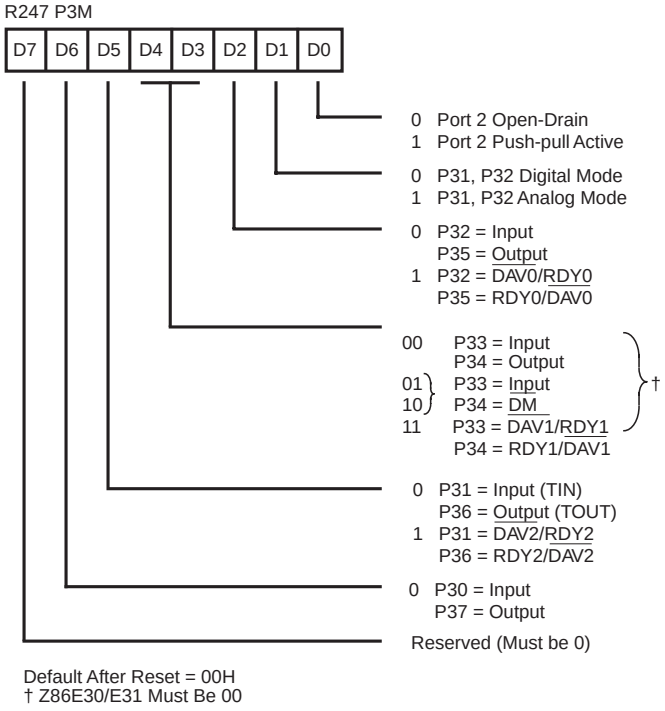


Figure 52. Port 3 Mode Register
F7H: Write Only

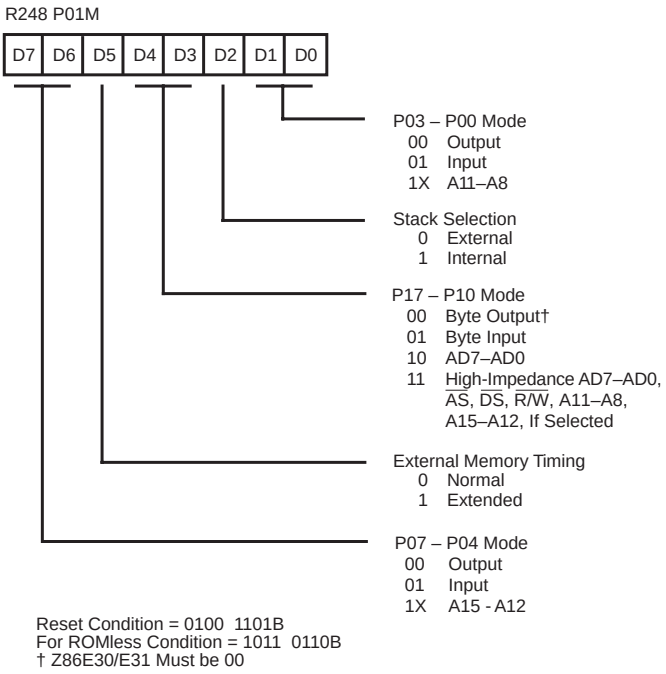


Figure 53. Port 0 and 1 Mode Register
F8H: Write Only
Z86E30/E31 Only

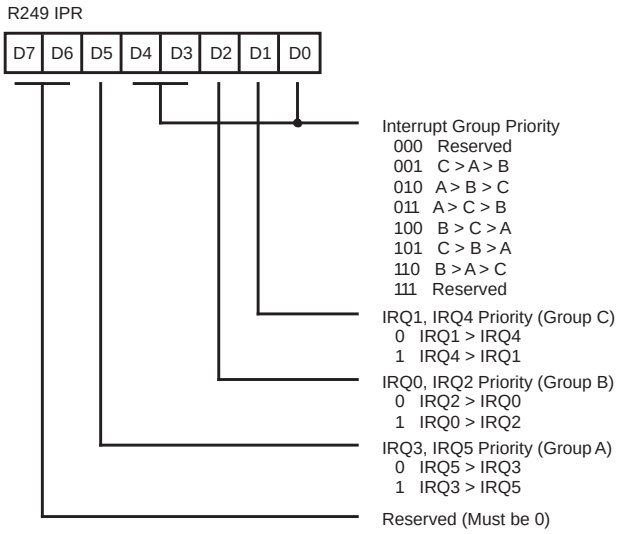
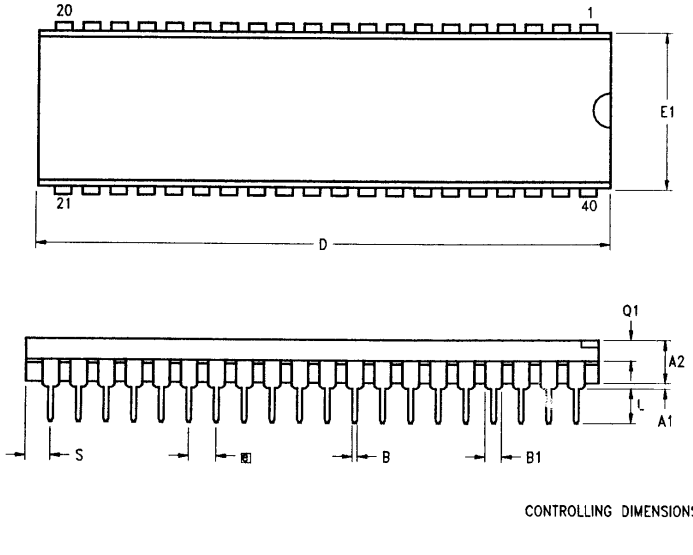


Figure 54. Interrupt Priority Register
F9H: Write Only

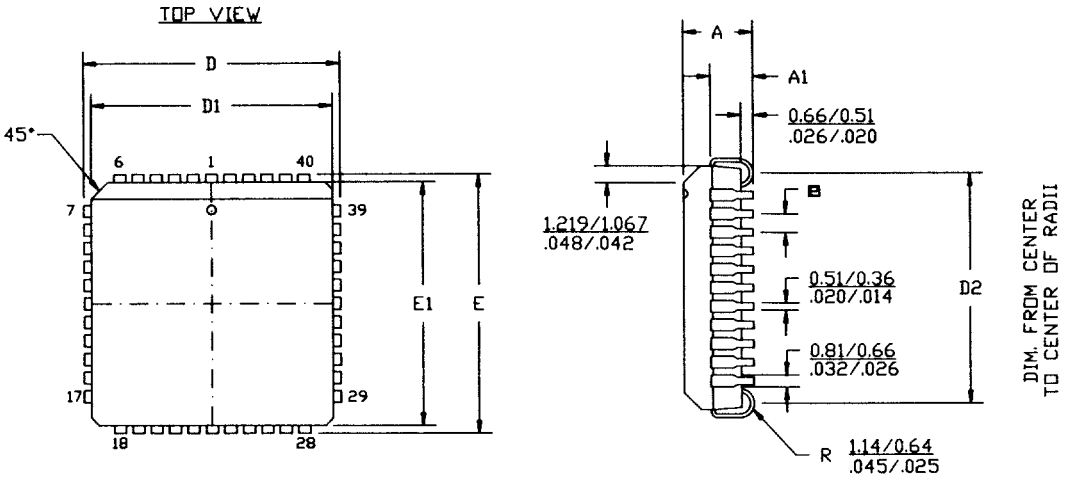
PACKAGE INFORMATION (Continued)

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

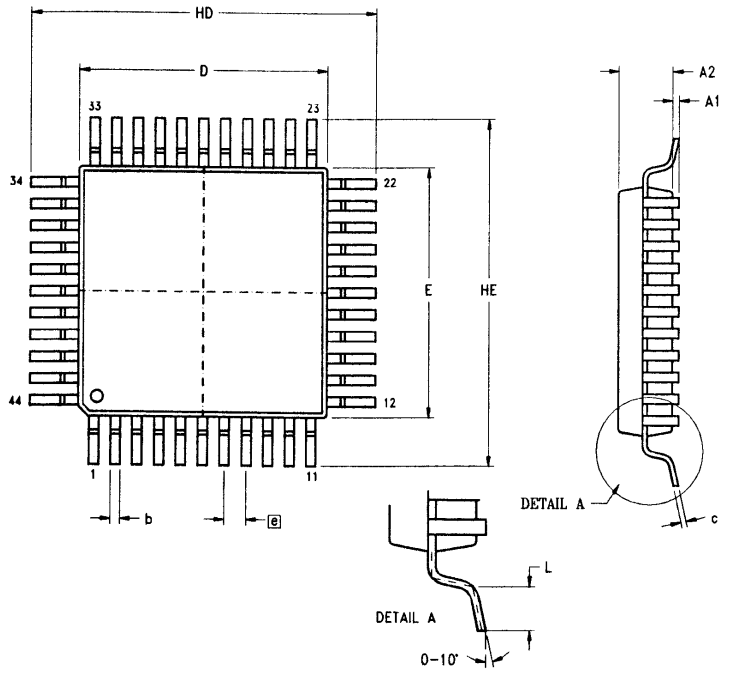
Figure 61. 40-Pin DIP Package Diagram



NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.41	2.92	.095	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

Figure 62. 44-Pin PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

Figure 63. 44-Pin LQFP Package Diagram

Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.