Zilog - Z86E4016VSC00TR Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e4016vsc00tr

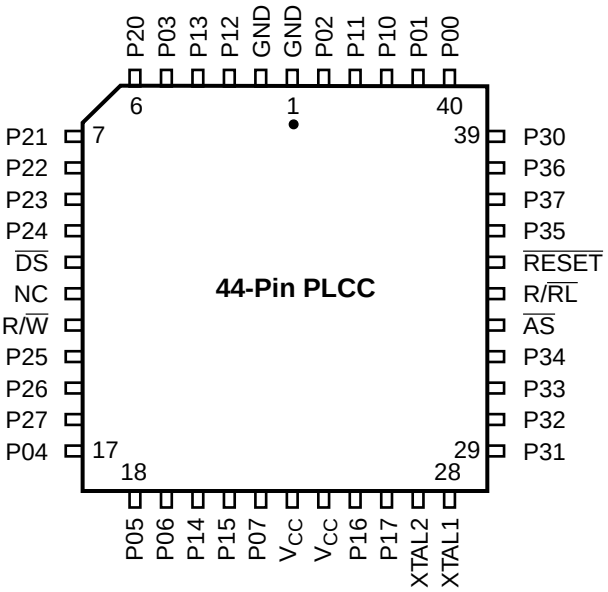


Figure 4. 44-Pin PLCC Pin Configuration
Standard Mode

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1–2	GND	Ground	
3–4	P12–P13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6–10	P20–P24	Port 2, Pins 0,1,2,3,4	In/Output
11	$\overline{DS}$	Data Strobe	Output
12	NC	No Connection	
13	R/$\overline{W}$	Read/Write	Output
14–16	P25–P27	Port 2, Pins 5,6,7	In/Output
17–19	P04–P06	Port 0, Pins 4,5,6	In/Output
20–21	P14–P15	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23–24	V_{CC}	Power Supply	
25–26	P16–P17	Port 1, Pins 6,7	In/Output
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29–31	P31–P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
33	$\overline{AS}$	Address Strobe	Output
34	R/$\overline{RL}$	ROM/ROMless select	Input
35	$\overline{RESET}$	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40–41	P00–P01	Port 0, Pins 0,1	In/Output
42–43	P10–P11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

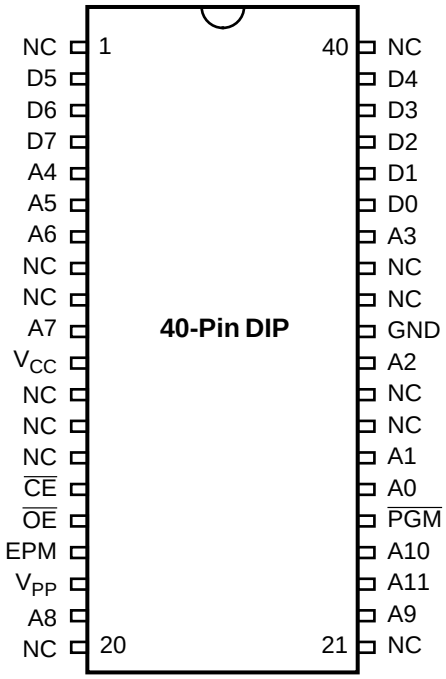


Figure 6. 40-Pin DIP Pin Configuration EPROM Mode

Table 4. 40-Pin DIP Package Pin Identification EPROM Mode

Pin #	Symbol	Function	Direction
1	NC	No Connection	
2–4	D5–D7	Data 5,6,7	In/Output
5–7	A4–A6	Address 4,5,6	Input
8–9	NC	No Connection	
10	A7	Address 7	Input
11	V_{CC}	Power Supply	
12–14	NC	No Connection	
15	$\overline{CE}$	Chip Select	Input
16	$\overline{OE}$	Output Enable	Input
17	EPM	EPROM Prog. Mode	Input
18	V_{PP}	Prog. Voltage	Input
19	A8	Address 8	Input
20–21	NC	No Connection	
22	A9	Address 9	Input
23	A11	Address 11	Input
24	A10	Address 10	Input
25	$\overline{PGM}$	Prog. Mode	Input
26–27	A0–A1	Address 0,1	Input
28–29	NC	No Connection	
30	A2	Address 2	Input
31	GND	Ground	
32–33	NC	No Connection	
34	A3	Address 3	Input
35–39	D0–D4	Data 0,1,2,3,4	In/Output
40	NC	No Connection	

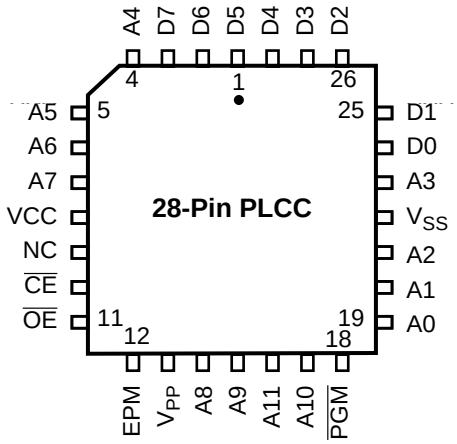


Figure 12. EPROM Programming Mode 28-Pin PLCC Pin Configuration

Table 8. 28-Pin EPROM Pin Identification

Pin #	Symbol	Function	Direction
1–3	D5–D7	Data 5,6,7	In/Output
4–7	A4–A7	Address 4,5,6,7	Input
8	V_{CC}	Power Supply	
9	NC	No connection	
10	$\overline{CE}$	Chip Select	Input
11	$\overline{OE}$	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V_{PP}	Prog. Voltage	Input
14–15	A8–A9	Address 8,9	Input
16	A11	Address 11	Input
17	A10	Address 10	Input
18	$\overline{PGM}$	Prog. Mode	Input
19–21	A0–A2	Address 0,1,2	Input
22	V_{SS}	Ground	
23	A3	Address 3	Input
24–28	D0–D4	Data 0,1,2,3,4	In/Output

DC ELECTRICAL CHARACTERISTICS (Continued)

			T_A=–40 °C to +105 °C					
Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{ALH}	Auto Latch High Current	4.5V	-1.0	-10	-3.8	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V	-1.0	-10	-3.8	µA	$0V < V_{IN} < V_{CC}$	9
T_{POR}	Power On Reset	4.5V	2.0	14	4	mS		
		5.5V	2.0	14	4	mS		
V_{LV}	Auto Reset Voltage		2.0	3.3	2.9	V		1

1. Device does function down to the Auto Reset voltage.
2. GND=0V
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1= CL2 = 22 pF
6. Same as note [4] except inputs at V_{CC}.
7. Maximum temperature is 70°C
8. STD Mode (not Low EMI Mode)
9. Auto Latch (mask option) selected
10. For analog comparator inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.
12. Typicals are at V_{CC} = 5.0V
13. Z86E40 only
14. WDT is not running.

Additional Timing Table

				T_A = -40 °C to +105 °C 16 MHz				
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Units	Conditions	Notes
1	TpC	Input Clock Period	3.5V	62.5	DC	ns		1,7,8
			5.5V	62.5	DC	ns		1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15	ns		1,7,8
			5.5V		15	ns		1,7,8
3	TwC	Input Clock Width	3.5V	31		ns		1,7,8
			5.5V	31		ns		1,7,8
4	TwTinL	Timer Input Low Width	3.5V	70		ns		1,7,8
			5.5V	70		ns		1,7,8
5	TwTinH	Timer Input High Width	3.5V	5TpC				1,7,8
			5.5V	5TpC				1,7,8
6	TpTin	Timer Input Period	3.5V	8TpC				1,7,8
			5.5V	8TpC				1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100	ns		1,7,8
			5.5V		100	ns		1,7,8
8A	TwIL	Int. Request Low Time	3.5V	70		ns		1,2,7,8
			5.5V	70		ns		1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V	5TpC				1,3,7,8
			5.5V	5TpC				1,3,7,8
9	TwIH	Int. Request Input High Time	3.5V	5TpC				1,2,7,8
			5.5V					
10	Twsm	STOP Mode Recovery Width Spec	3.5V	12		ns		4,8
			5.5V	12		ns		4,8
11	Tost	Oscillator Startup Time	3.5V		5TpC			4,8
			5.5V		5TpC			4,8
12	Twdt	Watch-Dog Timer Delay Time Before Timeout	3.5V	10		ms	D0 = 0	5,11
			5.5V	5		ms	D1 = 0	5,11
			3.5V	20		ms	D0 = 1	5,11
			5.5V	10		ms	D1 = 0	5,11
			3.5V	40		ms	D0 = 0	5,11
			5.5V	20		ms	D1 = 1	5,11
			3.5V	160		ms	D0 = 1	5,11
			5.5V	80		ms	D1 = 1	5,11

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31–P33)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Reg. WDTMR
6. The V_{CC} voltage spec. of 5.5V guarantees 5.0V ± 0.5V.
7. SMR D1 = 0
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
9. For RC and LC oscillator, and for oscillator driven by clock driver.
10. Standard Mode (not Low EMI output ports)
11. Using internal RC

Port 0 (P07–P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble programmed. Either nibble output that can be globally programmed as push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can be placed under handshake control. In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. In ROMless mode, after a hardware reset, Port 0 is configured as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode. In ROM mode, Port 0 is defined as input after reset.

Port 0 can be set in the High-Impedance Mode if selected as an address output state, along with Port 1 and the control signals $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$ (Figure 18).

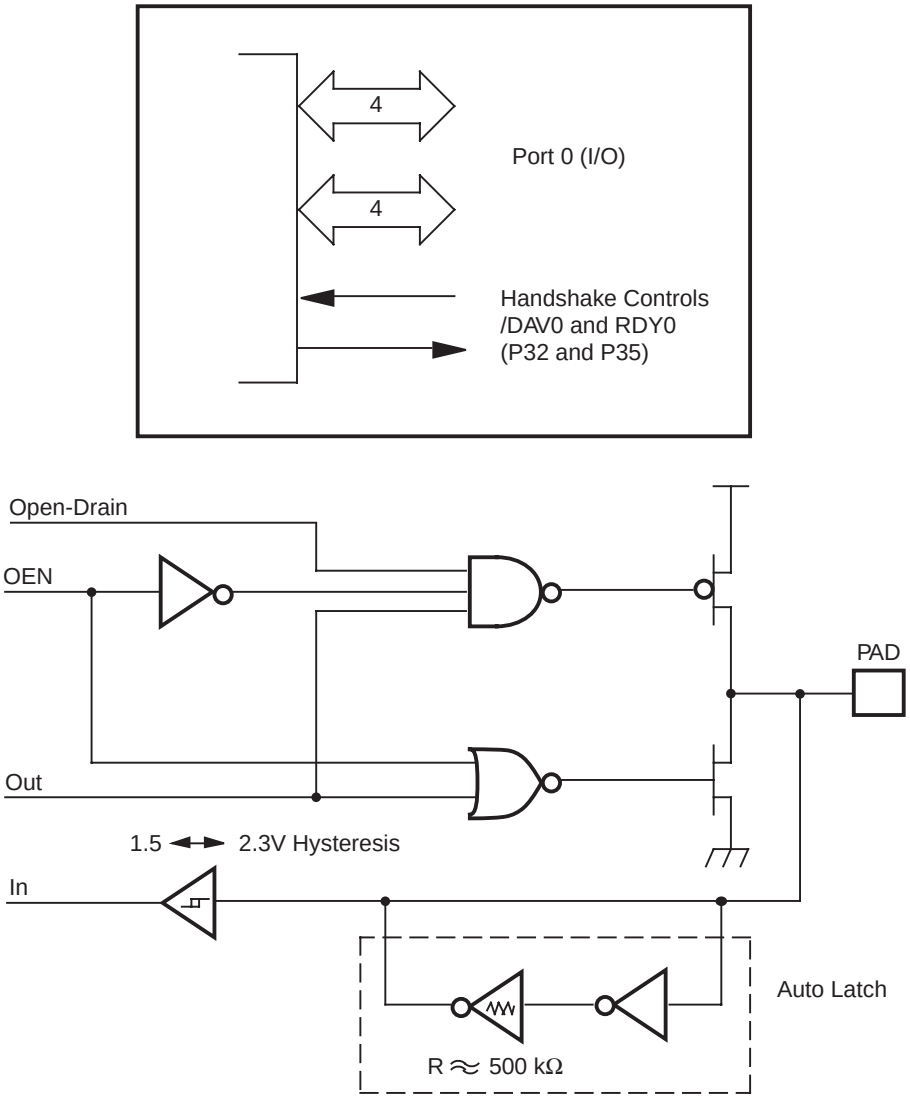


Figure 18. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P17–P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7–A0) and Data (D7–D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and /DAV1 (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (Figure 19).

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z86E40 to share common resources in multiprocessor and DMA applications.

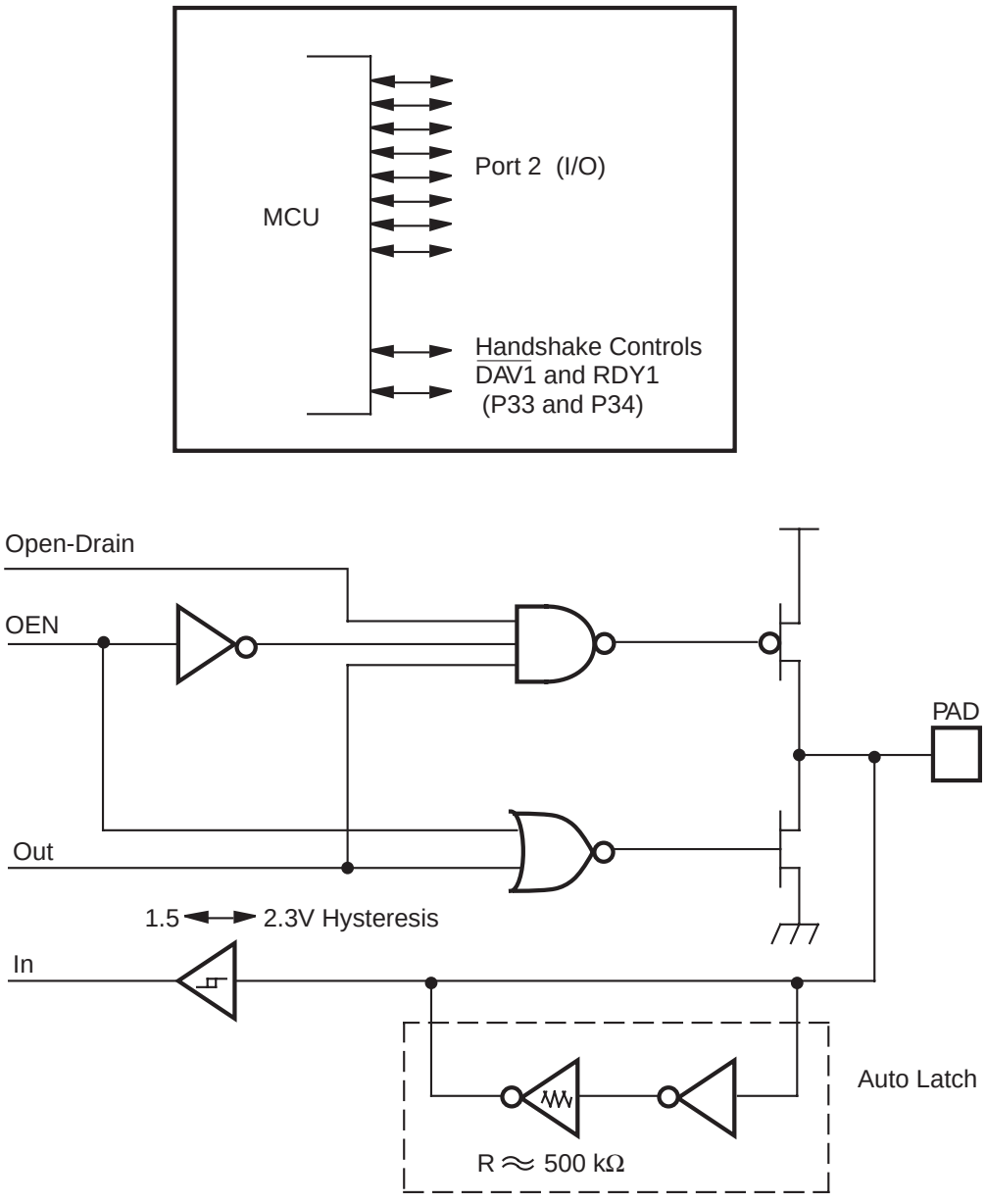


Figure 19. Port 1 Configuration (Z86E40 Only)

FUNCTIONAL DESCRIPTION

The MCU incorporates the following special functions to enhance the standard Z8 architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of three ways:

1. Power-On Reset
2. Watch-Dog Timer
3. STOP-Mode Recovery Source

Note: Having the Auto Power-On Reset circuitry built-in, the MCU does not need to be connected to an external power-on reset circuit. The reset time is 5 ms (typical). The MCU does not reinitialize WDTMR, SMR, P2M, and P3M registers to their reset values on a STOP-Mode Recovery operation.

Note: The device V_{CC} must rise up to the operating V_{CC} specification before the TPOR expires.

Program Memory. The MCU can address up to 4 KB of Internal Program Memory (Figure 22). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 12 (000CH) to address 4095 (0FFFH) consists of programmable EPROM. After reset, the program counter points at the address 000CH, which is the starting address of the user program.

In ROMless mode, the Z86E40 can address up to 64 KB of External Program Memory. The ROM/ROMless option is only available on the 44-pin devices.

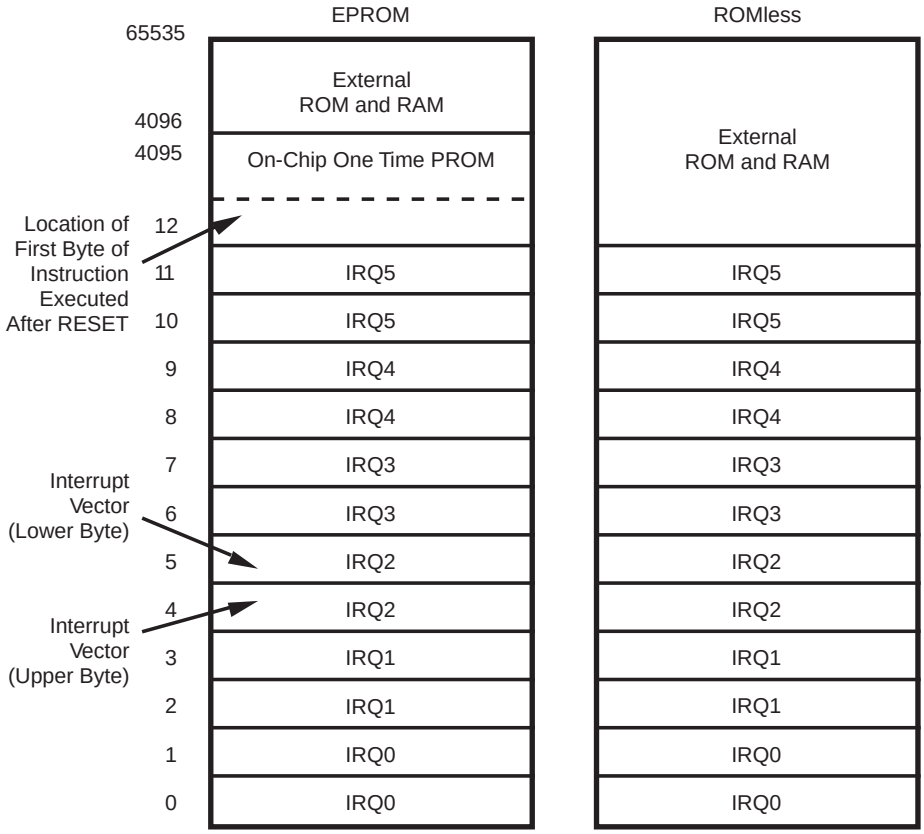


Figure 22. Program Memory Map (ROMless Z86E40 Only)

EPROM Protect. When in ROM Protect Mode, and executing out of External Program Memory, instructions LDC, LDCI, LDE, and LDEI cannot read Internal Program Memory.

When in ROM Protect Mode and executing out of Internal Program Memory, instructions LDC, LDCI, LDE, and LDEI can read Internal Program Memory.

Register File. The register file consists of three I/O port registers, 236/125 general-purpose registers, 15 control and status registers, and three system configuration registers in the expanded register group. The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 24). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Bank E0–EF can only be accessed through working register and indirect addressing modes. (This bank is available in Z86E30/E40 only.)

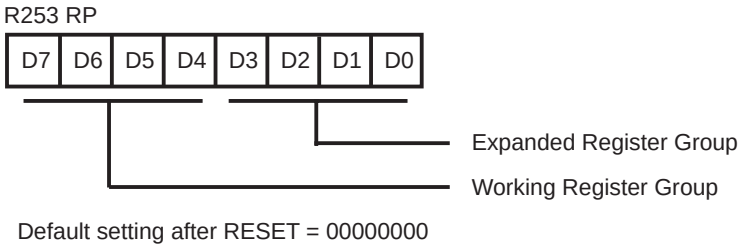


Figure 24. Register Pointer Register

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 26). These register groups are known as the Expanded Register File (ERF).

The low nibble (D3–D0) of the Register Pointer (RP) select the active ERF group, and the high nibble (D7–D4) of register RP select the working register group. Three system configuration registers reside in the Expanded Register File at bank FH: PCON, SMR, and WDTMR. The rest of the Expanded Register is not physically implemented and is reserved for future expansion.

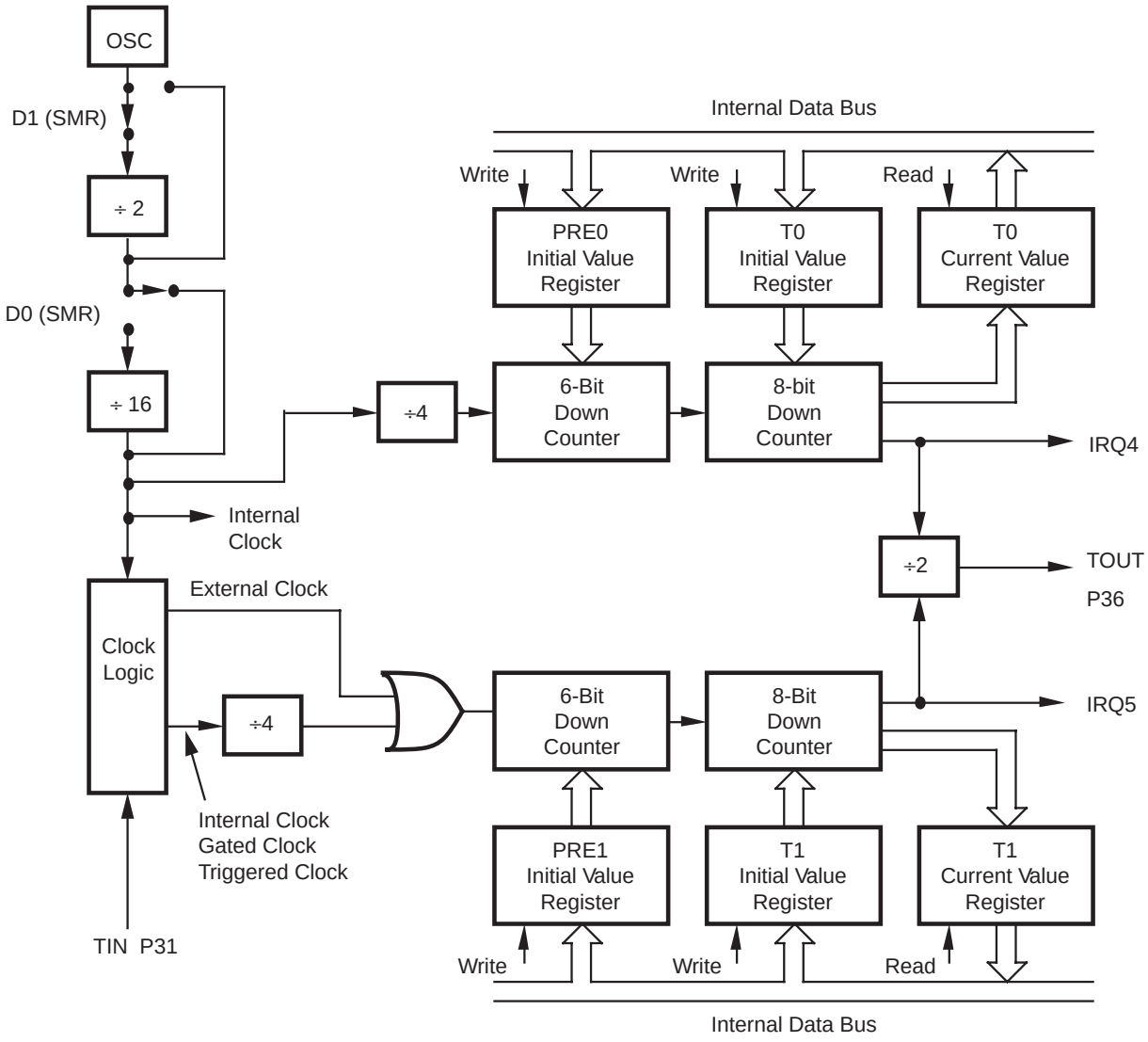


Figure 27. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

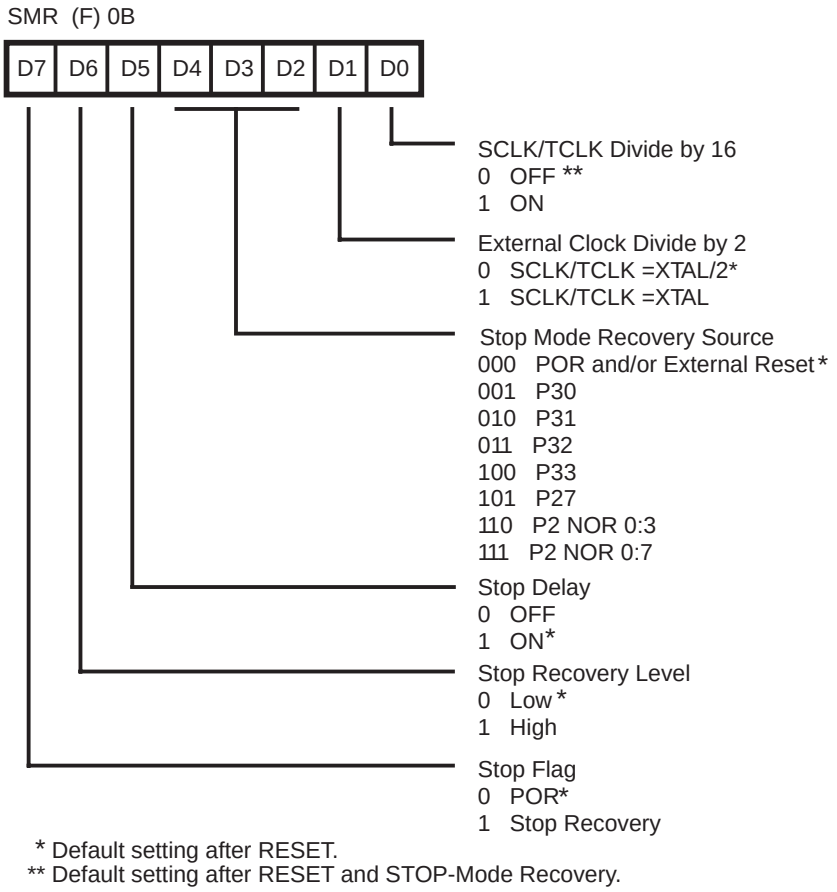


Figure 31. STOP-Mode Recovery Register (Write-Only Except Bit D7, Which is Read-Only)

FUNCTIONAL DESCRIPTION (Continued)

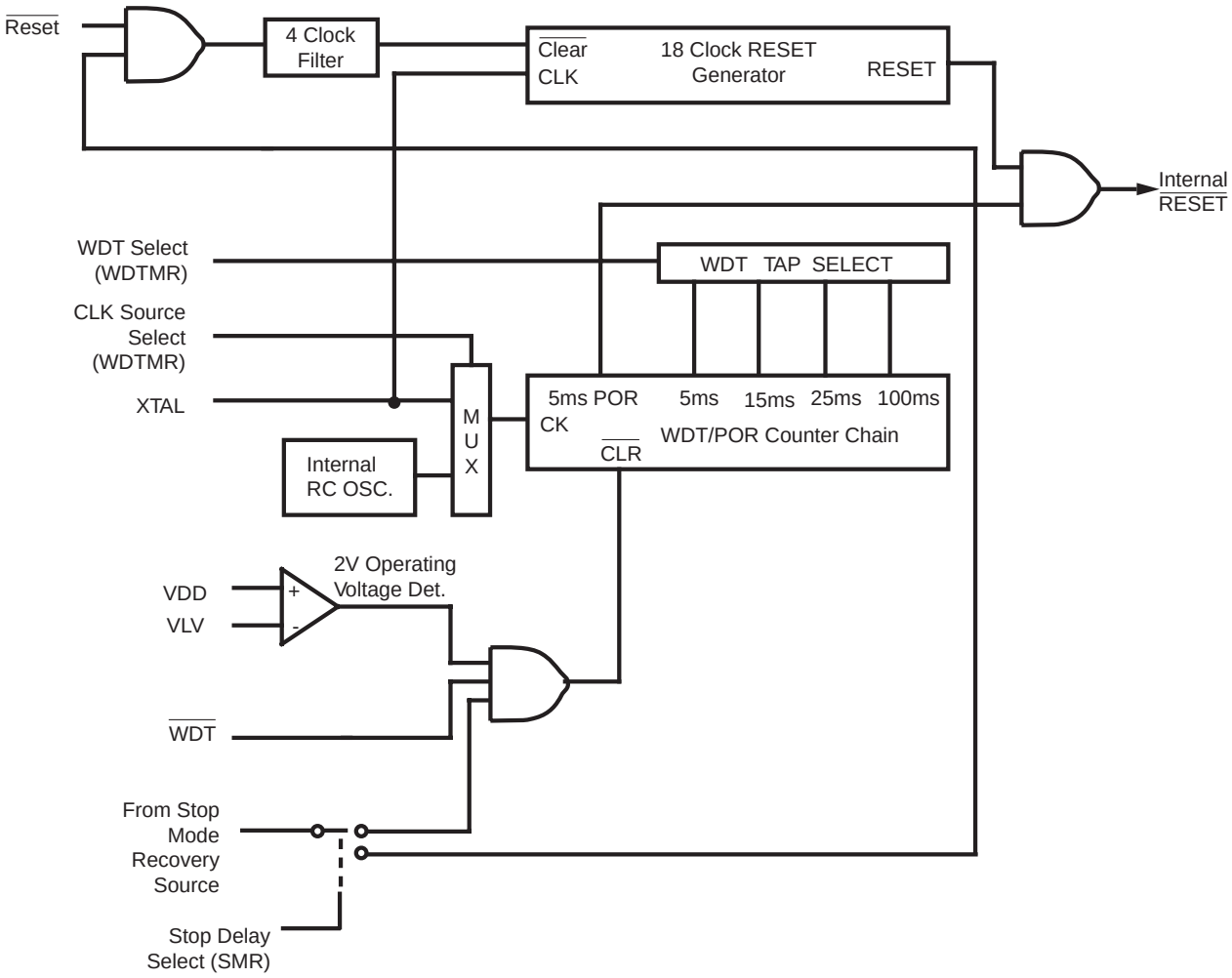


Figure 34. Resets and WDT

Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{LV} (Figure 35).

Note: V_{CC} must be in the allowed operating range prior to the minimum Power-On Reset time-out (T_{POR}).

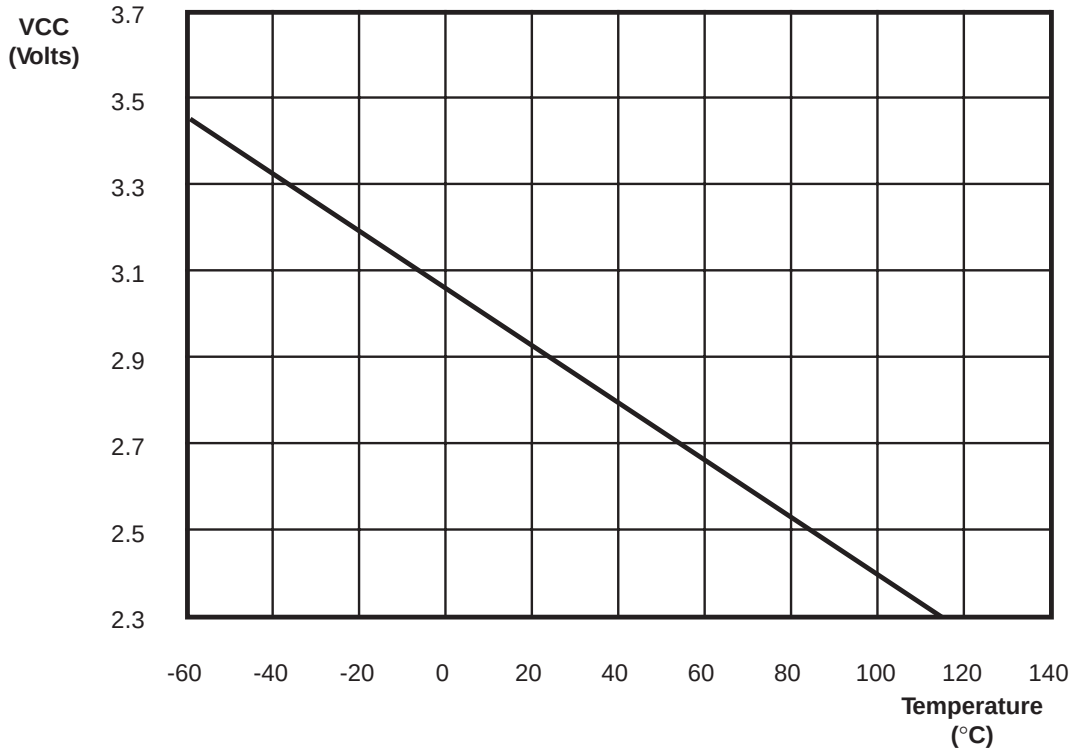


Figure 35. Typical Z86E40 V_{LV} Voltage vs. Temperature

FUNCTIONAL DESCRIPTION (Continued)

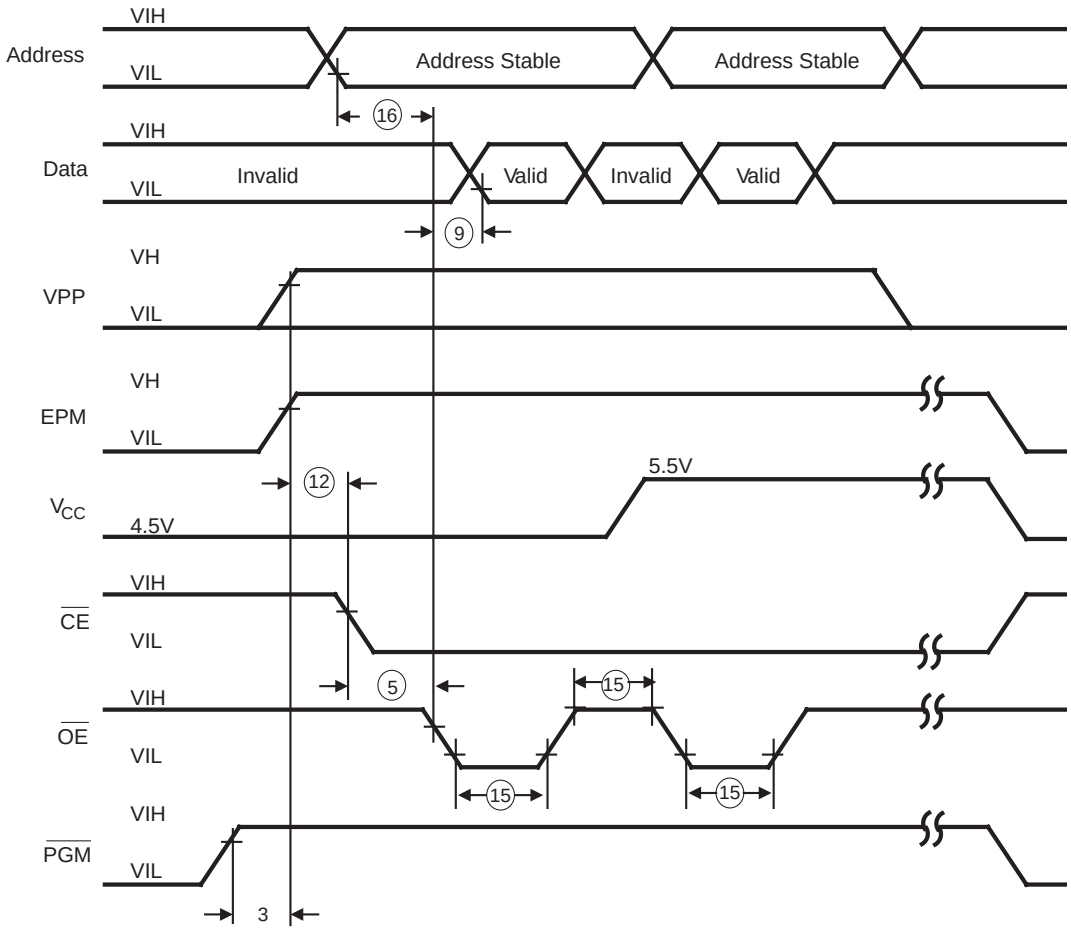


Figure 36. EPROM Read Mode Timing Diagram

Z8 CONTROL REGISTER DIAGRAMS (Continued)

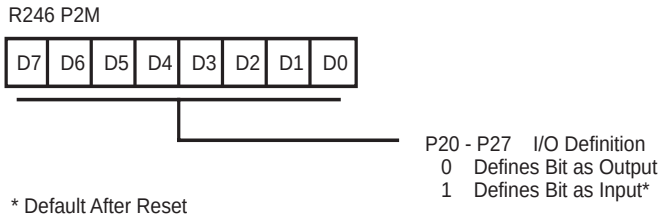


Figure 51. Port 2 Mode Register
F6H: Write Only

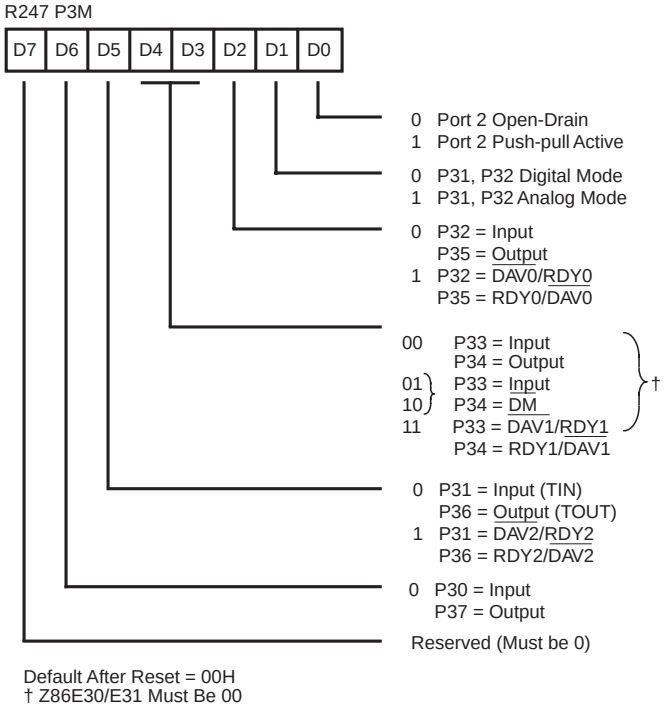


Figure 52. Port 3 Mode Register
F7H: Write Only

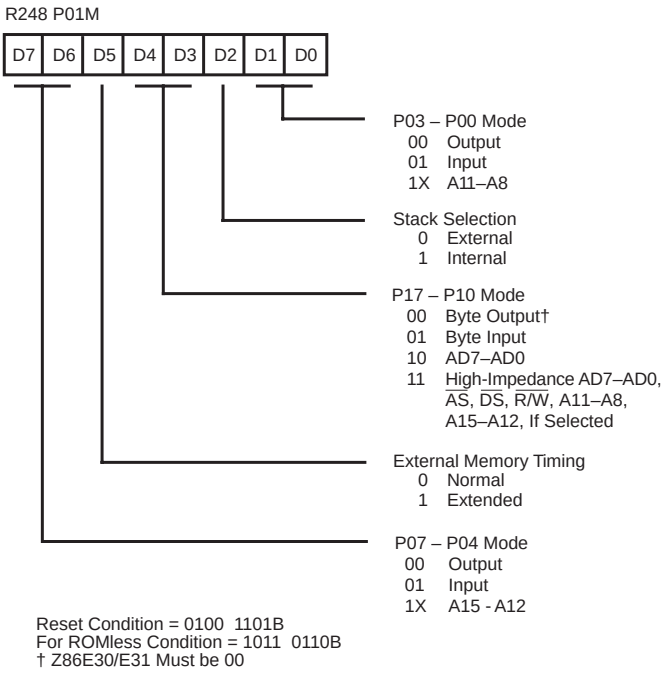


Figure 53. Port 0 and 1 Mode Register
F8H: Write Only
Z86E30/E31 Only

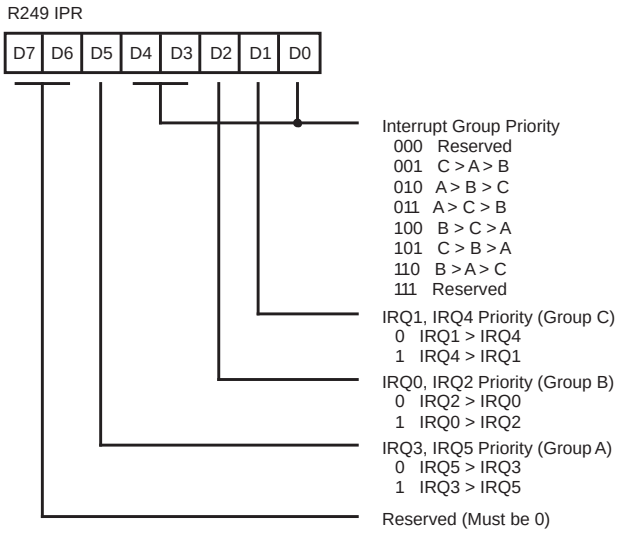


Figure 54. Interrupt Priority Register
F9H: Write Only

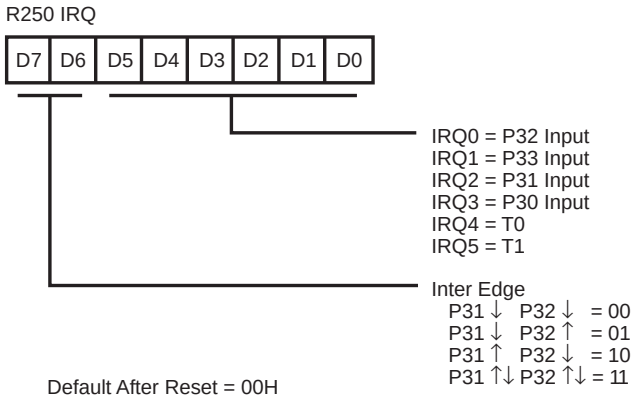
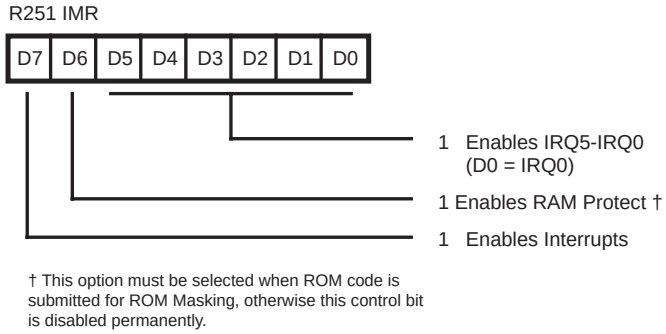


Figure 55. Interrupt Request Register
FAH: Read/Write



† This option must be selected when ROM code is submitted for ROM Masking, otherwise this control bit is disabled permanently.

Figure 56. Interrupt Mask Register
FBH: Read/Write

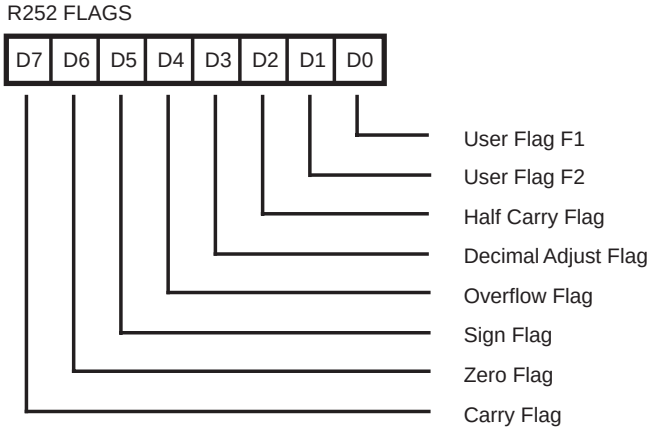


Figure 57. Flag Register
FCH: Read/Write

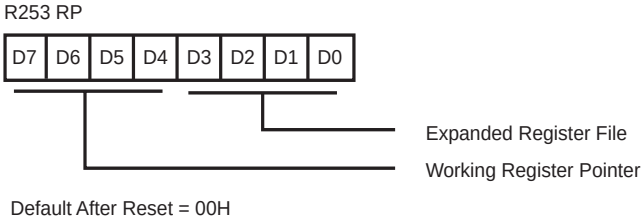


Figure 58. Register Pointer
FDH: Read/Write

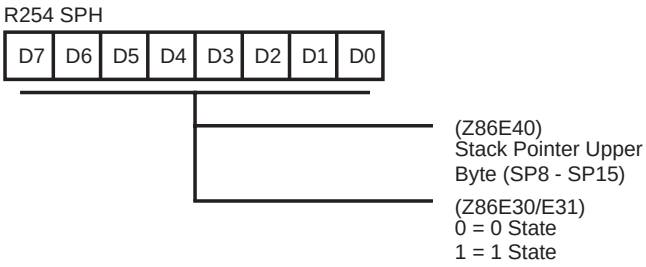


Figure 59. Stack Pointer High
FEH: Read/Write

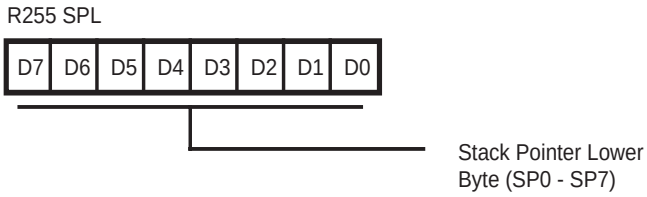
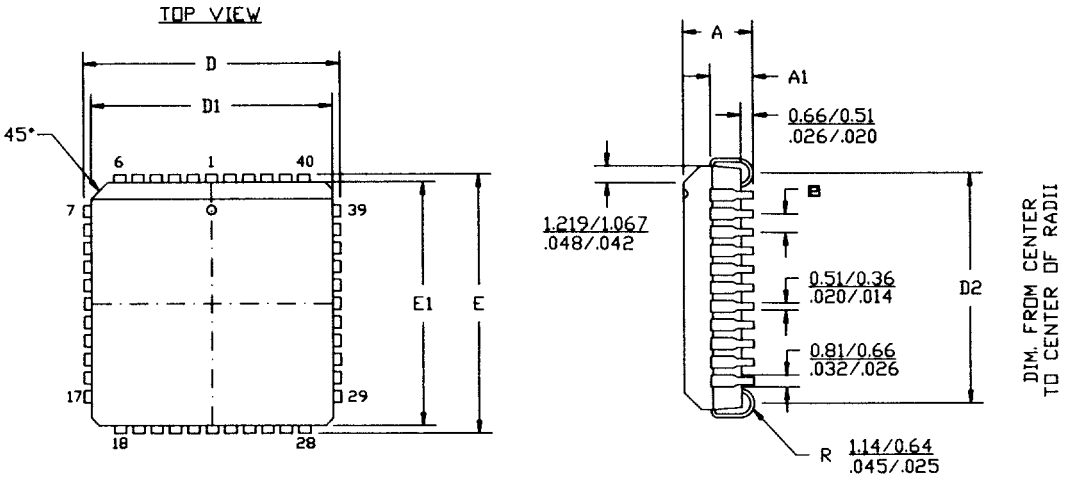


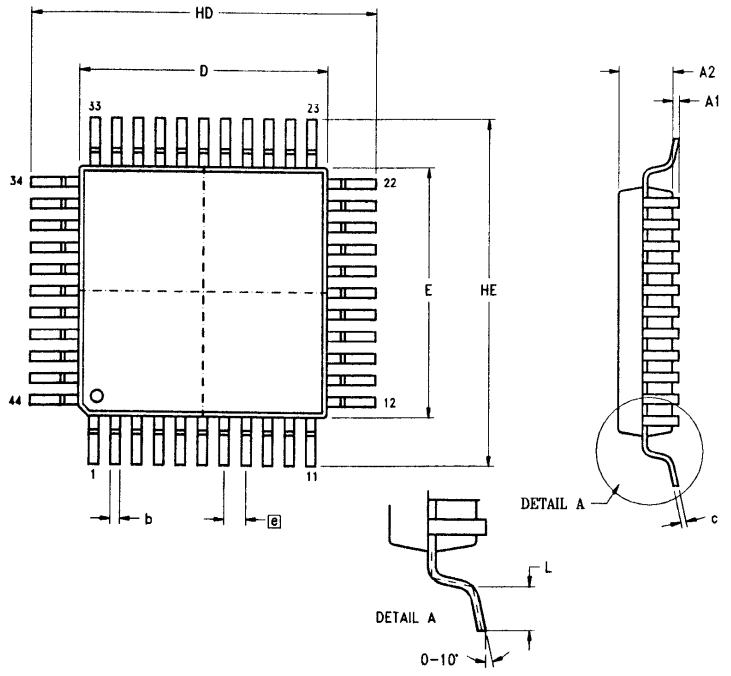
Figure 60. Stack Pointer Low
FFH: Read/Write



NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.41	2.92	.095	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

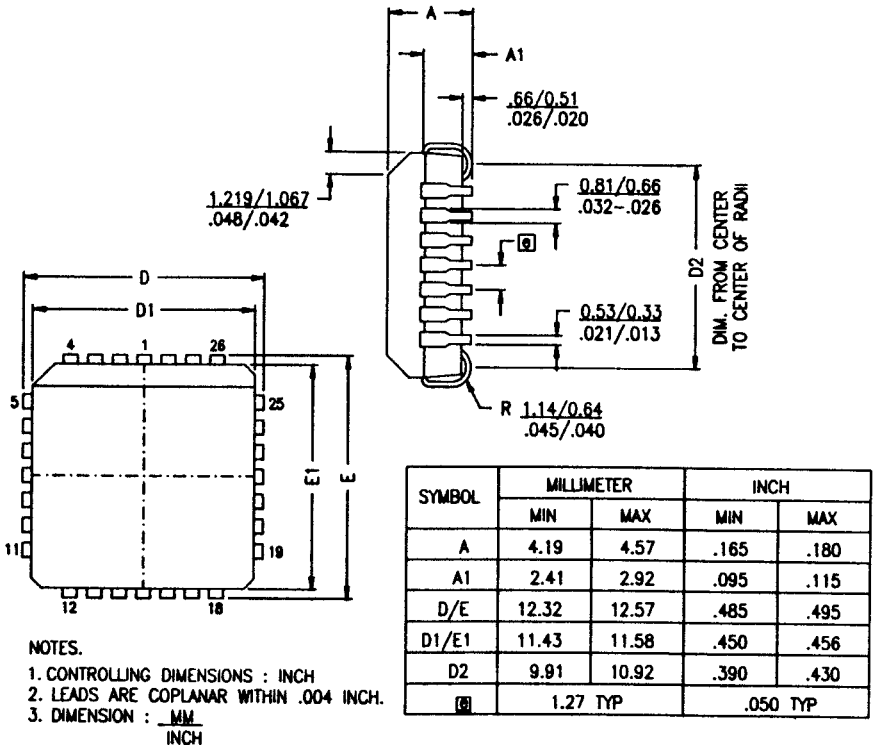
Figure 62. 44-Pin PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

Figure 63. 44-Pin LQFP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.19	4.57	.165	.180
A1	2.41	2.92	.095	.115
D/E	12.32	12.57	.485	.495
D1/E1	11.43	11.58	.450	.456
D2	9.91	10.92	.390	.430
e	1.27 TYP		.050 TYP	

Figure 66. 28-Pin PLCC Package Diagram

ORDERING INFORMATION

Z86E40 (16 MHz)

40-Pin DIP	44-Pin PLCC	44-Pin LQFP
Z86E4016PSC	Z86E4016VSC	Z86E4016FSC
Z86E4016PEC	Z86E4016VEC	Z86E4016FEC

Z86E30 (16 MHz)

28-Pin DIP	28-Pin SOIC	28-Pin PLCC
Z86E3016PSC	Z86E3016SSC	Z86E3016VSC
Z96E3016PEC	Z86E3016SEC	Z86E3016VEC

Z86E31 (16 MHz)

28-Pin DIP	28-Pin SOIC	28-Pin PLCC
Z86E3116PSC	Z86E3116SSC	Z86E3116VSC
Z86E3116PEC	Z86E3116SEC	Z86E3116VEC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package

P = Plastic DIP

V = Plastic Leaded Chip Carrier

F = Plastic Quad Flat Pack

S = SOIC (Small Outline Integrated Circuit)

Temperature

S = 0 °C to +70 °C
E = -40 °C to +105 °C

Speed

16 = 16 MHz

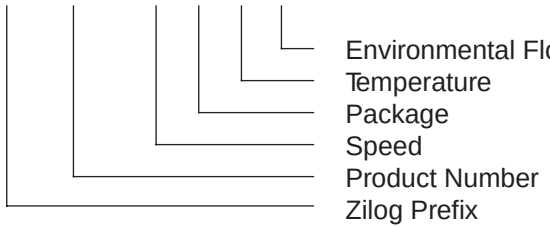
Environmental

C= Plastic Standard

E = Hermetic Standard

Example:

Z 86E40 16 P S C is a Z86E40, 16 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.