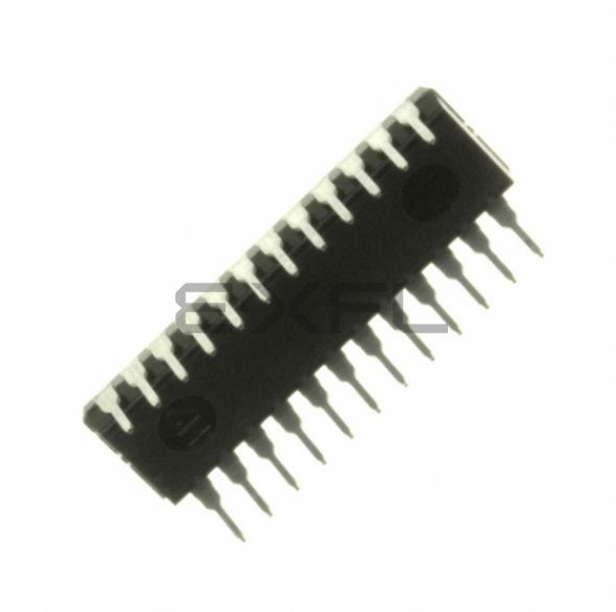

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	LINbus, LPC, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	496 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 6x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	24-SDIP (0.300", 7.62mm)
Supplier Device Package	24-SDIP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f203kp-g-sh-sne2

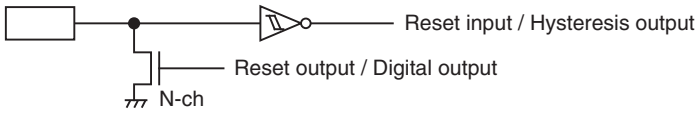
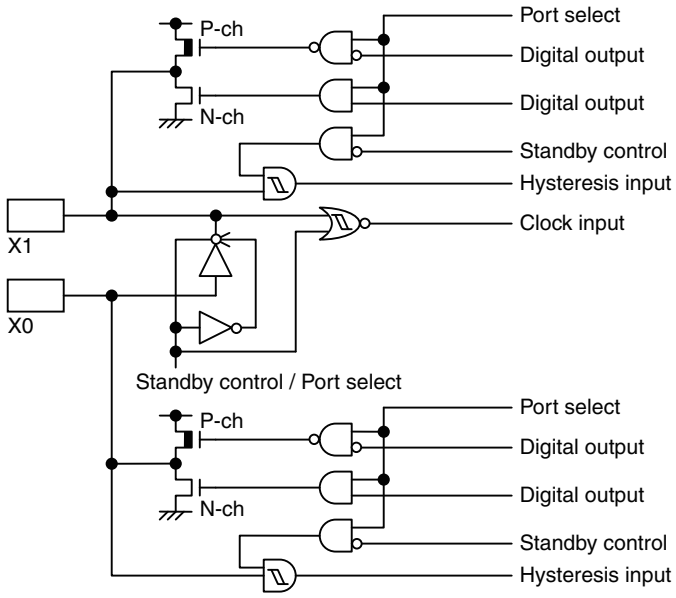
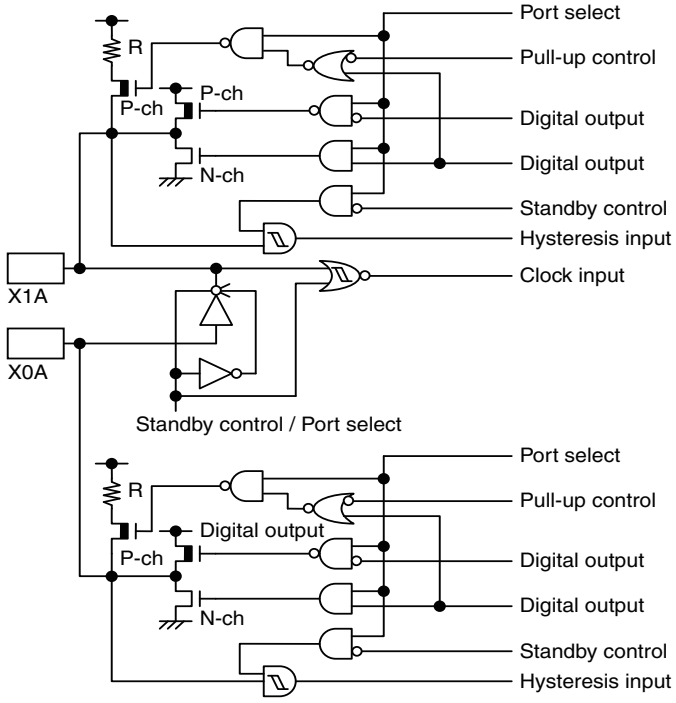
Contents

7. Pin Description (MB95210H Series)

Pin no.	Pin name	I/O circuit type*	Function
1	V_{SS}	—	Power supply pin (GND)
2	V_{CC}	—	Power supply pin
3	C	—	Capacitor connection pin
4	RSTX/PF2	A	General-purpose I/O port This pin is also used as a reset pin. This pin is a dedicated reset pin in MB95F214H/F213H/F212H.
5	P04/INT04/AN04/HCLK1 /EC0	E	General-purpose I/O port This pin is also used as the external interrupt input. This pin is also used as the A/D converter analog input. This pin is also used as the external clock input. This pin is also used as the 8/16-bit composite timer ch. 0 clock input.
6	P05/AN05/TO00/HCLK2	E	General-purpose I/O port High-current port This pin is also used as the A/D converter analog input. This pin is also used as the 8/16-bit composite timer ch. 0 output. This pin is also used as the external clock input.
7	P06/INT06/TO01	G	General-purpose I/O port High-current port This pin is also used as the external interrupt input. This pin is also used as the 8/16-bit composite timer ch. 0 output.
8	P12/EC0/DBG	H	General-purpose I/O port This pin is also used as the DBG input pin. This pin is also used as the 8/16-bit composite timer ch. 0 clock input.

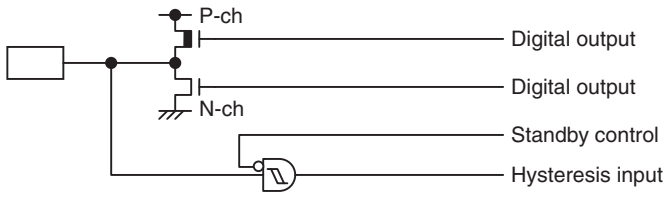
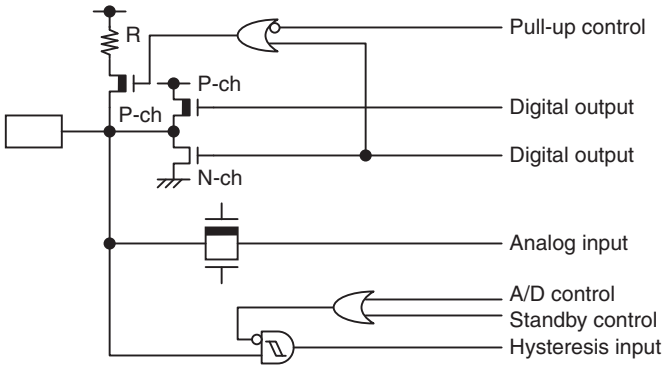
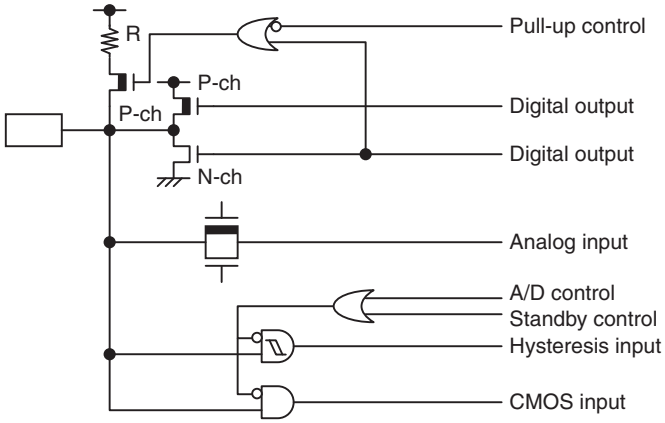
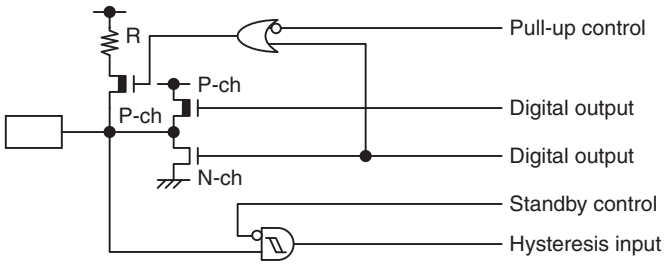
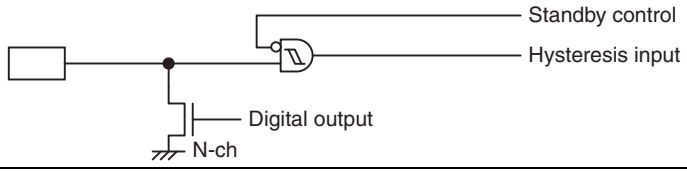
*: For the I/O circuit types, see “8.I/O Circuit Type”.

8. I/O Circuit Type

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • CMOS output • Hysteresis input
C		• Oscillation circuit • Low-speed side Feedback resistance: approx. 10 MΩ • CMOS output • Hysteresis input • Pull-up control available

(Continued)

(Continued)

Type	Circuit	Remarks
D		• CMOS output • Hysteresis input
E		• CMOS output • Hysteresis input • Pull-up control available
F		• CMOS output • Hysteresis input • CMOS input • Pull-up control available
G		• Hysteresis input • CMOS output • Pull-up control available
H		• N-ch open drain output • Hysteresis input

Address	Register abbreviation	Register name	R/W	Initial value
$004A_H$	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000_B
$004B_H$	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000_B
$004C_H$ to $004F_H$	—	(Disabled)	—	—
0050_H	SCR	LIN-UART serial control register	R/W	00000000_B
0051_H	SMR	LIN-UART serial mode register	R/W	00000000_B
0052_H	SSR	LIN-UART serial status register	R/W	00001000_B
0053_H	RDR/TDR	LIN-UART receive/transmit data register	R/W	00000000_B
0054_H	ESCR	LIN-UART extended status control register	R/W	00000100_B
0055_H	ECCR	LIN-UART extended communication control register	R/W	$000000XX_B$
0056_H to $006B_H$	—	(Disabled)	—	—
$006C_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000_B
$006D_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000_B
$006E_H$	ADDH	8/10-bit A/D converter data register (Upper)	R/W	00000000_B
$006F_H$	ADDL	8/10-bit A/D converter data register (Lower)	R/W	00000000_B
0070_H to 0071_H	—	(Disabled)	—	—
0072_H	FSR	Flash memory status register	R/W	$000X0000_B$
0073_H to 0075_H	—	(Disabled)	—	—
0076_H	WREN	Wild register address compare enable register	R/W	00000000_B
0077_H	WROR	Wild register data test setting register	R/W	00000000_B
0078_H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	ILR2	Interrupt level setting register 2	R/W	11111111_B
$007C_H$	ILR3	Interrupt level setting register 3	R/W	11111111_B
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—
$0F80_H$	WRARH0	Wild register address setting register (Upper) ch. 0	R/W	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$004A_H$	EIC20	External interrupt circuit control register ch. 4	R/W	00000000_B
$004B_H$	EIC30	External interrupt circuit control register ch. 6	R/W	00000000_B
$004C_H$ to $004F_H$	—	(Disabled)	—	—
0050_H	—	(Disabled)	—	—
0051_H	—	(Disabled)	—	—
0052_H	—	(Disabled)	—	—
0053_H	—	(Disabled)	—	—
0054_H	—	(Disabled)	—	—
0055_H	—	(Disabled)	—	—
0056_H to $006B_H$	—	(Disabled)	—	—
$006C_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000_B
$006D_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000_B
$006E_H$	ADDH	8/10-bit A/D converter data register (Upper)	R/W	00000000_B
$006F_H$	ADDL	8/10-bit A/D converter data register (Lower)	R/W	00000000_B
0070_H to 0071_H	—	(Disabled)	—	—
0072_H	FSR	Flash memory status register	R/W	$000X0000_B$
0073_H to 0075_H	—	(Disabled)	—	—
0076_H	WREN	Wild register address compare enable register	R/W	00000000_B
0077_H	WROR	Wild register data test setting register	R/W	00000000_B
0078_H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	—	(Disabled)	—	—
$007C_H$	—	(Disabled)	—	—
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—
$0F80_H$	WRARH0	Wild register address setting register (Upper) ch. 0	R/W	00000000_B
$0F81_H$	WRARL0	Wild register address setting register (Lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0F83_H$	WRARH1	Wild register address setting register (Upper) ch. 1	R/W	00000000_B
$0F84_H$	WRARL1	Wild register address setting register (Lower) ch. 1	R/W	00000000_B
$0F85_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000_B
$0F86_H$	WRARH2	Wild register address setting register (Upper) ch. 2	R/W	00000000_B
$0F87_H$	WRARL2	Wild register address setting register (Lower) ch. 2	R/W	00000000_B
$0F88_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000_B
$0F89_H$ to $0F91_H$	—	(Disabled)	—	—
$0F92_H$	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000_B
$0F93_H$	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000_B
$0F94_H$	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000_B
$0F95_H$	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000_B
$0F96_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000_B
$0F97_H$	—	(Disabled)	—	—
$0F98_H$	—	(Disabled)	—	—
$0F99_H$	—	(Disabled)	—	—
$0F9A_H$	—	(Disabled)	—	—
$0F9B_H$	—	(Disabled)	—	—
$0F9C_H$ to $0FBB_H$	—	(Disabled)	—	—
$0FBC_H$	—	(Disabled)	—	—
$0FBD_H$	—	(Disabled)	—	—
$0FBE_H$ to $0FC2_H$	—	(Disabled)	—	—
$0FC3_H$	AIDRL	A/D input disable register (Lower)	R/W	00000000_B
$0FC4_H$ to $0FE3_H$	—	(Disabled)	—	—
$0FE4_H$	CRTH	Main CR clock trimming register (Upper)	R/W	$1XXXXXXX_B$
$0FE5_H$	CRTL	Main CR clock trimming register (Lower)	R/W	$000XXXXX_B$
$0FE6_H$ to $0FE7_H$	—	(Disabled)	—	—
$0FE8_H$	SYSC	System configuration register	R/W	11000011_B

(Continued)

18. Electrical Characteristics

18.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS}−0.3	V_{SS}+6	V	
Input voltage*1	V_{I1}	V_{SS}−0.3	V_{CC}+0.3	V	Other than PF2*2
	V_{I2}	V_{SS}−0.3	10.5	V	PF2
Output voltage*1	V_O	V_{SS}−0.3	V_{SS}+6	V	*2
Maximum clamp current	I_{CLAMP}	-2	+2	mA	Applicable to pins listed in *3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to pins listed in *3
“L” level maximum output current	I_{OL1}	—	15	mA	Other than P05, P06, P62 and P63*4
	I_{OL2}		15		P05, P06, P62 and P63*4
“L” level average current	I_{OLAV1}	—	4	mA	Other than P05, P06, P62 and P63*4 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P05, P06, P62 and P63*4 Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	I_{OH1}	—	-15	mA	Other than P05, P06, P62 and P63*4
	I_{OH2}		-15		P05, P06, P62 and P63*4
“H” level average current	I_{OHAV1}	—	-4	mA	Other than P05, P06, P62 and P63*4 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		-8		P05, P06, P62 and P63*4 Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	-100	mA	
“H” level total average output current	ΣI_{OHAV}	—	-50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	-40	+85	°C	
Storage temperature	Tstg	-55	+150	°C	

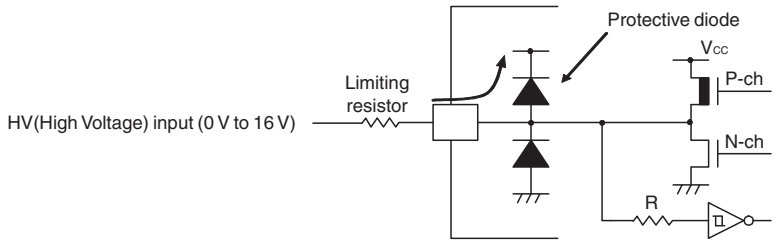
*1: The parameter is based on V_{SS} = 0.0 V.

*2: V_I and V_O must not exceed V_{CC}+0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

*3: Applicable to the following pins: P00 to P07, P62 to P64, PG1, PG2, PF0, PF1 (P00 to P03, P07, P62 to P64, PG1, PG2, PF0 and PF1 are available in MB95F204H/F203H/F202H/F204K/F203K/F202K.)

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current of stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit:

Input/Output Equivalent Circuit



*4: P62 and P63 are available in MB95F204H/F203H/F202H/F204K/F203K/F202K.

WARNING: A semiconductor device may be damaged by applying stress (voltage, current, temperature, etc.) in excess of the absolute maximum rating. Therefore, ensure that not a single parameter exceeds its absolute maximum rating.

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	
Power supply current*4	I_{CC}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	13	17	mA	Flash memory product (except writing and erasing)
				—	33.5	39.5	mA	Flash memory product (at writing and erasing)
				—	15	21	mA	At A/D conversion
	I_{CCS}		V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	5.5	9	mA	
	I_{CCL}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = +25 °C	—	65	153	µA	
	I_{CCLS}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = +25 °C	—	10	84	µA	
	I_{CCT}		V_{CC} = 5.5 V F_{CL} = 32 kHz Watch mode Main stop mode T_A = +25°C	—	5	30	µA	

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*4	I_{CCMCR}	V_{CC}	V_{CC} = 5.5 V F_{CRH} = 10 MHz F_{MP} = 10 MHz Main CR clock mode	—	8.6	—	mA	
	I_{CCSCR}		V_{CC} = 5.5 V Sub-CR clock mode (divided by 2) T_A = +25 °C	—	110	410	µA	
	I_{CCTS}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz Timebase timer mode T_A = +25 °C	—	1.1	3	mA	
	I_{CCH}		V_{CC} = 5.5 V Substop mode T_A = +25 °C	—	3.5	22.5	µA	Main stop mode for single clock selection
	I_{LVD}	V_{CC}	Current consumption for low-voltage detection circuit only	—	37	54	µA	
	I_{CRH}		Current consumption for the internal main CR oscillator	—	0.5	0.6	mA	
	I_{CRL}		Current consumption for the internal sub-CR oscillator oscillating at 100 kHz	—	20	72	µA	

*1: The input level of P04 can be switched between “CMOS input level” and “hysteresis input level”. The input level selection register (ILSR) is used to switch between the two input levels.

*2: P62 and P63 are available in MB95F204H/F203H/F202H/F204K/F203K/F202K.

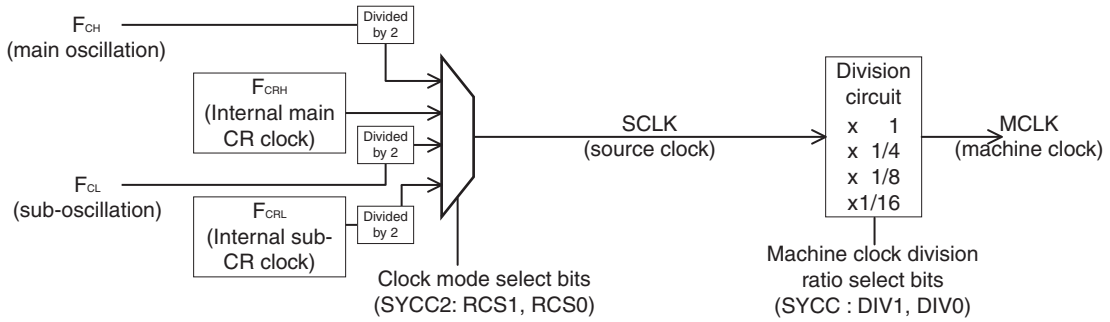
*3: P00 to P03, P07, PG1 and PG2 are available in MB95F204H/F203H/F202H/F204K/F203K/F202K.

*4: The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to a specified value. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH}, I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.

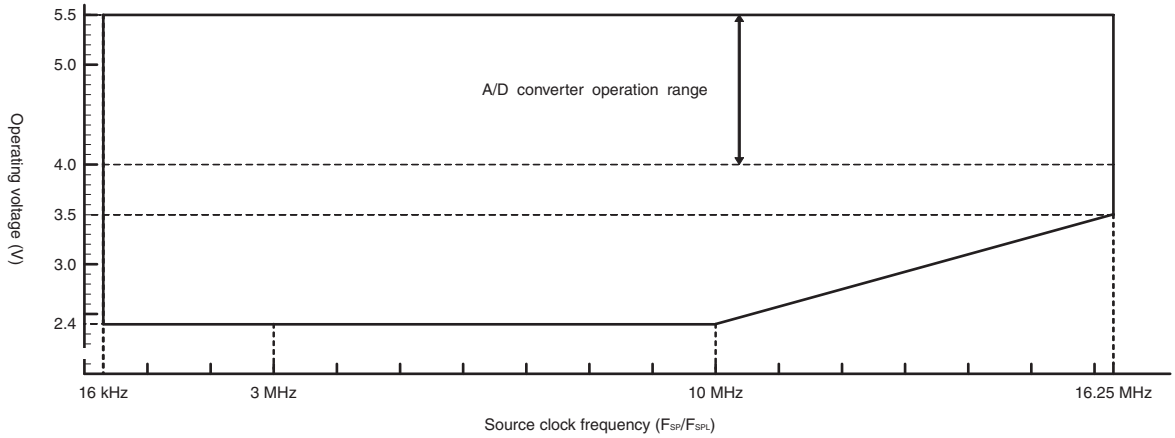
- See “18.4. AC Characteristics: 18.4.1.Clock Timing” for F_{CH} and F_{CL}.
- See “18.4. AC Characteristics: 18.4.2. Source Clock/Machine Clock” for F_{MP} and F_{MPL}.

*5 : PF2 act as high voltage supply for the flash memory during program and erase. It can tolerate high voltage input. For details, see section “18.6. Flash Memory Program/Erase Characteristics”.

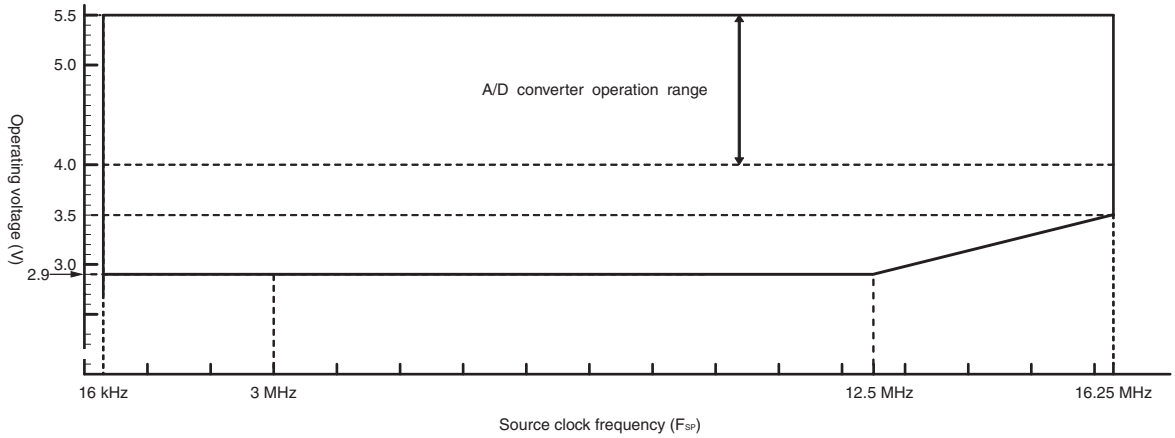
- Schematic diagram of the clock generation block



- Operating voltage - Operating frequency (When T_A = -40 °C to +85 °C)
  - ➢ MB95200H/210H (without the on-chip debug function)



- Operating voltage - Operating frequency (When T_A = +5 °C to +35 °C)
  - ➢ MB95200H/210H (with the on-chip debug function)



18.4.6 LIN-UART Timing (Available in MB95F204H/F203H/F202H/F204K/F203K/F202K only)

Sampling is executed at the rising edge of the sampling clock[1]*, and serial clock delay is disabled*[2]*.(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)*

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF+1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCK, SOT		-95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3+190	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin: C_L = 80 pF+1 TTL	3 t_{MCLK}*3–t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3+95	—	ns
SCK ↓→ SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3+95	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK, SIN		190	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3+95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.

*Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is enabled*2.(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 1)*

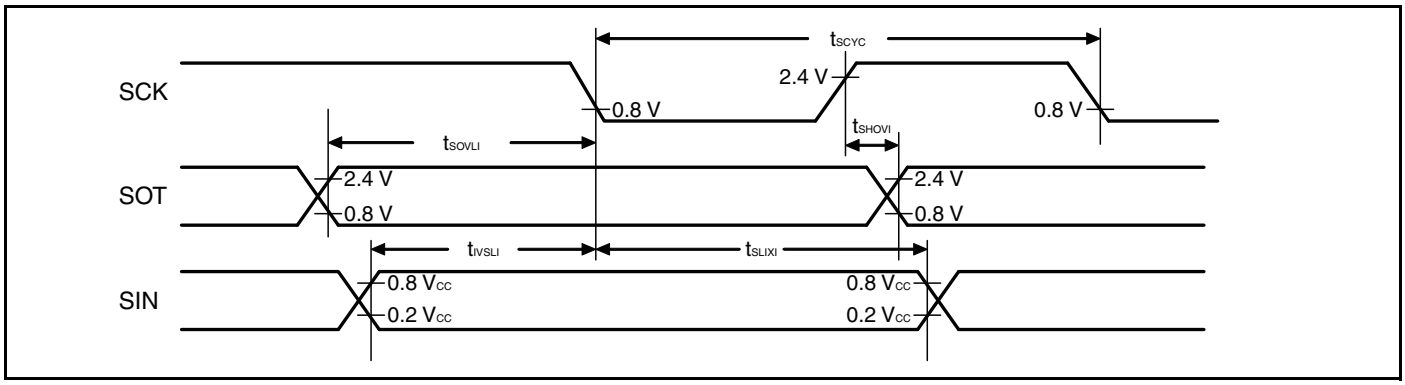
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF+1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑→ SOT delay time	t_{SHOVI}	SCK, SOT		-95	+95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3+190	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.

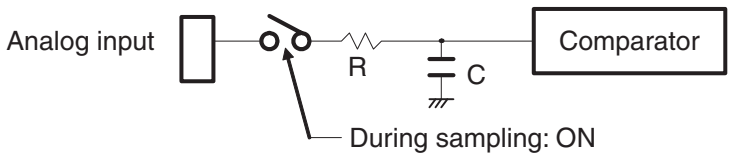


18.5.2 Notes on Using the A/D Converter

External impedance of analog input and its sampling time

- The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

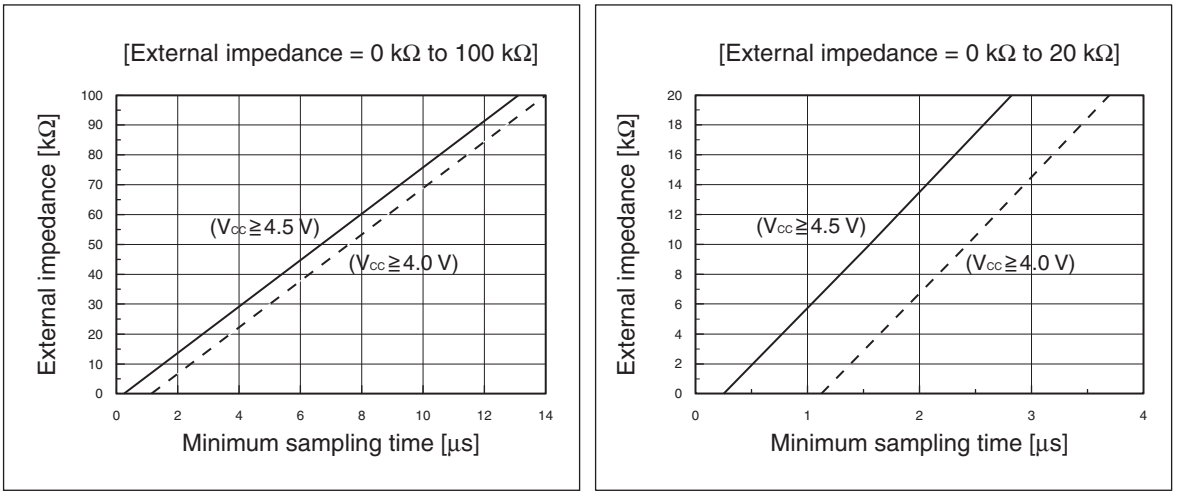
Analog input equivalent circuit



$4.5\ V \le V_{CC} \le 5.5\ V$: R ≈ 1.95 kΩ (Max), C ≈ 17 pF (Max)
$4.0\ V \le V_{CC} < 4.5\ V$: R ≈ 8.98 kΩ (Max), C ≈ 17 pF (Max)

Note: The values are reference values.

Relationship between external impedance and minimum sampling time

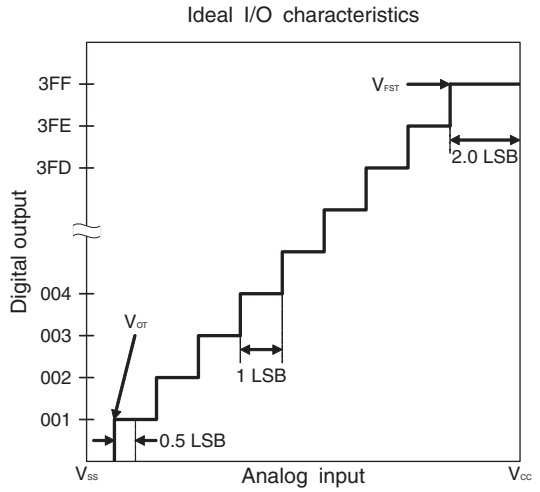


A/D conversion error

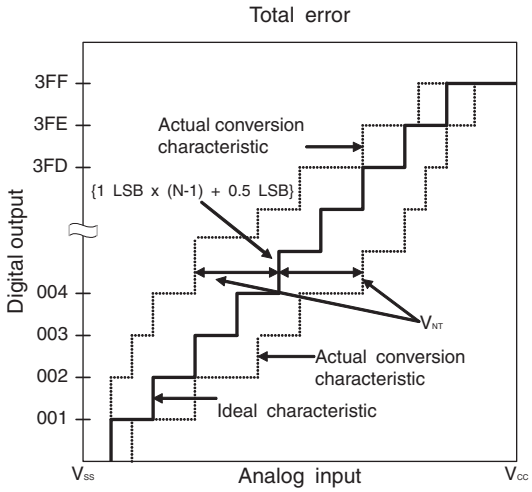
As $|V_{CC}-V_{SS}|$ decreases, the A/D conversion error increases proportionately.

18.5.3 Definitions of A/D Converter Terms

- Resolution
  It indicates the level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.
- Linearity error (unit: LSB)
  It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point ("00 0000 0000" ← → "00 0000 0001") of a device to the full-scale transition point ("11 1111 1111" ← → "11 1111 1110") of the same device.
- Differential linear error (unit: LSB)
  It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
  It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.



$$1\ LSB = \frac{V_{CC} - V_{SS}}{1024}\ (V)$$



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB \times (N - 1) + 0.5\ LSB\}}{1\ LSB}\ [LSB]$$

N : A/D converter digital output value

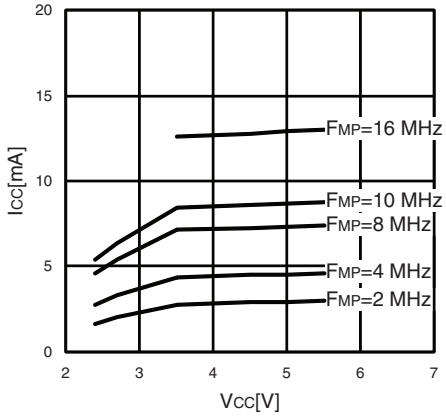
V_{NT}: Voltage at which the digital output transits from (N - 1) to N

(Continued)

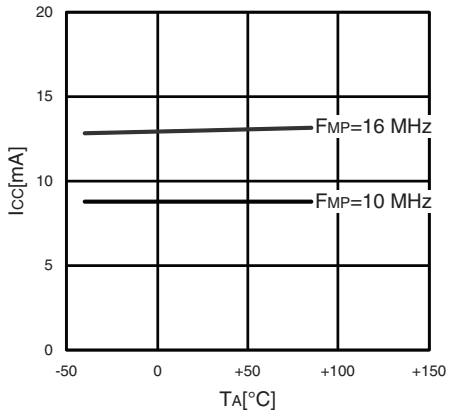
19. Sample Electrical Characteristics

Power supply current•temperature

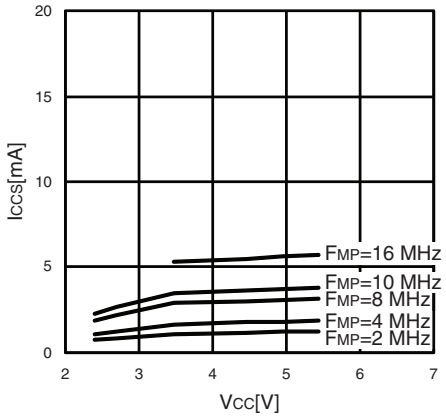
ICC - VCC
TA=+25°C, FMP=2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



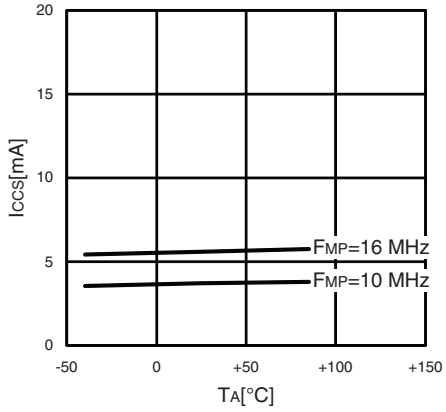
ICC - TA
VCC=5.5 V, FMP=10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



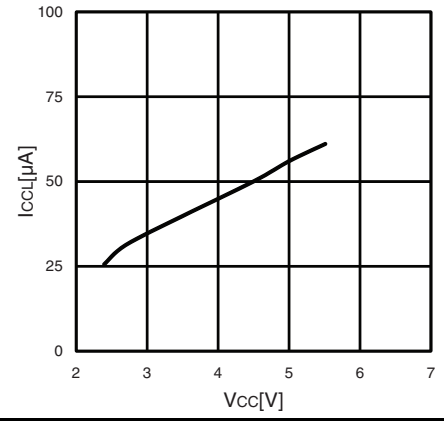
ICCS - VCC
TA=+25°C, FMP=2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



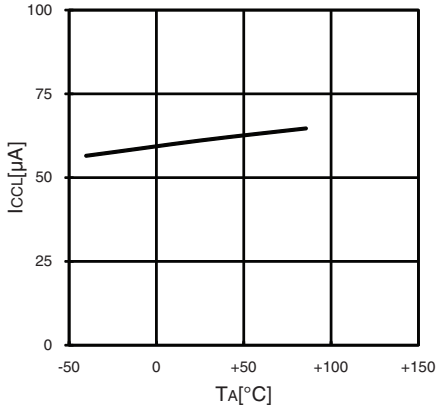
ICCS - TA
VCC=5.5 V, FMP=10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



ICCL - VCC
TA=+25°C, FMPL=16 kHz (divided by 2)
Subclock mode with the external clock operating



ICCL - TA
VCC=5.5 V, FMPL=16 kHz (divided by 2)
Subclock mode with the external clock operating



(Continued)

20. Mask Options

No.	Part Number	MB95F204H MB95F203H MB95F202H MB95F214H MB95F213H MB95F212H	MB95F204K MB95F203K MB95F202K MB95F214K MB95F213K MB95F212K
	Selection Method	**Setting disabled**	**Setting disabled**
1	Low-voltage detection reset •With low-voltage detection reset •Without low-voltage detection reset	Without low-voltage detection reset	With low-voltage detection reset
2	Reset •With dedicated reset input •Without dedicated reset input	With dedicated reset input	Without dedicated reset input

21. Ordering Information

Part Number	Package
MB95F204HP-G-SH-SNE2 MB95F204KP-G-SH-SNE2 MB95F203HP-G-SH-SNE2 MB95F203KP-G-SH-SNE2 MB95F202HP-G-SH-SNE2 MB95F202KP-G-SH-SNE2	24-pin plastic SDIP (DIP-24P-M07)
MB95F204HPF-G-SNE2 MB95F204KPF-G-SNE2 MB95F203HPF-G-SNE2 MB95F203KPF-G-SNE2 MB95F202HPF-G-SNE2 MB95F202KPF-G-SNE2	20-pin plastic SOP (FPT-20P-M09)
MB95F214HPH-G-SNE2 MB95F214KPH-G-SNE2 MB95F213HPH-G-SNE2 MB95F213KPH-G-SNE2 MB95F212HPH-G-SNE2 MB95F212KPH-G-SNE2	8-pin plastic DIP (DIP-8P-M03)
MB95F214HPF-G-SNE2 MB95F214KPF-G-SNE2 MB95F213HPF-G-SNE2 MB95F213KPF-G-SNE2 MB95F212HPF-G-SNE2 MB95F212KPF-G-SNE2	8-pin plastic SOP (FPT-8P-M08)

23. Major Changes

Spansion Publication Number: DS07-12623-5E

Page	Section	Change results
30	Electrical Characteristics 1. Absolute Maximum Ratings	Changed the characteristics of Input voltage.
33	3. DC Characteristics	Corrected the maximum value of “H” level input voltage for PF2 pin. $V_{CC} + 0.3 \rightarrow 10.5$
		Corrected the maximum value of Open-drain output application voltage. 0.2Vcc → Vss + 5.5
36		Added the footnote *5.
39	4. AC Characteristics (1) Clock Timing	Added a figure of HCLK1/HCLK2.
42	(2) Source Clock/Machine Clock	Corrected the graph of Operating voltage - Operating frequency (with the on-chip debug function). (Corrected the pitch)
43	(3) External Reset	Added “and power on” to the remarks column.
58	6. Flash Memory Program/Erase Characteristics	Added the row of “Current drawn on PF2”.
		Corrected the minimum value of Power supply voltage at erase/program. 4.5 → 3.0

Note: Please see “Document History” about later revised information.

Document History

Document Title: MB95200H/210H Series F^{2}MC-8FX 8-bit Microcontroller **Document Number: 002-07463**				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	AKIH	07/16/2010	Migrated to Cypress and assigned document number 002-07463. No change to document contents or format.
*A	5177811	AKIH	03/18/2016	Updated to Cypress format.

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