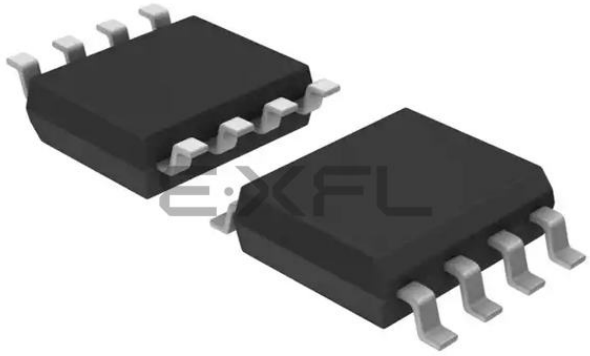

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	5
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	240 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 2x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f212kpf-g-sne2

1. Product Line-up

Parameter \ Part number	MB95 F204H	MB95 F203H	MB95 F202H	MB95 F204K	MB95 F203K	MB95 F202K	MB95 F214H	MB95 F213H	MB95 F212H	MB95 F214K	MB95 F213K	MB95 F212K
Type	Flash memory product											
Clock supervisor counter	It supervises the main clock oscillation.											
ROM capacity	16 KB	8 KB	4 KB	16 KB	8 KB	4 KB	16 KB	8 KB	4 KB	16 KB	8 KB	4 KB
RAM capacity	496 B	496 B	240 B	496 B	496 B	240 B	496 B	496 B	240 B	496 B	496 B	240 B
Low-voltage detection reset	No			Yes			No			Yes		
Reset input	Dedicated			Software select			Dedicated			Software select		
CPU functions	Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 61.5 ns (with machine clock = 16.25 MHz) Interrupt processing time : 0.6 µs (with machine clock = 16.25 MHz)											
General-purpose I/O	I/O ports (Max): 16 CMOS: 15, N-ch: 1			I/O ports (Max): 17 CMOS: 15, N-ch: 2			I/O ports (Max): 4 CMOS: 3, N-ch: 1			I/O ports (Max): 5 CMOS: 3, N-ch: 2		
Timebase timer	Interrupt cycle : 0.256 ms - 8.3 s (when external clock = 4 MHz)											
Hardware/software watchdog timer	Reset generation cycle Main oscillation clock at 10 MHz : 105 ms (Min) The sub-CR clock can be used as the source clock of the hardware watchdog.											
Wild register	It can be used to replace three bytes of data.											
LIN-UART	A wide range of communication speed can be selected by a dedicated reload timer. It has a full duplex double buffer. Clock-synchronized serial data transfer and clock-asynchronized serial data transfer is enabled. The LIN function can be used as a LIN master or a LIN slave.						No LIN-UART					
8/10-bit A/D converter	6 ch.						2 ch.					
	8-bit or 10-bit resolution can be selected.											
8/16-bit composite timer	2 ch.						1 ch.					
	The timer can be configured as an "8-bit timer x 2 channels" or a "16-bit timer x 1 channel". It has built-in timer function, PWC function, PWM function and input capture function. Count clock: it can be selected from internal clocks (seven types) and external clocks. It can output square wave.											
External interrupt	6 ch.						2 ch.					
	Interrupt by edge detection (rising edge, falling edge, or both edges can be selected.) It can be used to wake up the device from standby modes.											
On-chip debug	1-wire serial control It supports serial writing. (asynchronous mode)											

(Continued)

(Continued)

Part number / Parameter	MB95 F204H	MB95 F203H	MB95 F202H	MB95 F204K	MB95 F203K	MB95 F202K	MB95 F214H	MB95 F213H	MB95 F212H	MB95 F214K	MB95 F213K	MB95 F212K
Watch prescaler	Eight different time intervals can be selected.											
Flash memory	It supports automatic programming, Embedded Algorithm, write/erase/erase-suspend/erase-resume commands. It has a flag indicating the completion of the operation of Embedded Algorithm. Number of write/erase cycles: 100000 Data retention time: 20 years For write/erase, external Vpp(+10 V) input is required. Flash Security Feature for protecting the contents of the flash											
Standby mode	Sleep mode, stop mode, watch mode, timebase timer mode											
Package	SDIP-24 SOP-20						DIP-8 SOP-8					

2. Packages and Corresponding Products

Part number / Package	MB95 F204H	MB95 F203H	MB95 F202H	MB95 F204K	MB95 F203K	MB95 F202K	MB95 F214H	MB95 F213H	MB95 F212H	MB95 F214K	MB95 F213K	MB95 F212K
24-pin plastic SDIP	O	O	O	O	O	O	X	X	X	X	X	X
20-pin plastic SOP	O	O	O	O	O	O	X	X	X	X	X	X
8-pin plastic DIP	X	X	X	X	X	X	O	O	O	O	O	O
8-pin plastic SOP	X	X	X	X	X	X	O	O	O	O	O	O

O: Available

X: Unavailable

3. Differences Among Products And Notes On Product Selection

Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/program.

For details of current consumption, see “18.Electrical Characteristics”.

Package

For details of information on each package, see “2.Packages and Corresponding Products” and “22.Package Dimensions”.

Operating voltage

The operating voltage varies, depending on whether the on-chip debug function is used or not.

For details of the operating voltage, see “18.Electrical Characteristics”.

On-chip debug function

The on-chip debug function requires that V_{CC}, V_{SS} and 1 serial-wire be connected to an evaluation tool. In addition, if the flash memory data has to be updated, the RSTX/PF2 pin must also be connected to the same evaluation tool.

6. Pin Description (MB95200H Series 20 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF0/X0	B	General-purpose I/O port This pin is also used as the main clock input oscillation pin.
2	PF1/X1	B	General-purpose I/O port This pin is also used as the main clock input/output oscillation pin.
3	V_{SS}	—	Power supply pin (GND)
4	PG2/X1A	C	General-purpose I/O port This pin is also used as the subclock input/output oscillation pin.
5	PG1/X0A	C	General-purpose I/O port This pin is also used as the subclock input oscillation pin.
6	V_{CC}	—	Power supply pin
7	C	—	Capacitor connection pin
8	PF2/RSTX	A	General-purpose I/O port This pin is also used as a reset pin. This pin is a dedicated reset pin in MB95F204H/F203H/F202H.
9	P62/TO10	D	General-purpose I/O port High-current port This pin is also used as the 8/16-bit composite timer ch. 1 output.
10	P63/TO11	D	General-purpose I/O port High-current port This pin is also used as the 8/16-bit composite timer ch. 1 output.
11	P64/EC1	D	General-purpose I/O port This pin is also used as the 8/16-bit composite timer ch. 1 clock input.
12	P00/AN00	E	General-purpose I/O port This pin is also used as the A/D converter analog input.
13	P01/AN01	E	General-purpose I/O port This pin is also used as the A/D converter analog input.
14	P02/INT02/AN02/SCK	E	General-purpose I/O port This pin is also used as the external interrupt input. This pin is also used as the A/D converter analog input. This pin is also used as the LIN-UART clock I/O.
15	P03/INT03/AN03/SOT	E	General-purpose I/O port This pin is also used as the external interrupt input. This pin is also used as the A/D converter analog input. This pin is also used as the LIN-UART data output.
16	P04/INT04/AN04/SIN /HCLK1/EC0	F	General-purpose I/O port This pin is also used as the external interrupt input. This pin is also used as the A/D converter analog input. This pin is also used as the LIN-UART data input. This pin is also used as the external clock input. This pin is also used as the 8/16-bit composite timer ch. 0 clock input.

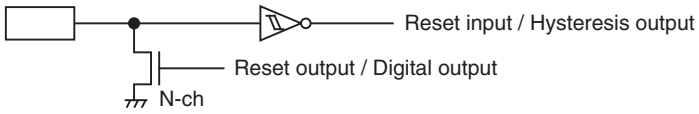
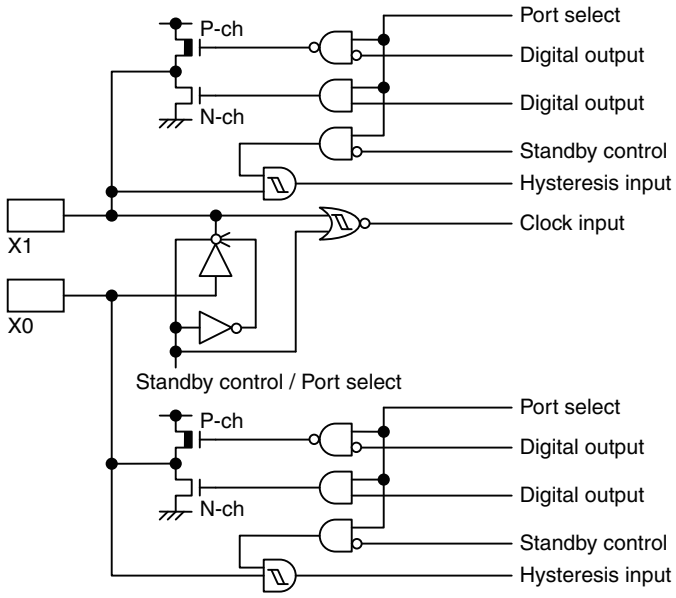
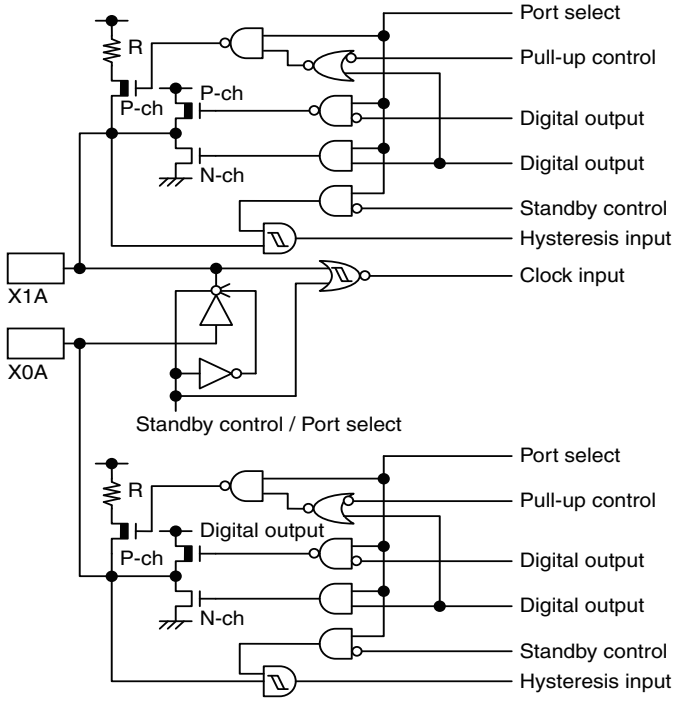
(Continued)

7. Pin Description (MB95210H Series)

Pin no.	Pin name	I/O circuit type*	Function
1	V_{SS}	—	Power supply pin (GND)
2	V_{CC}	—	Power supply pin
3	C	—	Capacitor connection pin
4	RSTX/PF2	A	General-purpose I/O port This pin is also used as a reset pin. This pin is a dedicated reset pin in MB95F214H/F213H/F212H.
5	P04/INT04/AN04/HCLK1 /EC0	E	General-purpose I/O port This pin is also used as the external interrupt input. This pin is also used as the A/D converter analog input. This pin is also used as the external clock input. This pin is also used as the 8/16-bit composite timer ch. 0 clock input.
6	P05/AN05/TO00/HCLK2	E	General-purpose I/O port High-current port This pin is also used as the A/D converter analog input. This pin is also used as the 8/16-bit composite timer ch. 0 output. This pin is also used as the external clock input.
7	P06/INT06/TO01	G	General-purpose I/O port High-current port This pin is also used as the external interrupt input. This pin is also used as the 8/16-bit composite timer ch. 0 output.
8	P12/EC0/DBG	H	General-purpose I/O port This pin is also used as the DBG input pin. This pin is also used as the 8/16-bit composite timer ch. 0 clock input.

*: For the I/O circuit types, see “8.I/O Circuit Type”.

8. I/O Circuit Type

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • CMOS output • Hysteresis input
C		• Oscillation circuit • Low-speed side Feedback resistance: approx. 10 MΩ • CMOS output • Hysteresis input • Pull-up control available

(Continued)

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Address	Register abbreviation	Register name	R/W	Initial value
$0FE6_H$ to $0FE7_H$	—	(Disabled)	—	—
$0FE8_H$	SYSC	System configuration register	R/W	11000011_B
$0FE9_H$	CMCR	Clock monitoring control register	R/W	$XX000000_B$
$0FEA_H$	CMDR	Clock monitoring data register	R/W	00000000_B
$0FEB_H$	WDTH	Watchdog timer selection ID register (Upper)	R/W	$XXXXXXXX_B$
$0FEC_H$	WDTL	Watchdog timer selection ID register (Lower)	R/W	$XXXXXXXX_B$
$0FED_H$	—	(Disabled)	—	—
$0FEE_H$	ILSR	Input level select register	R/W	00000000_B
$0FEF_H$ to $0FFF_H$	—	(Disabled)	—	—

R/W access symbols

R/W : Readable / Writable
R : Read only
W : Write only

Initial value symbols

0 : The initial value of this bit is “0”.
1 : The initial value of this bit is “1”.
X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an undefined value is returned.

18. Electrical Characteristics

18.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS}−0.3	V_{SS}+6	V	
Input voltage*1	V_{I1}	V_{SS}−0.3	V_{CC}+0.3	V	Other than PF2*2
	V_{I2}	V_{SS}−0.3	10.5	V	PF2
Output voltage*1	V_O	V_{SS}−0.3	V_{SS}+6	V	*2
Maximum clamp current	I_{CLAMP}	-2	+2	mA	Applicable to pins listed in *3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to pins listed in *3
“L” level maximum output current	I_{OL1}	—	15	mA	Other than P05, P06, P62 and P63*4
	I_{OL2}		15		P05, P06, P62 and P63*4
“L” level average current	I_{OLAV1}	—	4	mA	Other than P05, P06, P62 and P63*4 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P05, P06, P62 and P63*4 Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	I_{OH1}	—	-15	mA	Other than P05, P06, P62 and P63*4
	I_{OH2}		-15		P05, P06, P62 and P63*4
“H” level average current	I_{OHAV1}	—	-4	mA	Other than P05, P06, P62 and P63*4 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		-8		P05, P06, P62 and P63*4 Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	-100	mA	
“H” level total average output current	ΣI_{OHAV}	—	-50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	-40	+85	°C	
Storage temperature	Tstg	-55	+150	°C	

18.2 Recommended Operating Conditions

(V_{SS} = 0.0 V)

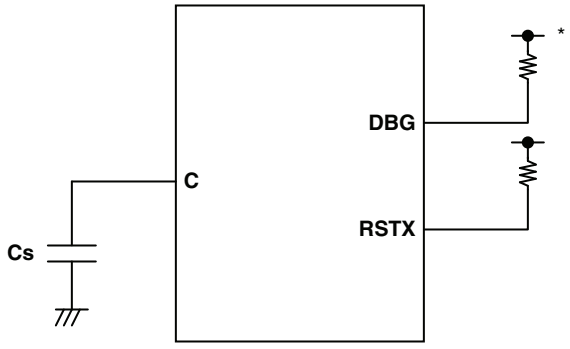
Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V_{CC}	2.4*1*2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Smoothing capacitor	C_S	0.022	1	µF	*3	
Operating temperature	T_A	-40	+85	°C	Other than on-chip debug function	
		+5	+35		On-chip debug function	

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The value is 2.88 V when the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

- **DBG / RSTX / C pin connection diagram**



*: Since the DBG pin becomes a communication pin in on-chip debug mode, set a pull-up resistor value suiting the input/output specifications of P12/DBG.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the electrical characteristics of the device are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact sales representatives beforehand.

18.3 DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI}	P04	*1	0.7 V_{CC}	—	V_{CC}+0.3	V	When CMOS input level (hysteresis input) is selected
	V_{IHS}	P00 to P07, P12, P62 to P64, PF0 to PF1, PG1 to PG2	*1	0.8 V_{CC}	—	V_{CC}+0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.7 V_{CC}	—	10.5	V	Hysteresis input*5
"L" level input voltage	V_{IL}	P04	*1	V_{SS}–0.3	—	0.3 V_{CC}	V	When CMOS input level (hysteresis input) is selected
	V_{ILS}	P00 to P07, P12, P62 to P64, PF0 to PF1, PG1 to PG2	*1	V_{SS}–0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS}–0.3	—	0.3 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	PF2, P12	—	V_{SS}–0.3	—	V_{SS}+5.5	V	
"H" level output voltage	V_{OH1}	Output pins other than P05, P06, P62, P63, PF2 and P12*2	I_{OH} = -4 mA	V_{CC}–0.5	—	—	V	
	V_{OH2}	P05, P06, P62, P63*2	I_{OH} = -8 mA	V_{CC}–0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P05, P06, P62 and P63*2	I_{OL} = 4 mA	—	—	0.4	V	
	V_{OL2}	P05, P06, P62, P63*2	I_{OL} = 2 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	-5	—	+5	µA	When pull-up resistance is disabled
Pull-up resistance	R_{PULL}	P00 to P07, PG1, PG2*3	V_I = 0 V	25	50	100	kΩ	When pull-up resistance is enabled

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	
Power supply current*4	I_{CC}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	13	17	mA	Flash memory product (except writing and erasing)
				—	33.5	39.5	mA	Flash memory product (at writing and erasing)
				—	15	21	mA	At A/D conversion
	I_{CCS}		V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	5.5	9	mA	
	I_{CCL}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = +25 °C	—	65	153	µA	
	I_{CCLS}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = +25 °C	—	10	84	µA	
	I_{CCT}		V_{CC} = 5.5 V F_{CL} = 32 kHz Watch mode Main stop mode T_A = +25°C	—	5	30	µA	

(Continued)

(Continued)

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input clock rise time and fall time	t_{CR} t_{CF}	X0	X1 open	—	—	5	ns	When the external clock is used
		X0, X1	*	—	—	5	ns	
		HCLK1, HCLK2	—					
CR oscillation start time	t_{CRHWK}	—	—	—	—	80	µs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	10	µs	When the sub-CR clock is used

* : The external clock signal is input to X0 and the inverted external clock signal to X1.

18.4.2 Source Clock/Machine Clock

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t_{SCLK}	—	61.5	—	2000	ns	When the main external clock is used Min: F_{CH} = 32.5 MHz, divided by 2 Max: F_{CH} = 1 MHz, divided by 2
			100	—	1000	ns	When the main CR clock is used Min: F_{CRH} = 10 MHz Max: F_{CRH} = 1 MHz
			—	61	—	µs	When the sub-CR clock is used F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When the sub-oscillation clock is used F_{CRL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			1	—	10	MHz	When the main CR clock is used
	F_{SPL}		—	16.384	—	kHz	When the sub-oscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2(minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
			100	—	16000	ns	When the main CR clock is used Min: F_{SP} = 10 MHz Max: F_{SP} = 1 MHz, divided by 16
			61	—	976.5	µs	When the sub-oscillation clock is used Min: F_{SPL} = 16.384 kHz, no division Max: F_{SPL} = 16.384 kHz, divided by 16
			20	—	320	µs	When the sub-CR clock is used Min: F_{SPL} = 50 kHz, no division Max: F_{SPL} = 50 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.0625	—	10	MHz	When the main CR clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the sub-oscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio selection bits (SYCC : DIV1 and DIV0) . This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio selection bits (SYCC : DIV1 and DIV0) . In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- Subclock divided by 2
- Sub-CR clock divided by 2

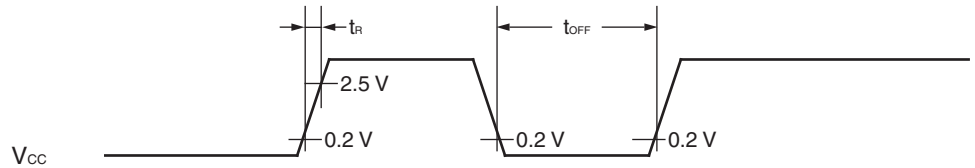
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

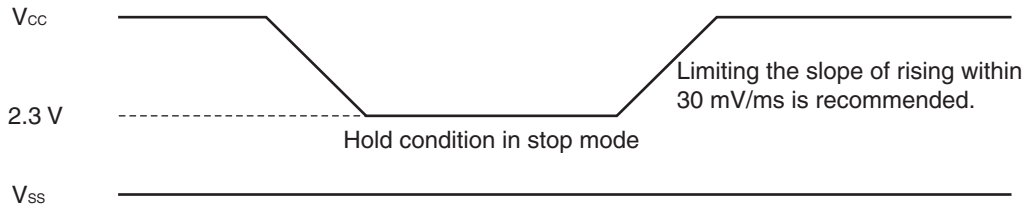
18.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to within 30 mV/ms as shown below.



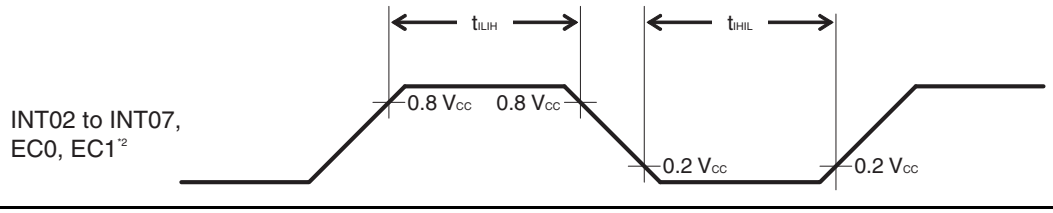
18.4.5 Peripheral Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT02 to INT07, EC0, EC1*2	2 t_{MCLK}*1	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*1	—	ns

*1: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.

*2: INT02, INT03, INT05, INT07 and EC1 are available in MB95F204H/F203H/F202H/F204K/F203K/F202K.



Sampling is executed at the falling edge of the sampling clock[1], and serial clock delay is disabled*[2].(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)*

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

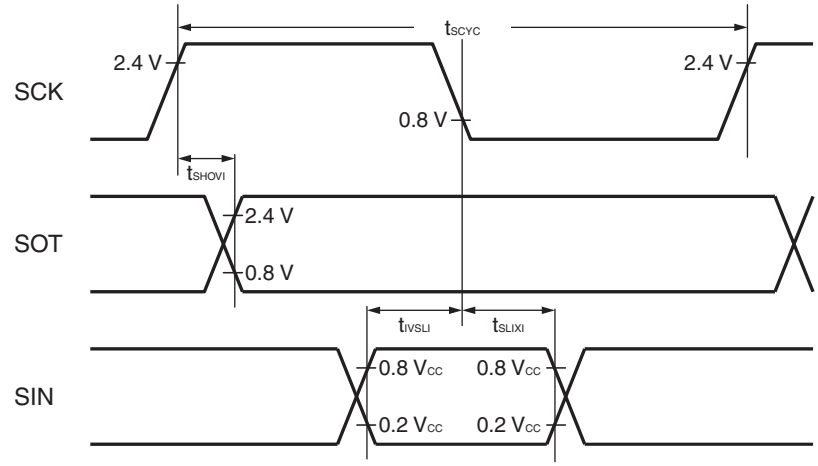
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF+1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑→ SOT delay time	t_{SHOVI}	SCK, SOT		-95	+95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3+190	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin: C_L = 80 pF+1 TTL	3 t_{MCLK}*3–t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3+95	——	ns
SCK ↑→ SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3+95	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK, SIN		190	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3+95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

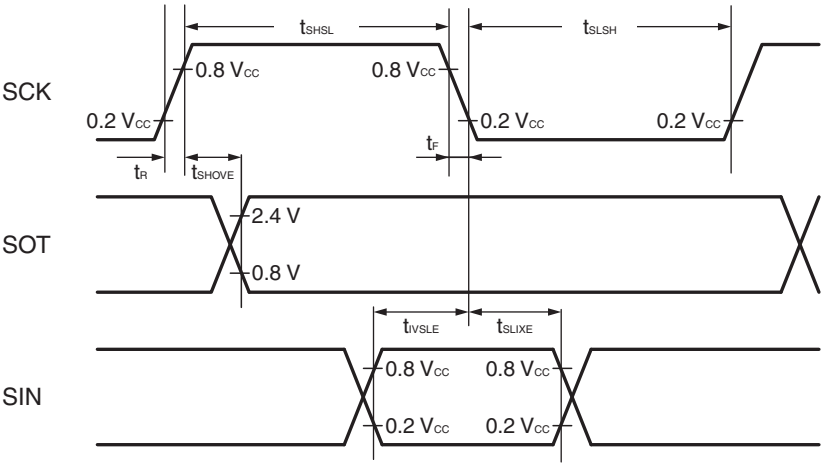
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



*Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2.*
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)

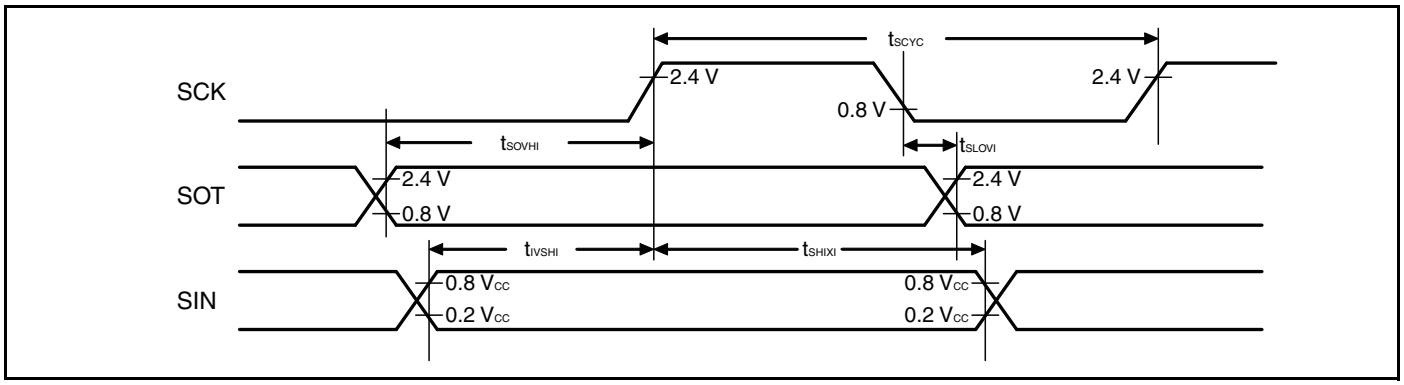
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF+1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCK, SOT		-95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3+190	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “18.4.2.Source Clock/Machine Clock” for t_{MCLK}.



18.4.7 Low-voltage Detection

(V_{SS} = 0.0 V, T_A = -40°C to +85°C)

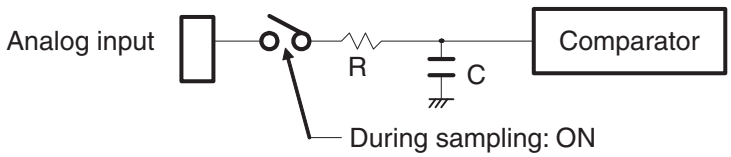
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
Detection voltage	V_{DL-}	2.42	2.6	2.78	V	At power supply fall
Hysteresis width	V_{HYS}	70	100	—	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	1	—	—	µs	Slope of power supply that the reset release signal generates
		—	3000	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	300	—	—	µs	Slope of power supply that the reset detection signal generates
		—	300	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	300	µs	
Reset detection delay time	t_{d2}	—	—	20	µs	

18.5.2 Notes on Using the A/D Converter

External impedance of analog input and its sampling time

- The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

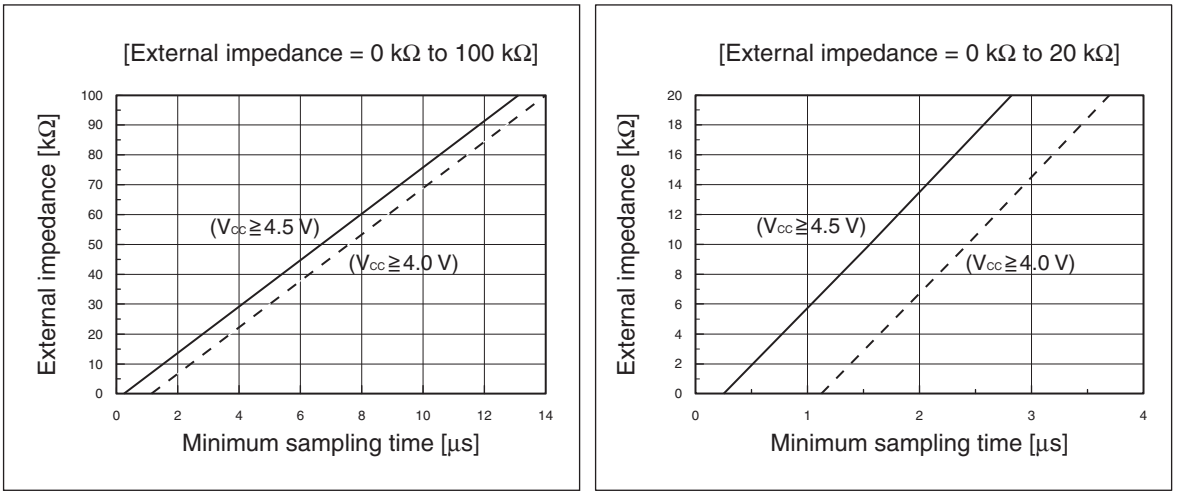
Analog input equivalent circuit



$4.5\ V \le V_{CC} \le 5.5\ V$: R ≈ 1.95 kΩ (Max), C ≈ 17 pF (Max)
$4.0\ V \le V_{CC} < 4.5\ V$: R ≈ 8.98 kΩ (Max), C ≈ 17 pF (Max)

Note: The values are reference values.

Relationship between external impedance and minimum sampling time



A/D conversion error

As $|V_{CC}-V_{SS}|$ decreases, the A/D conversion error increases proportionately.

18.6 Flash Memory Program/Erase Characteristics

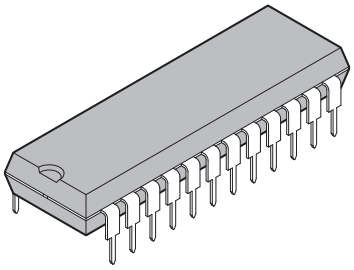
Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Chip erase time	—	1*1	15*2	s	00_H programming time prior to erasure is excluded.
Byte programming time	—	32	3600	µs	System-level overhead is excluded.
Erase/program voltage	9.5	10	10.5	V	The erase/program voltage must be applied to the PF2 pin in erase/program.
Current drawn on PF2	—	—	5.0	mA	Current consumption of PF2 pin during flash memory program/erase
Erase/program cycle	—	100000	—	cycle	
Power supply voltage at erase/program	3.0	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85°C

*1: T_A = +25°C, V_{CC} = 5.0 V, 100000 cycles

*2: T_A = +85°C, V_{CC} = 4.5 V, 100000 cycles

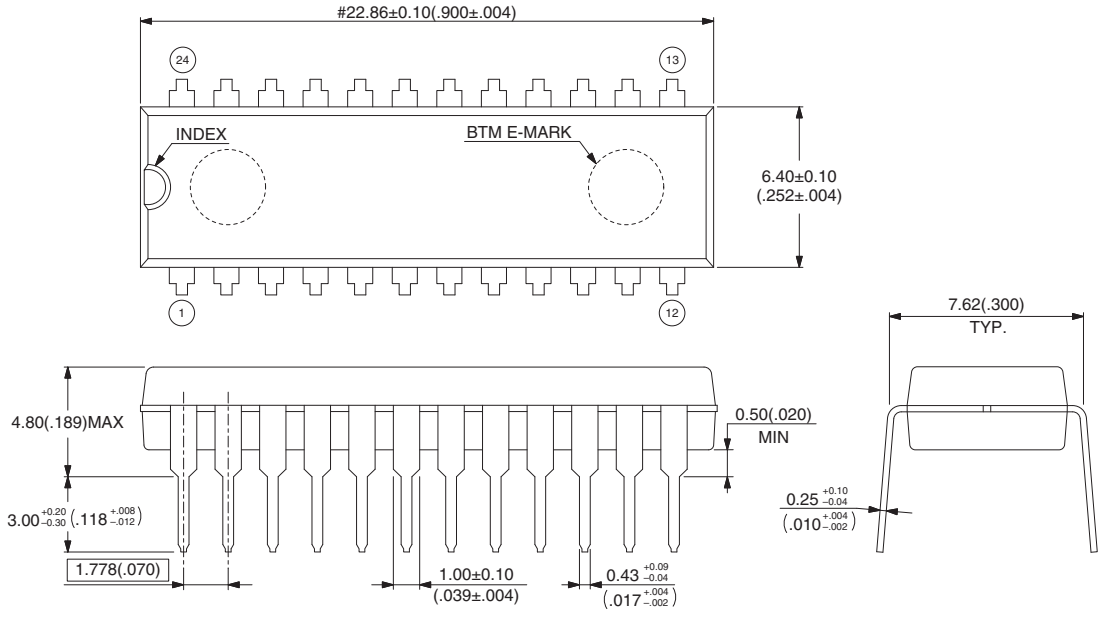
*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test by using the Arrhenius equation with the average temperature being +85°C) .

22. Package Dimensions

24-pin plastic SDIP		
 (DIP-24P-M07)	Lead pitch	1.778 mm
	Package width × package length	6.40 mm × 22.86 mm
	Sealing method	Plastic mold
	Mounting height	4.80 mm Max

24-pin plastic SDIP
(DIP-24P-M07)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)