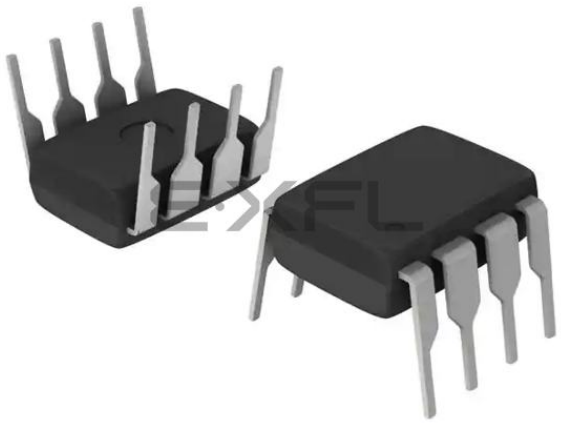

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	5
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	240 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 2x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-DIP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f212kph-g-sne2

1. Product Line-up

Parameter \ Part number	MB95 F204H	MB95 F203H	MB95 F202H	MB95 F204K	MB95 F203K	MB95 F202K	MB95 F214H	MB95 F213H	MB95 F212H	MB95 F214K	MB95 F213K	MB95 F212K
Type	Flash memory product											
Clock supervisor counter	It supervises the main clock oscillation.											
ROM capacity	16 KB	8 KB	4 KB	16 KB	8 KB	4 KB	16 KB	8 KB	4 KB	16 KB	8 KB	4 KB
RAM capacity	496 B	496 B	240 B	496 B	496 B	240 B	496 B	496 B	240 B	496 B	496 B	240 B
Low-voltage detection reset	No			Yes			No			Yes		
Reset input	Dedicated			Software select			Dedicated			Software select		
CPU functions	Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 61.5 ns (with machine clock = 16.25 MHz) Interrupt processing time : 0.6 µs (with machine clock = 16.25 MHz)											
General-purpose I/O	I/O ports (Max): 16 CMOS: 15, N-ch: 1			I/O ports (Max): 17 CMOS: 15, N-ch: 2			I/O ports (Max): 4 CMOS: 3, N-ch: 1			I/O ports (Max): 5 CMOS: 3, N-ch: 2		
Timebase timer	Interrupt cycle : 0.256 ms - 8.3 s (when external clock = 4 MHz)											
Hardware/software watchdog timer	Reset generation cycle Main oscillation clock at 10 MHz : 105 ms (Min) The sub-CR clock can be used as the source clock of the hardware watchdog.											
Wild register	It can be used to replace three bytes of data.											
LIN-UART	A wide range of communication speed can be selected by a dedicated reload timer. It has a full duplex double buffer. Clock-synchronized serial data transfer and clock-asynchronized serial data transfer is enabled. The LIN function can be used as a LIN master or a LIN slave.						No LIN-UART					
8/10-bit A/D converter	6 ch.						2 ch.					
	8-bit or 10-bit resolution can be selected.											
8/16-bit composite timer	2 ch.						1 ch.					
	The timer can be configured as an "8-bit timer x 2 channels" or a "16-bit timer x 1 channel". It has built-in timer function, PWC function, PWM function and input capture function. Count clock: it can be selected from internal clocks (seven types) and external clocks. It can output square wave.											
External interrupt	6 ch.						2 ch.					
	Interrupt by edge detection (rising edge, falling edge, or both edges can be selected.) It can be used to wake up the device from standby modes.											
On-chip debug	1-wire serial control It supports serial writing. (asynchronous mode)											

(Continued)

(Continued)

Part number / Parameter	MB95 F204H	MB95 F203H	MB95 F202H	MB95 F204K	MB95 F203K	MB95 F202K	MB95 F214H	MB95 F213H	MB95 F212H	MB95 F214K	MB95 F213K	MB95 F212K
Watch prescaler	Eight different time intervals can be selected.											
Flash memory	It supports automatic programming, Embedded Algorithm, write/erase/erase-suspend/erase-resume commands. It has a flag indicating the completion of the operation of Embedded Algorithm. Number of write/erase cycles: 100000 Data retention time: 20 years For write/erase, external Vpp(+10 V) input is required. Flash Security Feature for protecting the contents of the flash											
Standby mode	Sleep mode, stop mode, watch mode, timebase timer mode											
Package	SDIP-24 SOP-20						DIP-8 SOP-8					

2. Packages and Corresponding Products

Part number / Package	MB95 F204H	MB95 F203H	MB95 F202H	MB95 F204K	MB95 F203K	MB95 F202K	MB95 F214H	MB95 F213H	MB95 F212H	MB95 F214K	MB95 F213K	MB95 F212K
24-pin plastic SDIP	O	O	O	O	O	O	X	X	X	X	X	X
20-pin plastic SOP	O	O	O	O	O	O	X	X	X	X	X	X
8-pin plastic DIP	X	X	X	X	X	X	O	O	O	O	O	O
8-pin plastic SOP	X	X	X	X	X	X	O	O	O	O	O	O

O: Available

X: Unavailable

3. Differences Among Products And Notes On Product Selection

Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/program.

For details of current consumption, see “18.Electrical Characteristics”.

Package

For details of information on each package, see “2.Packages and Corresponding Products” and “22.Package Dimensions”.

Operating voltage

The operating voltage varies, depending on whether the on-chip debug function is used or not.

For details of the operating voltage, see “18.Electrical Characteristics”.

On-chip debug function

The on-chip debug function requires that V_{CC}, V_{SS} and 1 serial-wire be connected to an evaluation tool. In addition, if the flash memory data has to be updated, the RSTX/PF2 pin must also be connected to the same evaluation tool.

6. Pin Description (MB95200H Series 20 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF0/X0	B	General-purpose I/O port This pin is also used as the main clock input oscillation pin.
2	PF1/X1	B	General-purpose I/O port This pin is also used as the main clock input/output oscillation pin.
3	V_{SS}	—	Power supply pin (GND)
4	PG2/X1A	C	General-purpose I/O port This pin is also used as the subclock input/output oscillation pin.
5	PG1/X0A	C	General-purpose I/O port This pin is also used as the subclock input oscillation pin.
6	V_{CC}	—	Power supply pin
7	C	—	Capacitor connection pin
8	PF2/RSTX	A	General-purpose I/O port This pin is also used as a reset pin. This pin is a dedicated reset pin in MB95F204H/F203H/F202H.
9	P62/TO10	D	General-purpose I/O port High-current port This pin is also used as the 8/16-bit composite timer ch. 1 output.
10	P63/TO11	D	General-purpose I/O port High-current port This pin is also used as the 8/16-bit composite timer ch. 1 output.
11	P64/EC1	D	General-purpose I/O port This pin is also used as the 8/16-bit composite timer ch. 1 clock input.
12	P00/AN00	E	General-purpose I/O port This pin is also used as the A/D converter analog input.
13	P01/AN01	E	General-purpose I/O port This pin is also used as the A/D converter analog input.
14	P02/INT02/AN02/SCK	E	General-purpose I/O port This pin is also used as the external interrupt input. This pin is also used as the A/D converter analog input. This pin is also used as the LIN-UART clock I/O.
15	P03/INT03/AN03/SOT	E	General-purpose I/O port This pin is also used as the external interrupt input. This pin is also used as the A/D converter analog input. This pin is also used as the LIN-UART data output.
16	P04/INT04/AN04/SIN /HCLK1/EC0	F	General-purpose I/O port This pin is also used as the external interrupt input. This pin is also used as the A/D converter analog input. This pin is also used as the LIN-UART data input. This pin is also used as the external clock input. This pin is also used as the 8/16-bit composite timer ch. 0 clock input.

(Continued)

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
17	P05/INT05/AN05/TO00 /HCLK2	E	General-purpose I/O port High-current port This pin is also used as the external interrupt input. This pin is also used as the A/D converter analog input. This pin is also used as the 8/16-bit composite timer ch. 0 output. This pin is also used as the external clock input.
18	P06/INT06/TO01	G	General-purpose I/O port High-current port This pin is also used as the external interrupt input. This pin is also used as the 8/16-bit composite timer ch. 0 output.
19	P07/INT07	G	General-purpose I/O port This pin is also used as the external interrupt input.
20	P12/EC0/DBG	H	General-purpose I/O port This pin is also used as the DBG input pin. This pin is also used as the 8/16-bit composite timer ch. 0 clock input.

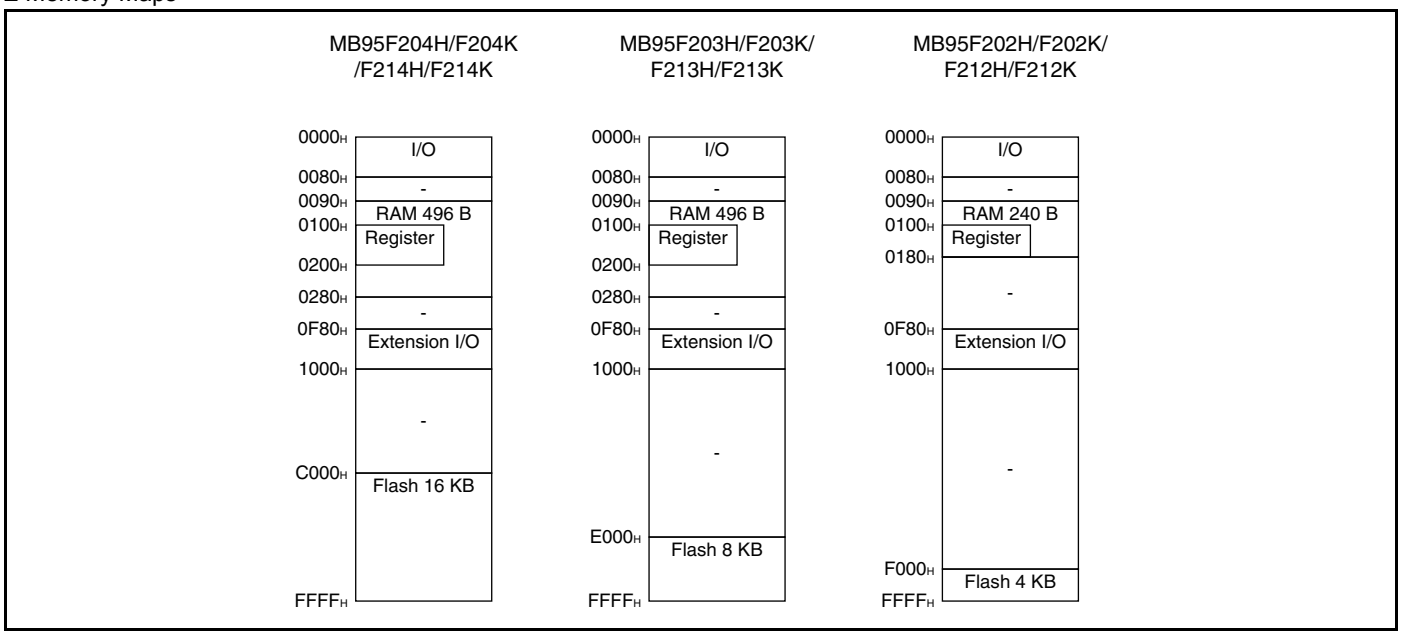
*: For the I/O circuit types, see “8.I/O Circuit Type”

13. CPU Core

Memory Space

The memory space of the MB95200H/210H Series is 64 KB in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95200H/210H Series are shown below.

■ Memory Maps



14. I/O Map (MB95200H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Disabled)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	—	(Disabled)	—	—
0007_H	SYCC	System clock control register	R/W	$XXXXXX11_B$
0008_H	STBC	Standby control register	R/W	$00000XXX_B$
0009_H	RSRR	Reset source register	R	$XXXXXXXX_B$
$000A_H$	TBTC	Timebase timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	00000000_B
$000D_H$	SYCC2	System clock control register 2	R/W	$XX100011_B$
$000E_H$ to 0015_H	—	(Disabled)	—	—
0016_H	PDR6	Port 6 data register	R/W	00000000_B
0017_H	DDR6	Port 6 direction register	R/W	00000000_B
0018_H to 0027_H	—	(Disabled)	—	—
0028_H	PDRF	Port F data register	R/W	00000000_B
0029_H	DDRF	Port F direction register	R/W	00000000_B
$002A_H$	PDRG	Port G data register	R/W	00000000_B
$002B_H$	DDRG	Port G direction register	R/W	00000000_B
$002C_H$	PUL0	Port 0 pull-up register	R/W	00000000_B
$002D_H$ to 0034_H	—	(Disabled)	—	—
0035_H	PULG	Port G pull-up register	R/W	00000000_B
0036_H	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000_B
0037_H	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000_B
0038_H	T11CR1	8/16-bit composite timer 11 status control register 1 ch. 1	R/W	00000000_B
0039_H	T10CR1	8/16-bit composite timer 10 status control register 1 ch. 1	R/W	00000000_B
$003A_H$ to 0048_H	—	(Disabled)	—	—
0049_H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$004A_H$	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000_B
$004B_H$	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000_B
$004C_H$ to $004F_H$	—	(Disabled)	—	—
0050_H	SCR	LIN-UART serial control register	R/W	00000000_B
0051_H	SMR	LIN-UART serial mode register	R/W	00000000_B
0052_H	SSR	LIN-UART serial status register	R/W	00001000_B
0053_H	RDR/TDR	LIN-UART receive/transmit data register	R/W	00000000_B
0054_H	ESCR	LIN-UART extended status control register	R/W	00000100_B
0055_H	ECCR	LIN-UART extended communication control register	R/W	$000000XX_B$
0056_H to $006B_H$	—	(Disabled)	—	—
$006C_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000_B
$006D_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000_B
$006E_H$	ADDH	8/10-bit A/D converter data register (Upper)	R/W	00000000_B
$006F_H$	ADDL	8/10-bit A/D converter data register (Lower)	R/W	00000000_B
0070_H to 0071_H	—	(Disabled)	—	—
0072_H	FSR	Flash memory status register	R/W	$000X0000_B$
0073_H to 0075_H	—	(Disabled)	—	—
0076_H	WREN	Wild register address compare enable register	R/W	00000000_B
0077_H	WROR	Wild register data test setting register	R/W	00000000_B
0078_H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	ILR2	Interrupt level setting register 2	R/W	11111111_B
$007C_H$	ILR3	Interrupt level setting register 3	R/W	11111111_B
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—
$0F80_H$	WRARH0	Wild register address setting register (Upper) ch. 0	R/W	00000000_B

(Continued)

15. I/O Map (MB95210H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Disabled)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	—	(Disabled)	—	—
0007_H	SYCC	System clock control register	R/W	$XXXXXX11_B$
0008_H	STBC	Standby control register	R/W	$00000XXX_B$
0009_H	RSRR	Reset source register	R	$XXXXXXXX_B$
$000A_H$	TBTC	Timebase timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	00000000_B
$000D_H$	SYCC2	System clock control register 2	R/W	$XX100011_B$
$000E_H$ to 0015_H	—	(Disabled)	—	—
0016_H	—	(Disabled)	—	—
0017_H	—	(Disabled)	—	—
0018_H to 0027_H	—	(Disabled)	—	—
0028_H	PDRF	Port F data register	R/W	00000000_B
0029_H	DDRF	Port F direction register	R/W	00000000_B
$002A_H$	—	(Disabled)	—	—
$002B_H$	—	(Disabled)	—	—
$002C_H$	PUL0	Port 0 pull-up register	R/W	00000000_B
$002D_H$ to 0034_H	—	(Disabled)	—	—
0035_H	—	(Disabled)	—	—
0036_H	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000_B
0037_H	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000_B
0038_H	—	(Disabled)	—	—
0039_H	—	(Disabled)	—	—
$003A_H$ to 0048_H	—	(Disabled)	—	—
0049_H	—	(Disabled)	—	—

(Continued)

18.4 AC Characteristics

18.4.1 Clock Timing

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	X1 open	1	—	12	MHz	When the main external clock is used
		X0, X1	*	1	—	32.5	MHz	
		HCLK1, HCLK2	—					
	F_{CRH}	—	—	9.7	10	10.3	MHz	When the main CR clock is used 3.3 V ≤ Vcc ≤ 5.5 V(-40 °C ≤ T_A ≤ 40 °C) 2.4 V ≤ Vcc < 3.3 V(0 °C ≤ T_A ≤ 40 °C)
				7.76	8	8.24	MHz	
				0.97	1	1.03	MHz	
				9.55	10	10.45	MHz	When the main CR clock is used 3.3 V ≤ Vcc ≤ 5.5 V (40 °C < T_A ≤ 85 °C)
				7.64	8	8.36	MHz	
				0.955	1	1.045	MHz	
				9.5	10	10.5	MHz	When the main CR clock is used 2.4 V ≤ Vcc < 3.3 V (-40 °C ≤ T_A < 0 °C, 40 °C < T_A ≤ 85 °C)
				7.6	8	8.4	MHz	
				0.95	1	1.05	MHz	
	F_{CL}	X0A, X1A	—	–	32.768	—	kHz	When the sub oscillation circuit is used
				–	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	200	kHz	When the sub-CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	X1 open	83.4	—	1000	ns	When the external clock is used
		X0, X1	*	30.8	—	1000	ns	
		HCLK1, HCLK2	—					
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the subclock is used
Input clock pulse width	t_{WH1} t_{WL1}	X0	X1 open	33.4	—	—	ns	When the external clock is used, the duty ratio should range between 40% and 60%.
		X0, X1	*	12.4	—	—	ns	
		HCLK1, HCLK2	—					
	t_{WH2} t_{WL2}	X0A	—	—	15.2	—	µs	

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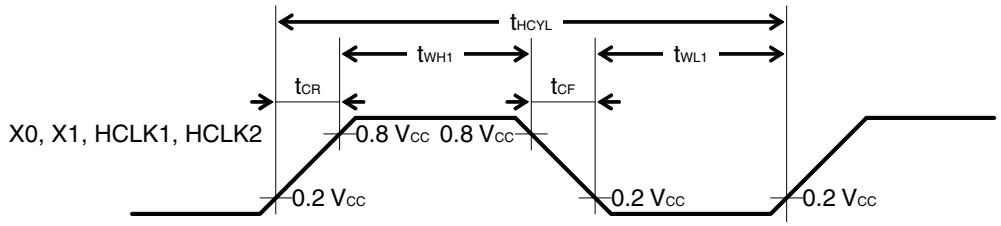
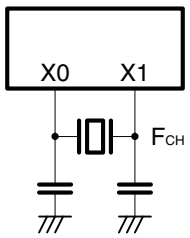
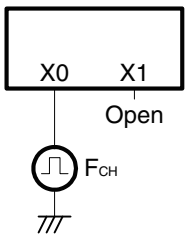


- Figure of main clock input port external connection

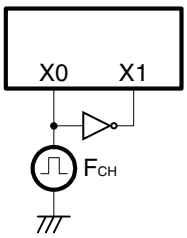
When a crystal oscillator or a ceramic oscillator is used



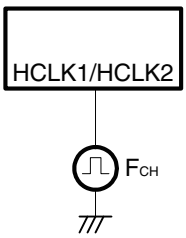
When the external clock is used (X1 is open)

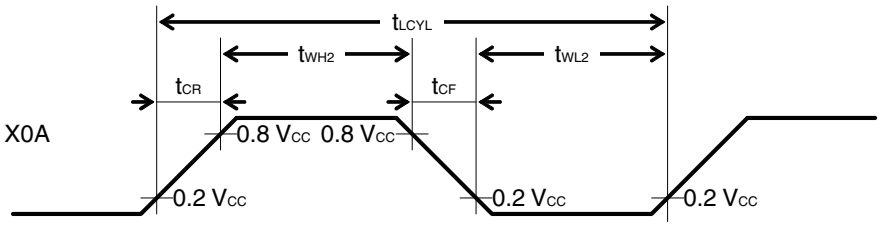


When the external clock is used



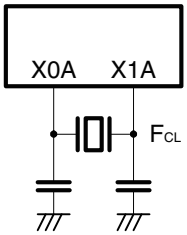
When the external clock is used



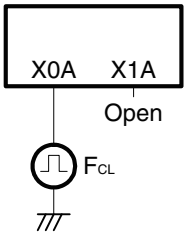


- Figure of subclock input port external connection

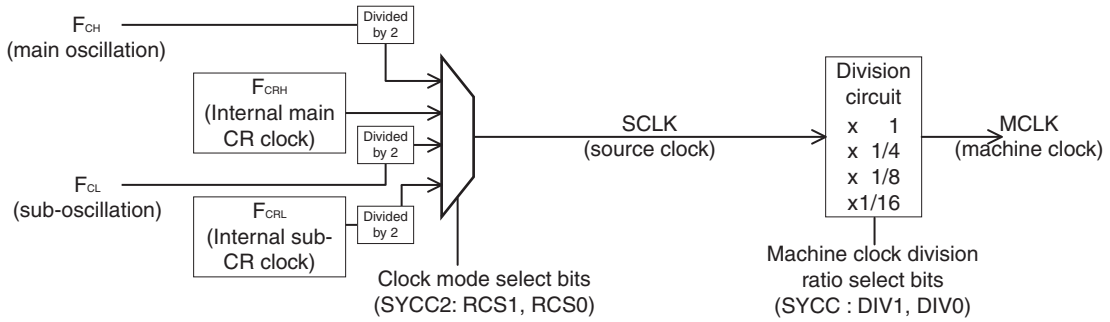
When a crystal oscillator or a ceramic oscillator is used



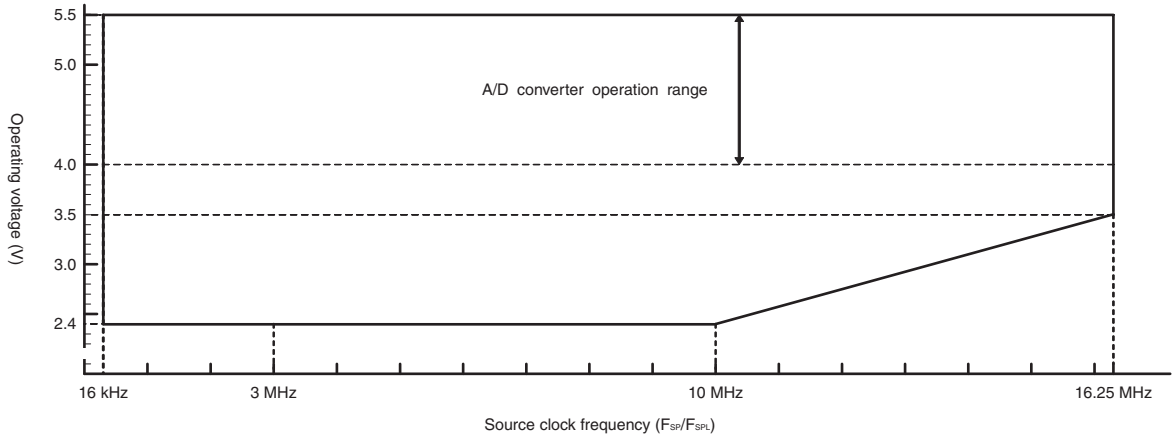
When the external clock is used



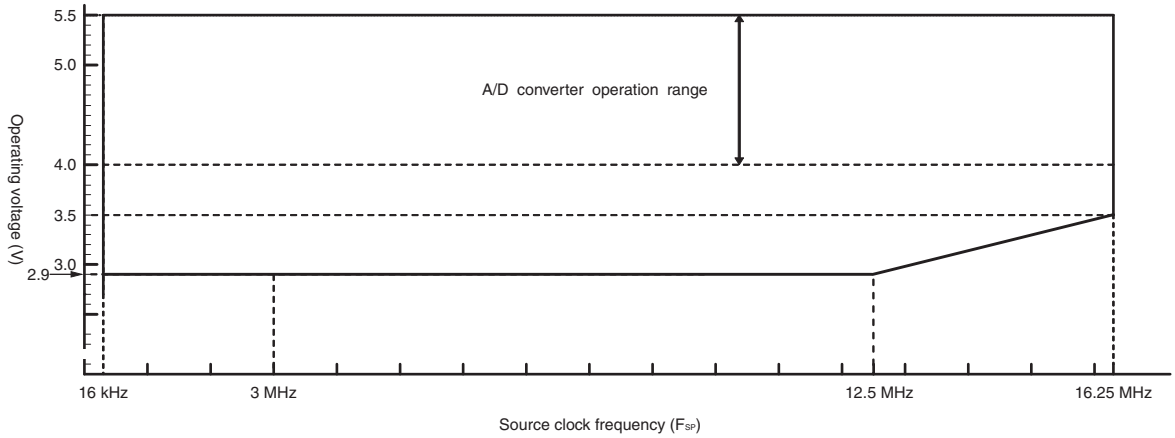
- Schematic diagram of the clock generation block



- Operating voltage - Operating frequency (When T_A = -40 °C to +85 °C)
  - ➢ MB95200H/210H (without the on-chip debug function)



- Operating voltage - Operating frequency (When T_A = +5 °C to +35 °C)
  - ➢ MB95200H/210H (with the on-chip debug function)



18.4.3 External Reset

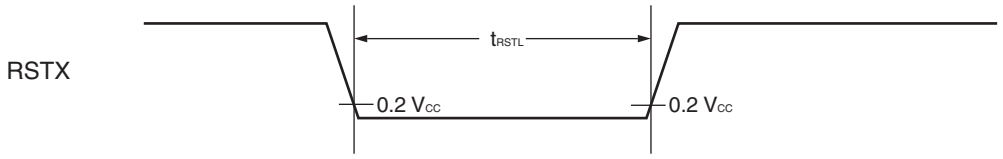
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
RSTX "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	In normal operation
		Oscillation time of the oscillator*2+100	—	µs	In stop mode, subclock mode, sub-sleep mode, watch mode, and power on
		100	—	µs	In timebase timer mode

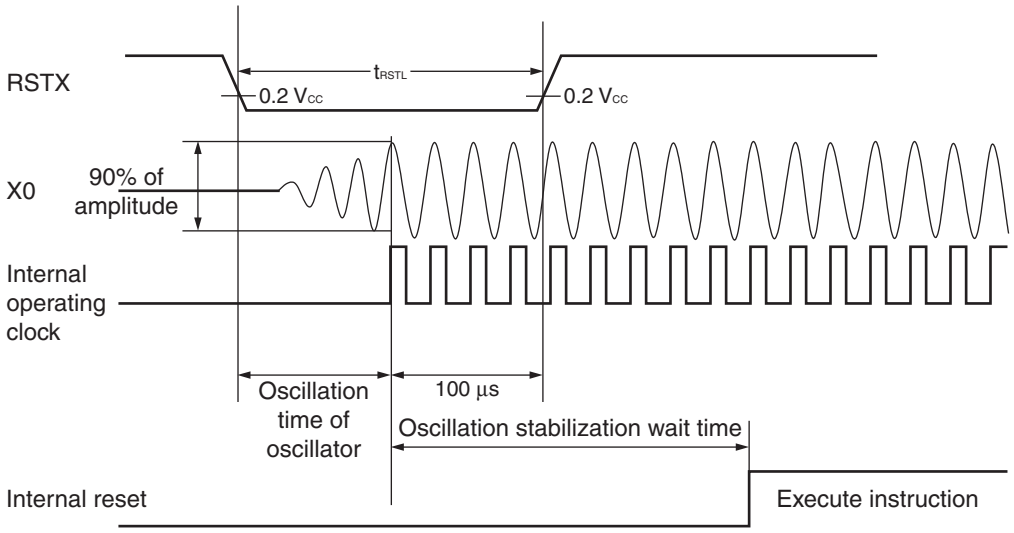
*1: See "18.4.2. Source Clock/Machine Clock" for t_{MCLK}.

*2: The oscillation time of an oscillator is the time that the amplitude reaches 90%. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of µs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several µs and several ms.

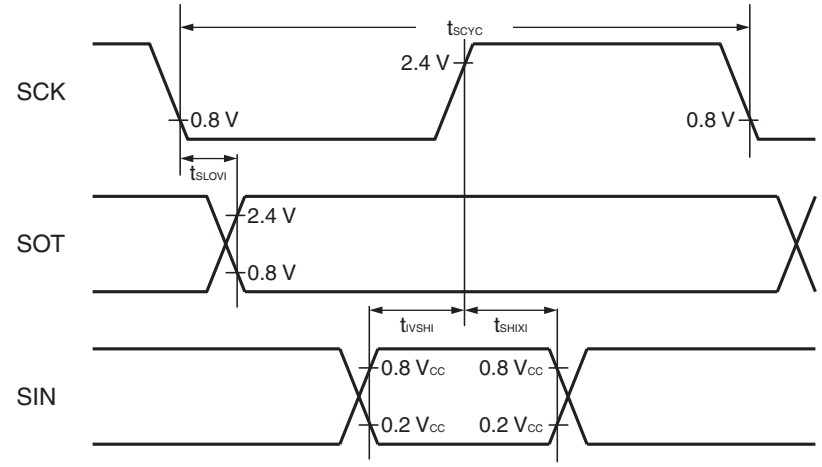
- In normal operation



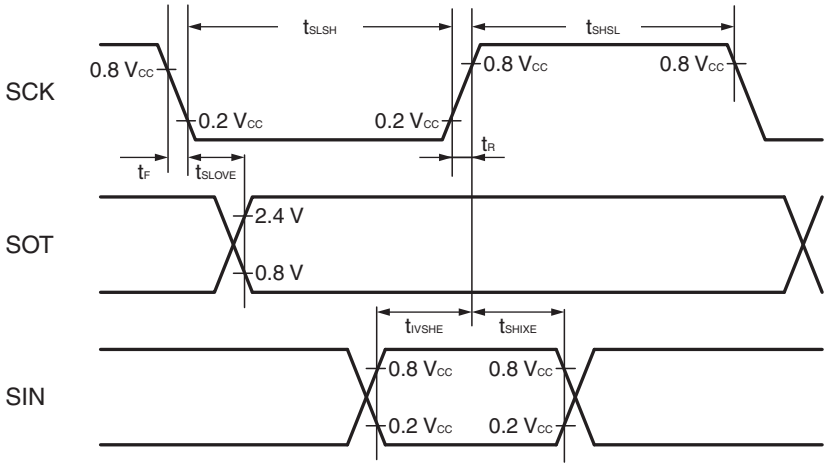
- In stop mode, sub-clock mode, sub-sleep mode, watch mode, and power-on



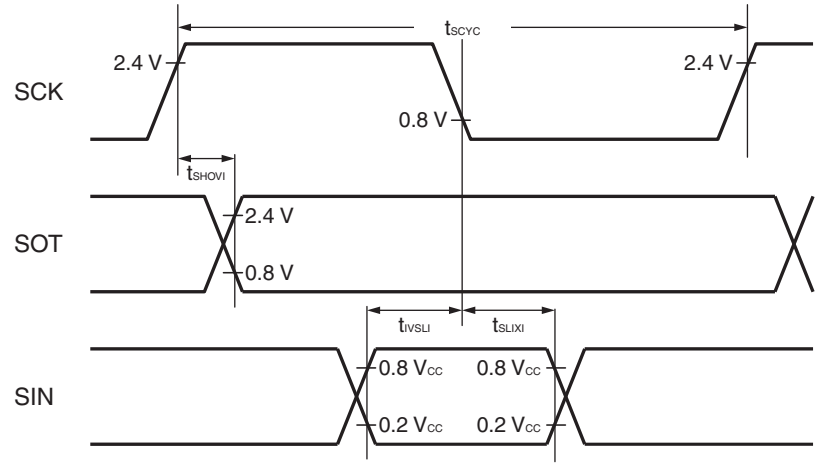
- Internal shift clock mode



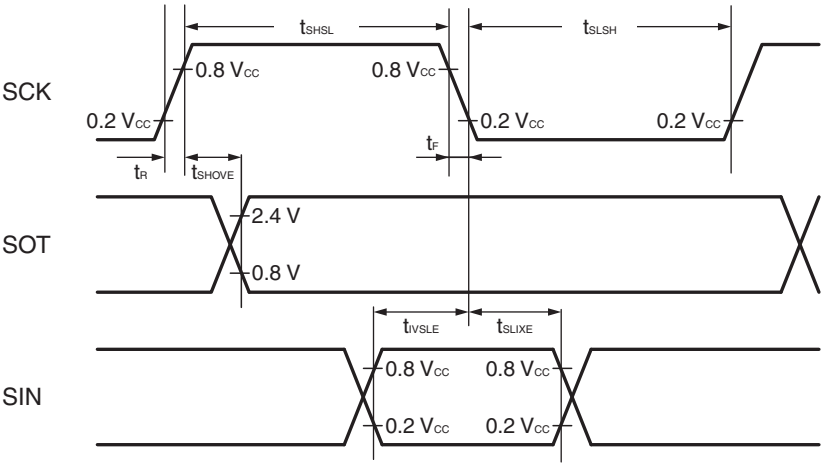
- External shift clock mode



- Internal shift clock mode



- External shift clock mode



*Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2.*
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)

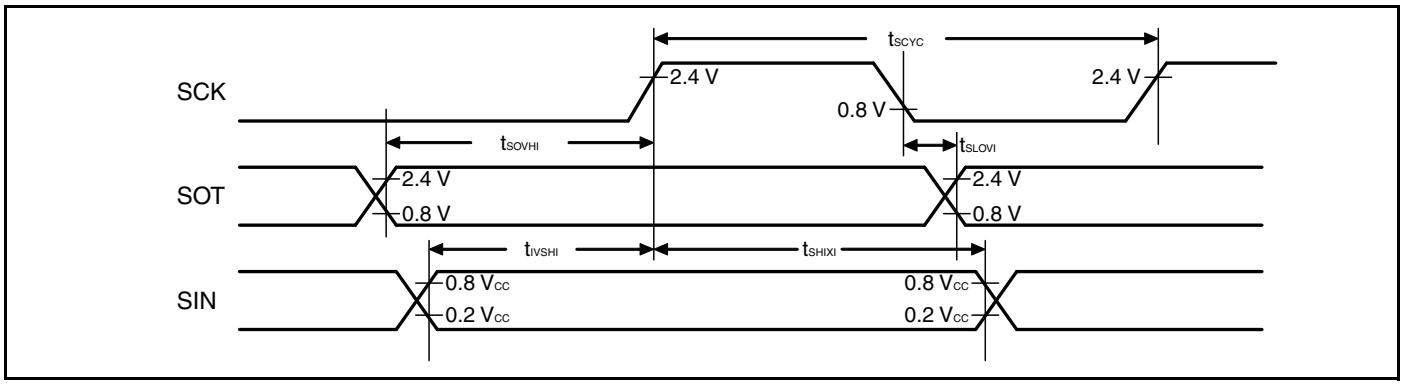
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF+1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCK, SOT		-95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3+190	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “18.4.2.Source Clock/Machine Clock” for t_{MCLK}.



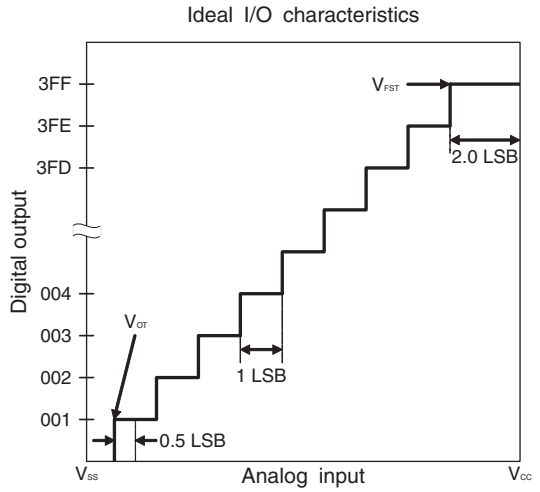
18.4.7 Low-voltage Detection

(V_{SS} = 0.0 V, T_A = -40°C to +85°C)

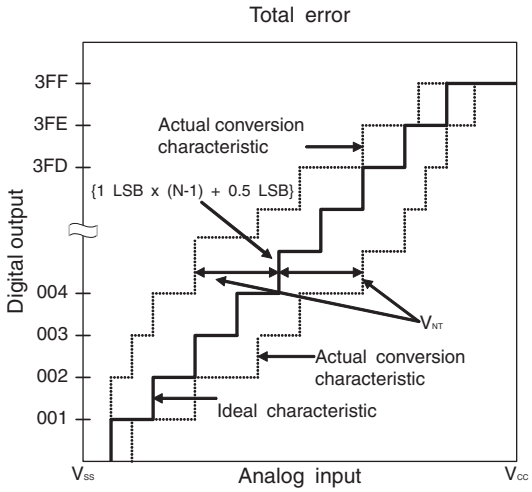
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
Detection voltage	V_{DL-}	2.42	2.6	2.78	V	At power supply fall
Hysteresis width	V_{HYS}	70	100	—	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	1	—	—	µs	Slope of power supply that the reset release signal generates
		—	3000	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	300	—	—	µs	Slope of power supply that the reset detection signal generates
		—	300	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	300	µs	
Reset detection delay time	t_{d2}	—	—	20	µs	

18.5.3 Definitions of A/D Converter Terms

- Resolution
  It indicates the level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.
- Linearity error (unit: LSB)
  It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point ("00 0000 0000" ← → "00 0000 0001") of a device to the full-scale transition point ("11 1111 1111" ← → "11 1111 1110") of the same device.
- Differential linear error (unit: LSB)
  It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
  It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.



$$1\ LSB = \frac{V_{CC} - V_{SS}}{1024}\ (V)$$



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB \times (N - 1) + 0.5\ LSB\}}{1\ LSB}\ [LSB]$$

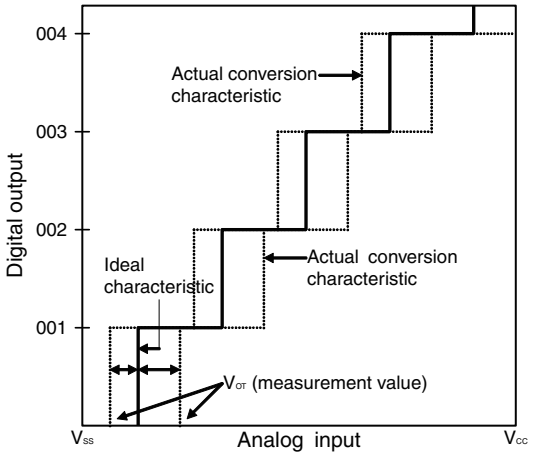
N : A/D converter digital output value

V_{NT}: Voltage at which the digital output transits from (N - 1) to N

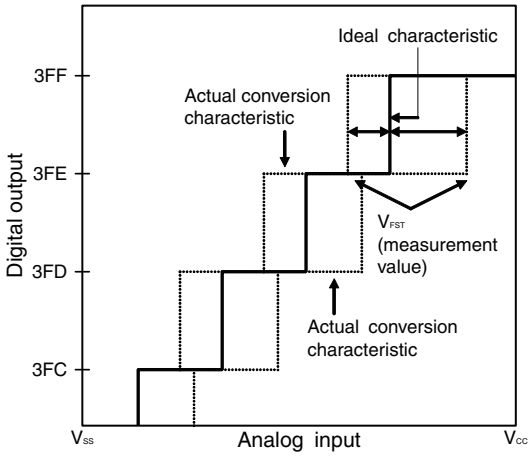
(Continued)

(Continued)

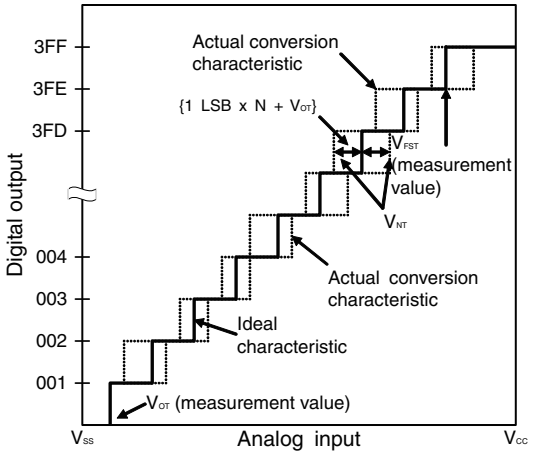
Zero transition error



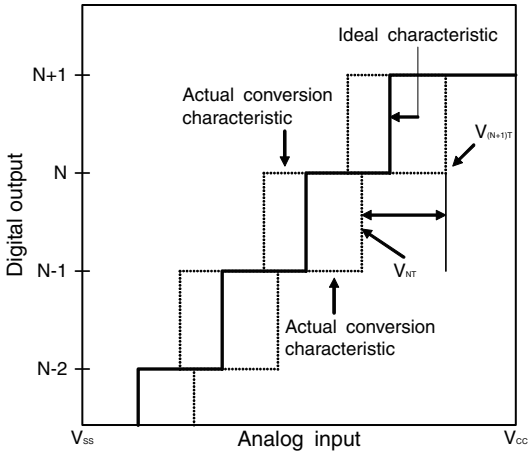
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

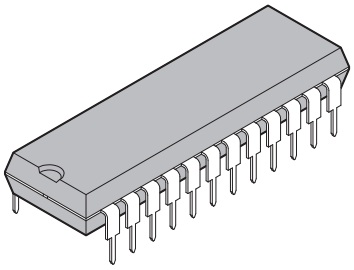
N : A/D converter digital output value

V_{NT}: Voltage at which the digital output transits from (N - 1) to N

V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

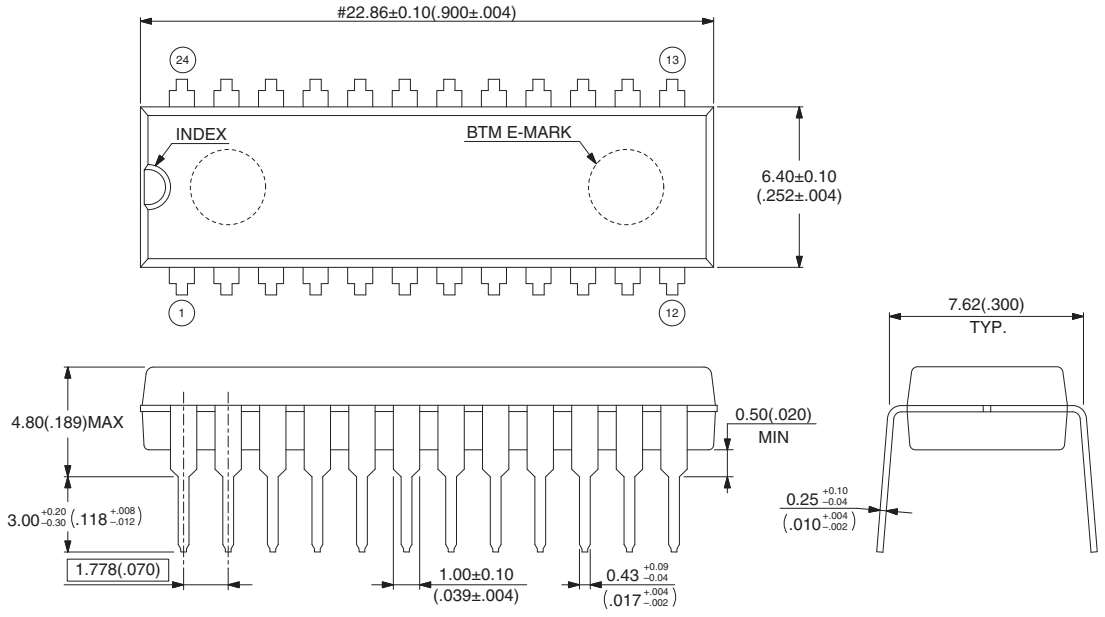
V_{FST} (ideal value) = V_{CC} - 2.0 LSB [V]

22. Package Dimensions

24-pin plastic SDIP		
 (DIP-24P-M07)	Lead pitch	1.778 mm
	Package width × package length	6.40 mm × 22.86 mm
	Sealing method	Plastic mold
	Mounting height	4.80 mm Max

24-pin plastic SDIP
(DIP-24P-M07)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)

23. Major Changes

Spansion Publication Number: DS07-12623-5E

Page	Section	Change results
30	Electrical Characteristics 1. Absolute Maximum Ratings	Changed the characteristics of Input voltage.
33	3. DC Characteristics	Corrected the maximum value of “H” level input voltage for PF2 pin. $V_{CC} + 0.3 \rightarrow 10.5$
		Corrected the maximum value of Open-drain output application voltage. 0.2Vcc → Vss + 5.5
36		Added the footnote *5.
39	4. AC Characteristics (1) Clock Timing	Added a figure of HCLK1/HCLK2.
42	(2) Source Clock/Machine Clock	Corrected the graph of Operating voltage - Operating frequency (with the on-chip debug function). (Corrected the pitch)
43	(3) External Reset	Added “and power on” to the remarks column.
58	6. Flash Memory Program/Erase Characteristics	Added the row of “Current drawn on PF2”.
		Corrected the minimum value of Power supply voltage at erase/program. 4.5 → 3.0

Note: Please see “Document History” about later revised information.

Document History

Document Title: MB95200H/210H Series F^{2}MC-8FX 8-bit Microcontroller **Document Number: 002-07463**				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	AKIH	07/16/2010	Migrated to Cypress and assigned document number 002-07463. No change to document contents or format.
*A	5177811	AKIH	03/18/2016	Updated to Cypress format.