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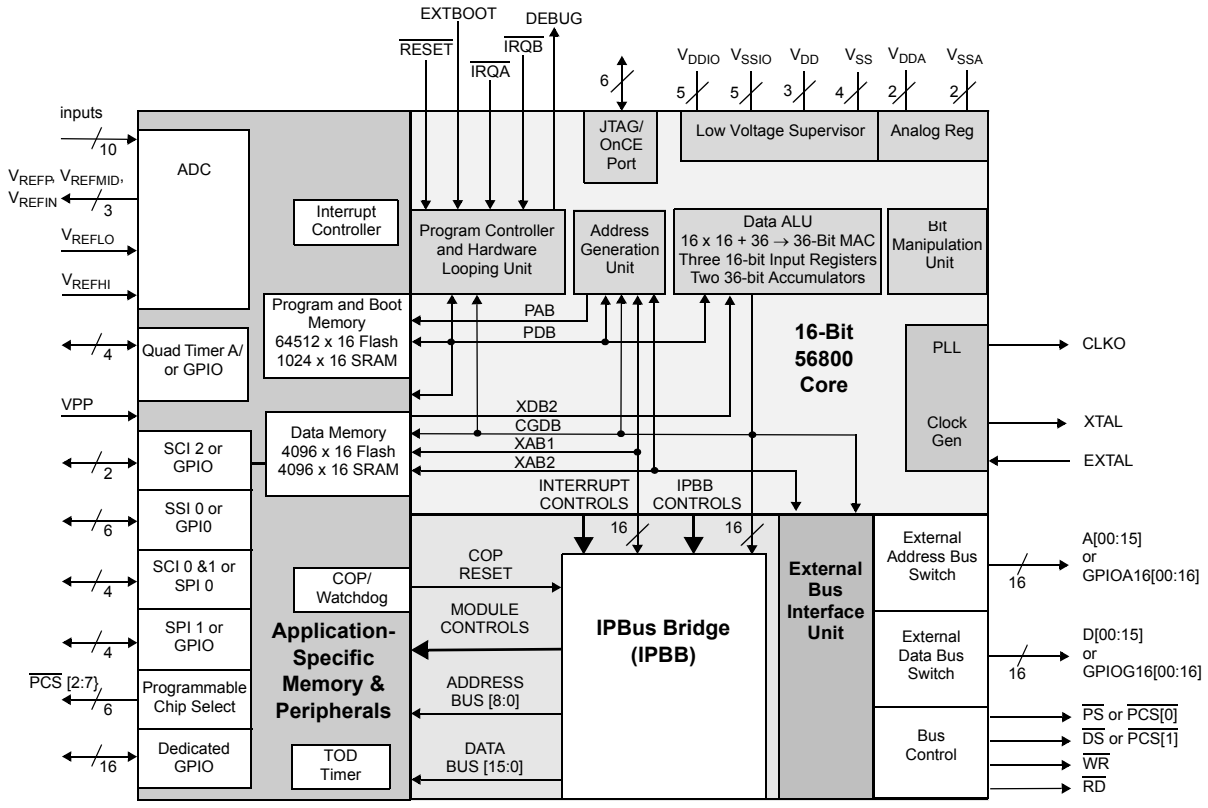
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800
Core Size	16-Bit
Speed	80MHz
Connectivity	EBI/EMI, SCI, SPI, SSI
Peripherals	POR, PWM, WDT
Number of I/O	64
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 2.75V
Data Converters	A/D 10x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (14x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=dsp56f827fg80e

56F827 General Description

- Up to 40 MIPS at 80MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- Hardware DO and REP loops
- 64K × 16-bit words (128KB) Program Flash
- 1K × 16-bit words (2KB) Program RAM
- 4K × 16-bit words (8KB) Data Flash
- 4K × 16-bit words (8KB) Data RAM
- Up to 64K × 16-bit words (128KB) external memory expansion each for Program and Data memory
- JTAG/OnCE™ for debugging
- General Purpose Quad Timer
- MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- 8-channel Programmable Chip Select
- 10-channel, 12-bit ADC
- Synchronous Serial Interface (SSI)
- Serial Port Interface (SPI)
- Serial Communications Interface (SCI)
- Time-of-Day (TOD) Timer
- 128-pin LQFP Package
- 16-dedicated and 48 shared GPIO



56F827 Block Diagram

Table 2-2 56F827 Signal and Package Information for the 128 Pin LQFP (Continued)

Signal Name	Pin No.	Type	Description
V_{PP}	90	Input	**V_{PP}**—This pin should be left unconnected as an open circuit for normal functionality.
EXTAL	59	Input	**External Crystal Oscillator Input**—This input should be connected to a 4MHz external crystal or ceramic resonator. For more information, please refer to **Section 3.6**. This pin can also be connected to an external clock source. For more information, please refer to **Section 3.6.3**.
XTAL (CLOCKIN)	60	Output Input	**Crystal Oscillator Output**—This output connects the internal crystal oscillator output to an external crystal or ceramic resonator. If an external clock source over 4MHz is used, XTAL must be used as the input and EXTAL connected to V_{SS}. For more information, please refer to **Section 3.6.3.** **External Clock Input**—This input should be used when using an external clock or ceramic resonator.
CLKO	57	Output	**Clock Output**—This pin outputs a buffered clock signal. By programming the CLKO Select Register (CLKOSR), the user can select between outputting a version of the signal applied to XTAL and a version of the device master clock at the output of the PLL. The clock frequency on this pin can be disabled by programming the CLKO Select Register (CLKOSR).

Table 2-2 56F827 Signal and Package Information for the 128 Pin LQFP (Continued)

Signal Name	Pin No.	Type	Description
$\overline{RD}$	15	Output	**Read Enable**—$\overline{RD}$ is asserted during external memory read cycles. When $\overline{RD}$ is asserted low, pins D0–D15 become inputs and an external device is enabled onto the device data bus. When $\overline{RD}$ is deasserted high, the external data is latched inside the device. When $\overline{RD}$ is asserted, it qualifies the A0–A15, $\overline{PS}$, and $\overline{DS}$ pins. $\overline{RD}$ can be connected directly to the $\overline{OE}$ pin of a Static RAM or ROM.
$\overline{WR}$	16	Output	**Write Enable**—$\overline{WR}$ is asserted during external memory write cycles. When $\overline{WR}$ is asserted low, pins D0–D15 become outputs and the device puts data on the bus. When $\overline{WR}$ is deasserted high, the external data is latched inside the external device. When $\overline{WR}$ is asserted, it qualifies the A0–A15, $\overline{PS}$, and $\overline{DS}$ pins. $\overline{WR}$ can be connected directly to the $\overline{WE}$ pin of a Static RAM.
TA0 (GPIOF0)	112	Input/Output Input/Output	**TA0–3**—Timer A Channels 0, 1, 2, and 3 **Port F GPIO**—These four General Purpose I/O (GPIO) pins can be individually programmed as input or output. After reset, the default state is Quad Timer.
TA1 (GPIOF1)	111		
TA2 (GPIOF2)	110		
TA3 (GPIOF3)	109		
TCK	44	Input (Schmitt)	**Test Clock Input**—This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/OnCE port. The pin is connected internally to a pull-down resistor.
TMS	46	Input (Schmitt)	**Test Mode Select Input**—This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
TDI	48	Input (Schmitt)	**Test Data Input**—This input pin provides a serial input data stream to the JTAG/OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
TDO	47	Input/Output	**Test Data Output**—This tri-statable output pin provides a serial output data stream from the JTAG/OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
$\overline{TRST}$	45	Input (Schmitt)	**Test Reset**—As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{TRST}$ should be asserted whenever $\overline{RESET}$ is asserted. The only exception occurs in a debugging environment when a hardware device reset is required and it is necessary not to reset the JTAG/OnCE module. In this case, assert $\overline{RESET}$, but do not assert $\overline{TRST}$. $\overline{TRST}$ must always be asserted at power-up. **Note:** For normal operation, connect $\overline{TRST}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{TRST}$ may be tied to V_{SS} through a 1K resistor.
$\overline{DE}$	41	Output	**Debug Event**—$\overline{DE}$ provides a low pulse on recognized debug events.

Table 2-2 56F827 Signal and Package Information for the 128 Pin LQFP (Continued)

Signal Name	Pin No.	Type	Description
GPIOB0	124	Input/Output	**Port B GPIO**—These eight dedicated General Purpose I/O (GPIO) pins can be individually programmed as input or output pins. After reset, the default state is GPIO input.
GPIOB1	123		
GPIOB2	122		
GPIOB3	121		
GPIOB4	120		
GPIOB5	119		
GPIOB6	118		
GPIOB7	117		
GPIOD0	98	Input/ Output	**Port D GPIO**—These eight dedicated GPIO pins can be individually programmed as an input or output pins. After reset, the default state is GPIO input.
GPIOD1	97		
GPIOD2	96		
GPIOD3	95		
GPIOD4	94		
GPIOD5	93		
GPIOD6	92		
GPIOD7	91		
SRD (GPIOC0)	55	Input/Output Input/Output	**SSI Receive Data (SRD)—**This input pin receives serial data and transfers the data to the SSI Receive Shift Receiver. **Port C GPIO**—This is a General Purpose I/O (GPIO) pin with the capability of being individually programmed as input or output. After reset, the default state is GPIO input.
SRFS (GPIOC1)	54	Input/Output Input/Output	**SSI Serial Receive Frame Sync (SRFS)**—This bidirectional pin is used by the receive section of the SSI as frame sync I/O or flag I/O. The STFS can be used only by the receiver. It is used to synchronize data transfer and can be an input or an output. **Port C GPIO**—This is a General Purpose I/O (GPIO) pin with the capability of being individually programmed as input or output. After reset, the default state is GPIO input.
SRCK (GPIOC2)	53	Input/Output Input/Output	**SSI Serial Receive Clock (SRCK)—**This bidirectional pin provides the serial bit rate clock for the Receive section of the SSI. The clock signal can be continuous or gated and can be used by both the transmitter and receiver in synchronous mode. **Port C GPIO**—This is a General Purpose I/O (GPIO) pin with the capability of being individually programmed as input or output. After reset, the default state is GPIO input.

Table 2-2 56F827 Signal and Package Information for the 128 Pin LQFP (Continued)

Signal Name	Pin No.	Type	Description
$\overline{SS}$ (GPIOF7)	99	Input/Output Input/Output	**SPI Slave Select**—In master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave. **Port F GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as input or output. After reset, the default state is $\overline{SS}$.
TXD0 (SCLK0)	108	Output Input/Output	**Transmit Data (TXD0)**—transmit data output **SPI Serial Clock**—In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. After reset, the default state is SCI output.
RXD0 (MOSI0)	107	Input Input/Output	**Receive Data (RXD0)**—receive data input **SPI Master Out/Slave In**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
TXD1 (MISO0)	106	Output Input/Output	**Transmit Data (TXD1)**—transmit data output **SPI Master In/Slave Out**—This serial data pin is an output to a master device and an input from a slave device. The master device places data on the MOSI line one half-cycle before the clock edge the slave device uses to latch the data. After reset, the default state is SCI input.
RXD1 ($\overline{SS0}$)	105	Input (Schmitt) Input	**Receive Data (RXD1)**— receive data input **SPI Slave Select**—In master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave. After reset, the default state is SCI input.
TXD2 (GPIOC6)	104	Output Input/Output	**Transmit Data (TXD2)**—transmit data output **Port C GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as input or output. After reset, the default state is GPIO output.
RXD2 (GPIOC7)	103	Input/Output Input/Output	**Receive Data (RXD2)**— receive data input **Port C GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as input or output. After reset, the default state is GPIO input.

Table 3-3 Thermal Characteristics[6]

Characteristic	Comments	Symbol	Value	Unit	Notes
			128-pin LQFP		
Junction to ambient Natural convection		$R_{\theta JA}$	50.8	°C/W	2
Junction to ambient (@1m/sec)		$R_{\theta JMA}$	46.5	°C/W	2
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$ (2s2p)	43.9	°C/W	1,2
Junction to ambient (@1m/sec)	Four layer board (2s2p)	$R_{\theta JMA}$	41.7	°C/W	1,2
Junction to case		$R_{\theta JC}$	13.9	°C/W	3
Junction to center of case		Ψ_{JT}	1.2	°C/W	4
I/O pin power dissipation		$P_{I/O}$	User Determined	W	
Power dissipation		P_D	$P_D = (I_{DD} \times V_{DD} + P_{I/O})$	W	
Junction to center of case		P_{DMAX}	(TJ - TA) /RθJA	W	7

Notes:

1. Theta-JA determined on 2s2p test boards is frequently lower than would be observed in an application. Determined on 2s2p thermal test board.
2. Junction to ambient thermal resistance, Theta-JA ($R_{\theta JA}$) was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection. Theta-JA was also simulated on a thermal test board with two internal planes (2s2p where s is the number of signal layers and p is the number of planes) per JESD51-6 and JESD51-7. The correct name for Theta-JA for forced convection or with the non-single layer boards is Theta-JMA.
3. Junction to case thermal resistance, Theta-JC ($R_{\theta JC}$), was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the "case" temperature. The basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.
4. Thermal Characterization Parameter, Psi-JT (Ψ_{JT}), is the "resistance" from junction to reference point thermocouple on top center of case as defined in JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in steady state customer environments.
5. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
6. See Section 5.1 from more details on thermal design considerations.
7. TJ = Junction Temperature
   TA = Ambient Temperature

Table 3-4 DC Electrical Characteristics (Continued)

Operating Conditions: V_{SSIO}=V_{SS} = V_{SSA} = 0V, V_{DDA} =V_{DDIO}=3.0–3.6V, V_{DD} = 2.25–2.75V, T_A = –40° to +85°C, C_L ≤ 50pF, f_{op} = 80MHz

Characteristic	Symbol	Min	Typ	Max	Unit
PWM pin output sink current[4]	I_{OLP}	16	—	—	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF
V_{DD} supply current	I_{DDT}[5]				
Run [6]		—	60	90	mA
Wait[7]		—	35	50	mA
Stop		—	6	15	mA
Low Voltage Interrupt, V_{DDIO} power supply[8]	V_{EIO}	2.4	2.7	3.0	V
Low Voltage Interrupt, V_{DD} power supply[9]	V_{EIC}	2.0	2.2	2.4	V
Power-on Reset[10]	V_{POR}	—	1.7	2.0	V

1. Schmitt Trigger inputs are: EXTBOOT, $\overline{IRQA}$, $\overline{IRQB}$, $\overline{RESET}$, TCS, TCK, $\overline{TRST}$, TMS, TDI, and RXD1.
2. Analog inputs are: ANA[0:7], XTAL and EXTAL. Specification assumes ADC is not sampling.
3. PWM pin output source current measured with 50% duty cycle.
4. PWM pin output sink current measured with 50% duty cycle.
5. I_{DDT} = I_{DD} + I_{DDA} (Total supply current for V_{DD} + V_{DDA})
6. Run (operating) I_{DD} measured using 4MHz clock source. All inputs 0.2V from rail; outputs unloaded. All ports configured as inputs; measured with all modules enabled.
7. Wait I_{DD} measured using external square wave clock source (f_{osc} = 4MHz) into XTAL; all inputs 0.2V from rail; no DC loads; less than 50pF on all outputs. C_L = 20pF on EXTAL; all ports configured as inputs; EXTAL capacitance linearly affects wait I_{DD}; measured with PLL enabled.
8. This low-voltage interrupt monitors the V_{DDIO} power supply. If V_{DDIO} drops below V_{EIO}, an interrupt is generated. Functionality of the device is guaranteed under transient conditions when V_{DDIO} ≥V_{EIO} (between the minimum specified V_{DDIO} and the point when the V_{EIO} interrupt is generated).
9. This low-voltage interrupt monitors the V_{DD} power supply. If V_{DDIO} drops below V_{EIC}, an interrupt is generated. Functionality of the device is guaranteed under transient conditions when V_{DD} ≥V_{EIC} (between the minimum specified V_{DD} and the point when the V_{EIC} interrupt is generated).
10. Power–on reset occurs whenever the V_{DD} power supply drops below V_{POR}. While power is ramping up, this signal remains active as long as V_{DD} is below V_{POR}, no matter how long the ramp-up rate is.

3.6.4 Phase Locked Loop Timing

Table 3-9 PLL Timing

Operating Conditions: $V_{SSIO}=V_{SS}=V_{SSA}=0V$, $V_{DDA}=V_{DDIO}=3.0–3.6V$, $V_{DD}=2.25–2.75V$, $T_A=–40°$ to $+85°C$, $C_L \le 50pF$, $f_{op}=80MHz$

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	2	4	6	MHz
PLL output frequency[2]	$f_{out}/2$	40	—	110	MHz
PLL stabilization time [3]-40° to +85°C	t_{plls}	—	1	10	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 4MHz input crystal.
2. ZCLK may not exceed 80MHz. For additional information on ZCLK and $f_{out}/2$, please refer to the OCCS chapter in the User Manual. ZCLK = f_{op}
3. This is the minimum time required after the PLL set-up is changed to ensure reliable operation.

3.7 External Bus Asynchronous Timing

Table 3-10 External Bus Asynchronous Timing[1, 2]

Operating Conditions: $V_{SSIO}=V_{SS}=V_{SSA}=0V$, $V_{DDA}=V_{DDIO}=3.0–3.6V$, $V_{DD}=2.25–2.75V$, $T_A=–40°$ to $+85°C$, $C_L \le 50pF$, $f_{op}=80MHz$

Characteristic	Symbol	Min	Max	Unit
Address Valid to $\overline{WR}$ Asserted	t_{AWR}	6.5	—	ns
$\overline{WR}$ Width Asserted Wait states = 0 Wait states > 0	t_{WR}	 7.5 (T*WS) + 7.5	 — —	 ns ns
$\overline{WR}$ Asserted to D0–D15 Out Valid	t_{WRD}	—	T + 4.2	ns
Data Out Hold Time from $\overline{WR}$ Deasserted	t_{DOH}	4.8	—	ns
Data Out Set Up Time to $\overline{WR}$ Deasserted Wait states = 0 Wait states > 0	t_{DOS}	 2.2 (T*WS) + 6.4	 — —	 ns ns
$\overline{RD}$ Deasserted to Address Not Valid	t_{RDA}	0	—	ns
Address Valid to $\overline{RD}$ Deasserted Wait states = 0 Wait states > 0	t_{ARDD}	 18.7 (T*WS) + 18.7	—	 ns ns

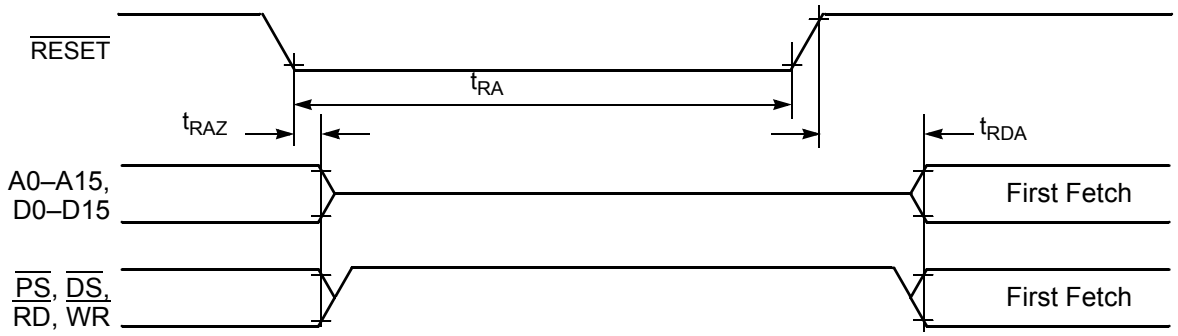


Figure 3-14 Asynchronous Reset Timing

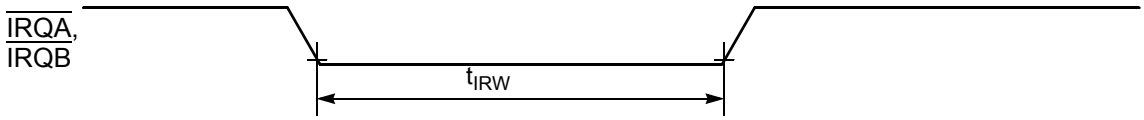
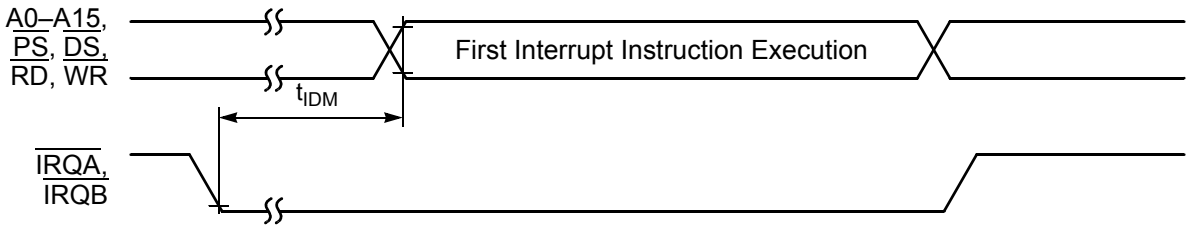
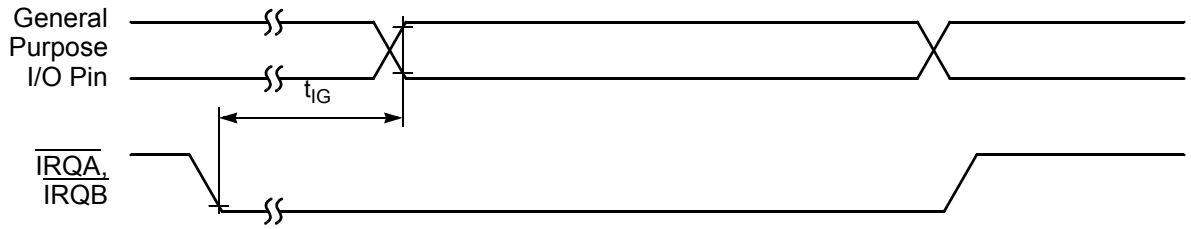


Figure 3-15 External Interrupt Timing (Negative-Edge-Sensitive)



a) First Interrupt Instruction Execution



b) General Purpose I/O

Figure 3-16 External Level-Sensitive Interrupt Timing

3.9 Serial Peripheral Interface (SPI) Timing

Table 3-12 SPI Timing[1]

Operating Conditions: V_{SSIO}=V_{SS} = V_{SSA} = 0V, V_{DDA} =V_{DDIO}=3.0–3.6V, V_{DD} = 2.25–2.75V, T_A = –40° to +85°C, C_L ≤ 50pF, f_{op} = 80MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 25	 — —	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	Figure 3-23
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	Figure 3-23
Clock (SCLK) high time Master Slave	t_{CH}	 24 12	 — —	ns ns	Figures 3-20, 3-21, 3-22, 3-23
Clock (SCLK) low time Master Slave	t_{CL}	 24.1 12	 — —	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Access time (time to data active from high-impedance state) Slave	t_A	 4.8	 15	 ns	Figure 3-23
Disable time (hold time to high-impedance state) Slave	t_D	 3.7	 15.2	 ns	Figure 3-23
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figures 3-20, 3-21, 3-22, 3-23

1. Parameters listed are guaranteed by design.

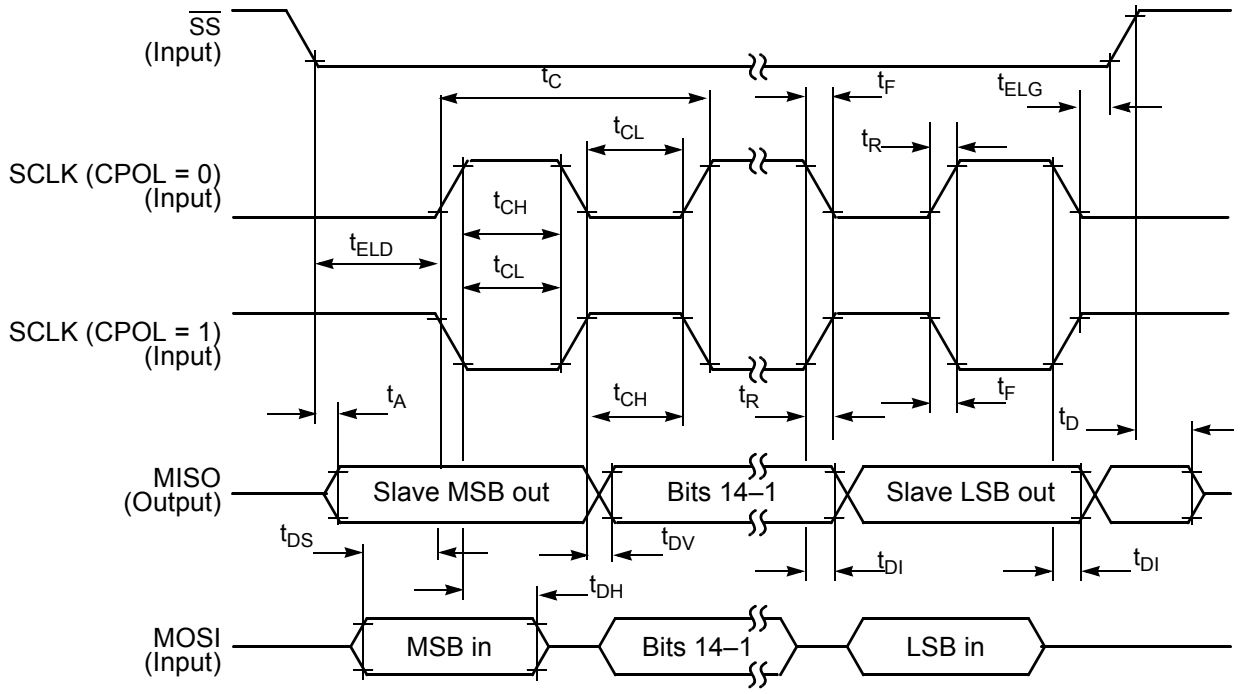


Figure 3-22 SPI Slave Timing (CPHA = 0)

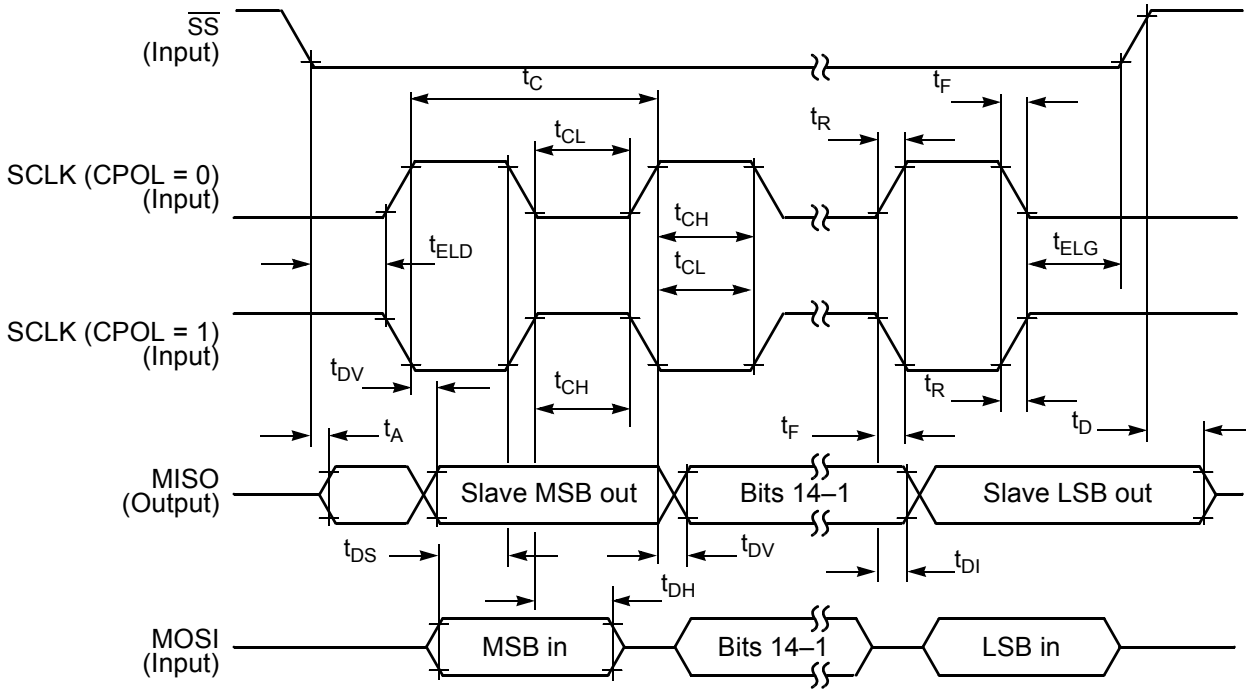
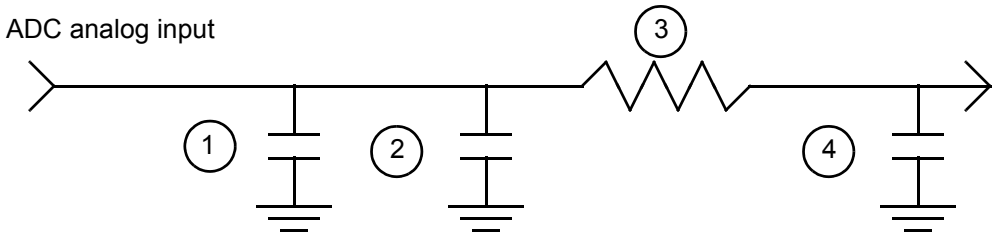


Figure 3-23 SPI Slave Timing (CPHA = 1)

2. Measured in 10-90% range.
3. LSB = Least Significant Bit.
4. Guaranteed by characterization.
5. $t_{AIC} = 1/f_{ADIC}$



1. Parasitic capacitance due to package, pin to pin, and pin to package base coupling. (1.8pf)
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing. (2.04pf)
3. Equivalent resistance for the ESD isolation resistor and the channel select mux. (500 ohms)
4. Sampling capacitor at the sample and hold circuit. Capacitor 4 is normally disconnected from the input and is only connected to it at sampling time. (1pf)

Figure 3-24 Equivalent Analog Input Circuit

3.11 Synchronous Serial Interface (SSI) Timing

Table 3-14 SSI Master Mode[1] Switching Characteristics

Operating Conditions: V_{SSIO}=V_{SS} = V_{SSA} = 0V, V_{DDA} =V_{DDIO}=3.0–3.6V, V_{DD} = 2.25–2.75V, T_A = –40° to +85°C, $C_L \leq$ 50pF, f_{op} = 80MHz

Parameter	Symbol	Min	Typ	Max	Units
STCK frequency	fs	—	—	10[2]	MHz
STCK period[3]	t_{SCKW}	100	—	—	ns
STCK high time	t_{SCKH}	50[4]	—	—	ns
STCK low time	t_{SCKL}	50[4]	—	—	ns
Output clock rise/fall time	—	—	4	—	ns
Delay from STCK high to STFS (bl) high - Master[5]	t_{TFSBHM}	0.1	—	0.5	ns
Delay from STCK high to STFS (wl) high - Master[5]	t_{TFSWHM}	0.1	—	0.5	ns
Delay from SRCK high to SRFS (bl) high - Master[5]	t_{RFSBHM}	0.6	—	1.3	ns
Delay from SRCK high to SRFS (wl) high - Master[5]	t_{RFSWHM}	0.6	—	1.3	ns
Delay from STCK high to STFS (bl) low - Master[5]	t_{TFSBLM}	-1.0	—	-0.1	ns

Table 3-15 SSI Slave Mode[1] Switching Characteristics

Operating Conditions: $V_{SSIO}=V_{SS} = V_{SSA} = 0V$, $V_{DDA} =V_{DDIO}=3.0–3.6V$, $V_{DD} = 2.25–2.75V$, $T_A = –40°$ to $+85°C$, $C_L \leq 50pF$, $f_{op} = 80MHz$

Parameter	Symbol	Min	Typ	Max	Units
Delay from STCK high to STFS (bl) high - Slave[5]	t_{TFSBHS}	0.1	—	46	ns
Delay from STCK high to STFS (wl) high - Slave[5]	t_{TFSWHS}	0.1	—	46	ns
Delay from SRCK high to SRFS (bl) high - Slave[5]	t_{RFSBHS}	0.1	—	46	ns
Delay from SRCK high to SRFS (wl) high - Slave[5]	t_{RFSWHS}	0.1	—	46	ns
Delay from STCK high to STFS (bl) low - Slave[5]	t_{TFSBLS}	-1	—	—	ns
Delay from STCK high to STFS (wl) low - Slave[5]	t_{TFSWLS}	-1	—	—	ns
Delay from SRCK high to SRFS (bl) low - Slave[5]	t_{RFSBLS}	-46	—	—	ns
Delay from SRCK high to SRFS (wl) low - Slave[5]	t_{RFSWLS}	-46	—	—	ns
STCK high to STXD enable from high impedance - Slave	t_{TXES}	—	—	—	ns
STCK high to STXD valid - Slave	t_{TXVS}	1	—	25	ns
STFS high to STXD enable from high impedance (first bit) - Slave	t_{FTXES}	5.5	—	25	ns
STFS high to STXD valid (first bit) - Slave	t_{FTXVS}	6	—	27	ns
STCK high to STXD not valid - Slave	t_{TXNVS}	11	—	13	ns
STCK high to STXD high impedance - Slave	t_{TXHIS}	11	—	28.5	ns
SRXD Setup time before SRCK low - Slave	t_{SS}	4	—	—	ns
SRXD Hold time after SRCK low - Slave	t_{HS}	4	—	—	ns
Synchronous Operation (in addition to standard external clock parameters)					
SRXD Setup time before STCK low - Slave	t_{TSS}	4	—	—	—
SRXD Hold time after STCK low - Slave	t_{THS}	4	—	—	—

1. Slave mode is externally generated clocks and frame syncs
2. Max clock frequency is IP_clk/4 = 40MHz / 4 = 10MHz for an 80MHz part.
3. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP=0 in SCR2 and RSCKP=0 in SCSR) and a non-inverted frame sync (TFSI=0 in SCR2 and RFSI=0 in SCSR). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS in the tables and in the figures.
4. 50% duty cycle
5. bl = bit length; wl = word length

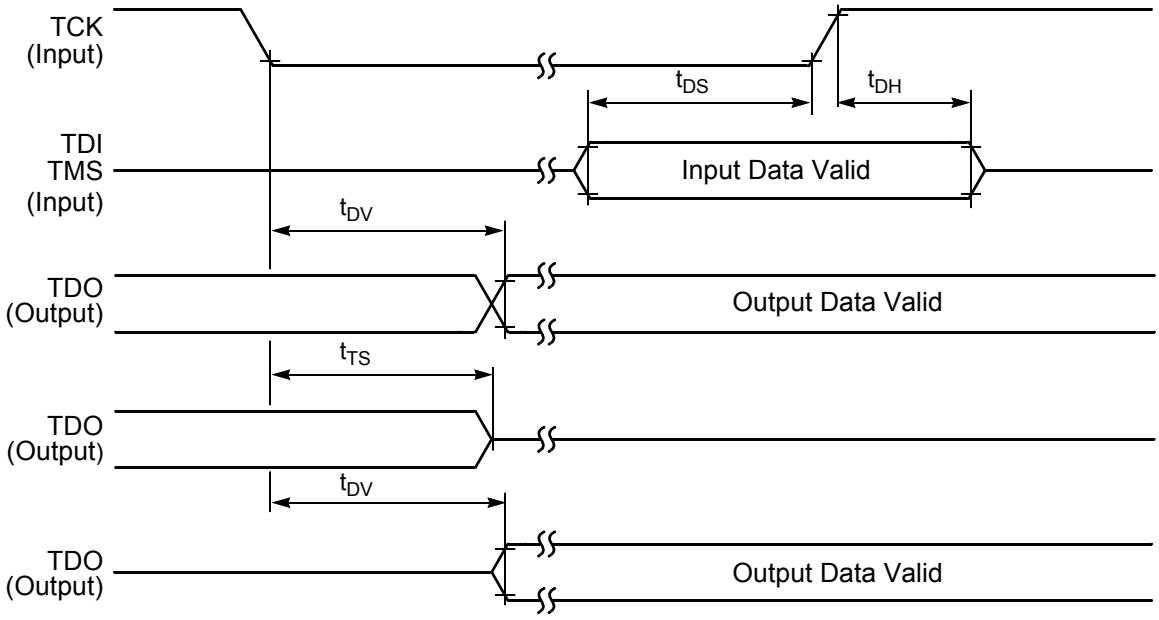


Figure 3-31 Test Access Port Timing Diagram

Figure 3-32 $\overline{\text{TRST}}$ Timing Diagram

Figure 3-33 OnCE—Debug Event

Table 4-1 56F827 Pin Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	D4	33	A10	65	V_{REFP}	97	GPIOD1
2	D5	34	A11	66	V_{REFN}	98	GPIOD0
3	D6	35	A12	67	V_{REFHI}	99	$\overline{SS}$
4	V_{DDIO}	36	A13	68	V_{REFMID}	100	MISO
5	V_{SSIO}	37	A14	69	V_{DDA_ADC}	101	MOSI
6	D7	38	A15	70	ANA0	102	SCLK
7	D8	39	EXTBOOT	71	ANA1	103	RXD2
8	D9	40	$\overline{IRQA}$	72	ANA2	104	TXD2
9	D10	41	$\overline{DE}$	73	ANA3	105	RXD1
10	D11	42	$\overline{RESET}$	74	ANA4	106	TXD1
11	D12	43	TCS	75	ANA5	107	RXD0
12	D13	44	TCK	76	ANA6	108	TXD0
13	D14	45	$\overline{TRST}$	77	ANA7	109	TA3
14	D15	46	TMS	78	ANA8	110	TA2
15	$\overline{RD}$	47	TDO	79	ANA9	111	TA1
16	$\overline{WR}$	48	TDI	80	V_{SS}	112	TA0
17	$\overline{DS}$	49	$\overline{IRQB}$	81	V_{DD}	113	V_{DDIO}
18	$\overline{PS}$	50	STCK	82	V_{DDIO}	114	V_{SSIO}
19	V_{DD}	51	STFS	83	V_{SSIO}	115	V_{SS}
20	V_{SS}	52	STD	84	PCS2	116	V_{DD}
21	A0	53	SRCK	85	PCS3	117	GPIOB7
22	A1	54	SRFS	86	PCS4	118	GPIOB6
23	A2	55	SRD	87	PCS5	119	GPIOB5
24	A3	56	V_{DDIO}	88	PCS6	120	GPIOB4
25	A4	57	CLKO	89	PCS7	121	GPIOB3
26	A5	58	V_{SSIO}	90	VPP	122	GPIOB2
27	A6	59	EXTAL	91	GPIOD7	123	GPIOB1

- Bypass the V_{DD} and V_{SS} layers of the PCB with approximately 100µF, preferably with a high-grade capacitor such as a tantalum capacitor.
- Because the controller's output signals have fast rise and fall times, PCB trace lengths should be minimal.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the VREF, V_{DDA} and V_{SSA} pins.
- When using Wired-OR mode on the SPI or the $\overline{\text{IRQx}}$ pins, the user must provide an external pull-up device.
- Designs that utilize the $\overline{\text{TRST}}$ pin for JTAG port or OnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{\text{TRST}}$ whenever $\overline{\text{RESET}}$ is asserted, as well as a means to assert $\overline{\text{TRST}}$ independently of $\overline{\text{RESET}}$. $\overline{\text{TRST}}$ must be asserted at power up for proper operation. Designs that do not require debugging functionality, such as consumer products, $\overline{\text{TRST}}$ should be tied low.
- Because the Flash memory is programmed through the JTAG/OnCE port, designers should provide an interface to this port to allow in-circuit Flash programming.

Part 6 Ordering Information

Table 6-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 6-1 56F827 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Ambient Frequency (MHz)	Order Number
56F827	2.25–2.75V	Low Profile Quad Flat Pack (LQFP)	128	80	DSP56F827FG80
56F827	2.25–2.75V	Low Profile Quad Flat Pack (LQFP)	128	80	DSP56F827FG80E *

*This package is RoHS compliant.

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