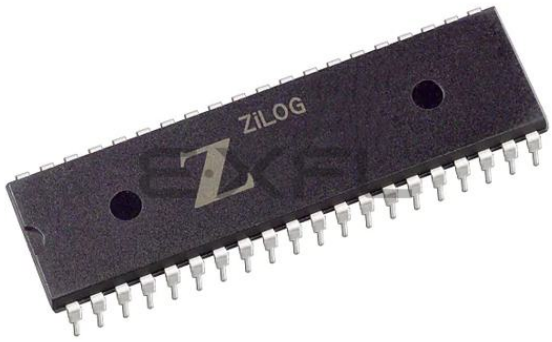


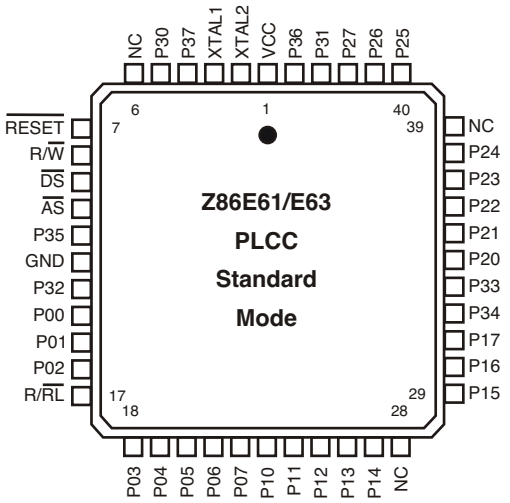
Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

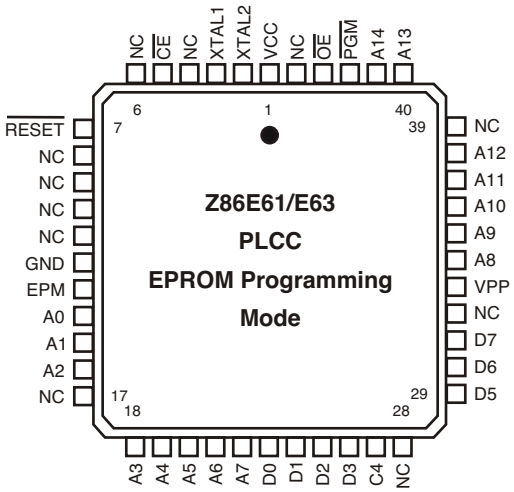
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e6116psc



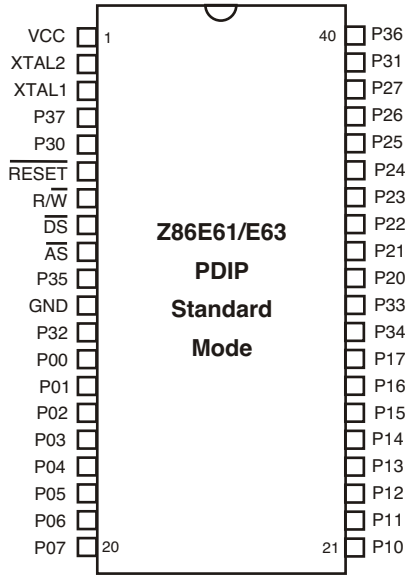
Pin Description - Standard Mode

XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{RESET}}$	Reset	Input
R/$\overline{\text{W}}$	Read/Write	Output
$\overline{\text{DS}}$	Data Strobe	Output
$\overline{\text{AS}}$	Address Strobe	Output
P00-P07 Port 0	8 bit Genaral IO	Input/Output
P10-P17 Port 1	8 bit Genaral IO	Input/Output
P20-P27 Port 2	8 bit Genaral IO	Input/Output
P30-P33 Port 3	4 bit Input	Input
P34-P37 Port 3	4 bit Output	Output
R/$\overline{\text{RL}}$	ROM/ROMless Ctrl	Input
GND	Ground	Input
VCC	Power Supply	Input



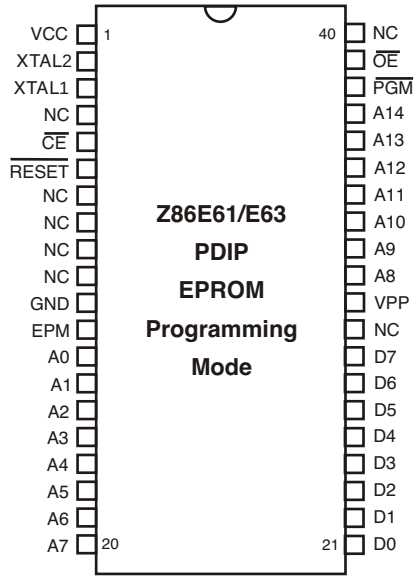
Pin Description - EPROM Programming Mode

XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{CE}}$	Chip Enable	Input
$\overline{\text{RESET}}$	Reset	Input
EPM	EPROM Prog Mode	Input
A0-A14	15-bit Address bus	Input
D7-D0	8-bit Data bus	Input/Output
VPP	Prog Voltage	Input
$\overline{\text{PGM}}$	Prog Mode	Input
$\overline{\text{OE}}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
VCC	Power Supply	Input



Pin Description - Standard Mode

XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{RESET}$	Reset	Input
R/$\overline{W}$	Read/Write	Output
$\overline{DS}$	Data Strobe	Output
$\overline{AS}$	Address Strobe	Output
P00-P07 Port 0	8 bit Genaral IO	Input/Output
P10-P17 Port 1	8 bit Genaral IO	Input/Output
P20-P27 Port 2	8 bit Genaral IO	Input/Output
P30-P33 Port 3	4 bit Input	Input
P34-P37 Port 3	4 bit Output	Output
GND	Ground	Input
VCC	Power Supply	Input



Pin Description - EPROM Programming Mode

XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
CE	Chip Enable	Input
$\overline{RESET}$	Reset	Input
$\overline{EPM}$	EPROM Prog Mode	Input
A0-A14	15-bit Address bus	Input
D7-D0	8-bit Data bus	Input/Output
VPP	Prog Voltage	Input
PGM	Prog Mode	Input
$\overline{OE}$	Output Enable	Input
$\overline{NC}$	Not Connected	Input
GND	Ground	Input
VCC	Power Supply	Input

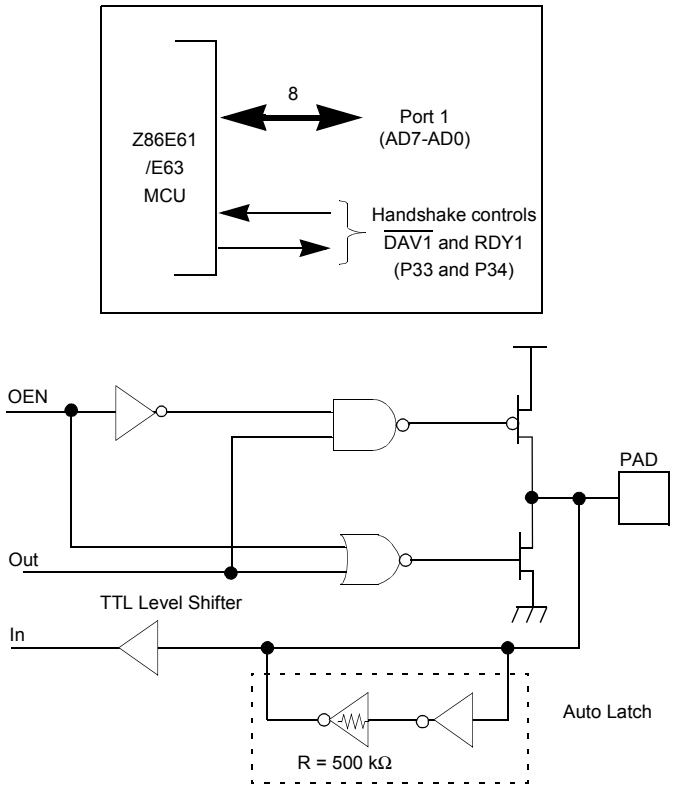


Figure 7. Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bi-directional, CM0S compatible port. Each of these eight I/0 lines can be independently programmed as an input or output, or globally as an open-drain output. Port 2 is always available for I/0 operation. When used as an I/0 port, Port 2 can be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines DAV2 and RDY2. The handshake signal assignment for Port 3 lines, P31 and P36, is dictated by the direction (input or output) assigned to P27 (Figure 8 and Table 21 on page 16).

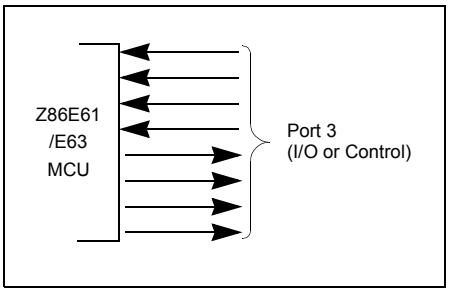


Figure 9. Port 3 Configuration

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (TIN and TOUT) Data Memory Select (/DM) and EPROM control signals (P30 = $\overline{CE}$, P31 = $\overline{OE}$, P32 = EPM and P33 = VPP).

Table 21. Port 3 Pin Assignments

Pin	I/O	CTCI	Int.	P0 HS	P1 HS	P2 HS	UART	Ext	EPROM
P30	IN	T_{IN}	IRQ3				Serial In		$\overline{CE}$
P31	IN	T_{IN}	IRQ2			D/R			$\overline{OE}$
P32	IN	T_{IN}	IRQ0	D/R					EPM
P33	IN	T_{IN}	IRQ1		D/R				V_{PP}
P34	OUT	T_{OUT}			R/D			DM	
P35	OUT	T_{OUT}		R/D					
P36	OUT	T_{OUT}				R/D			
P37	OUT	T_{OUT}					Serial Out		
T0			IRQ4						
T1			IRQ5						

1. HS = Handshake Signals D = Data Available R = Ready

UART OPERATION

Port 3 lines, P37 and P30, are programmed as serial I/0 lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/ Timer0.

The Z86E61/E63 automatically adds a start bit and two stop bits to transmitted data (Figure 10). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits, and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

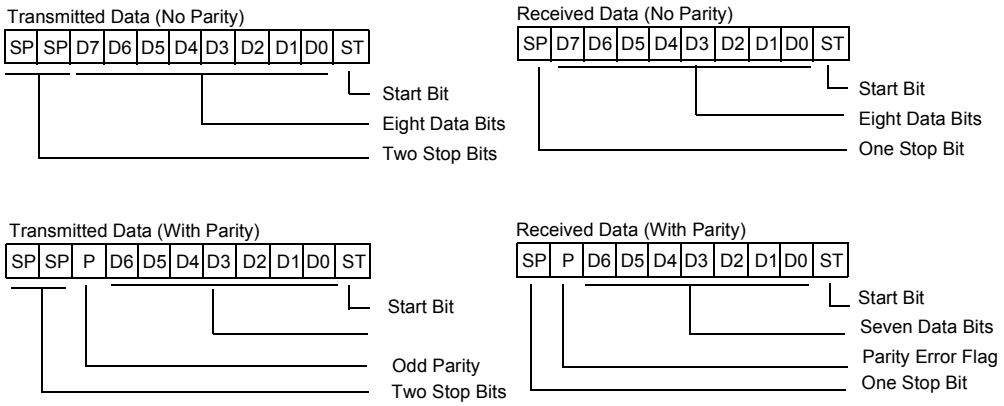


Figure 10. Serial Data Formats

Auto Latch

The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not driven by any source.

Note: P33-P30 inputs differ from the Z86C61/C63 in that there is no clamping diode to V_{CC} because of the EPROM high voltage detection circuits. Exceeding the VIH maximum specification during standard operating mode may cause the device to enter EPROM mode.

ADDRESS SPACE

Program Memory. The Z86E61/E63 can address 48 Kbytes (E61) or 32 Kbytes (E63) of external program memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 13 to byte 16383 (E61) or 32767 (E63) consists of on-chip EPROM. At addresses 16384 (E61) or 32768 (E63) and above, the Z86E61/E63 executes external program memory fetches. In ROMless mode, the Z86E61/E63 can address up to 64 Kbytes of program memory. Program execution begins at external location 000C (HEX) after a reset.

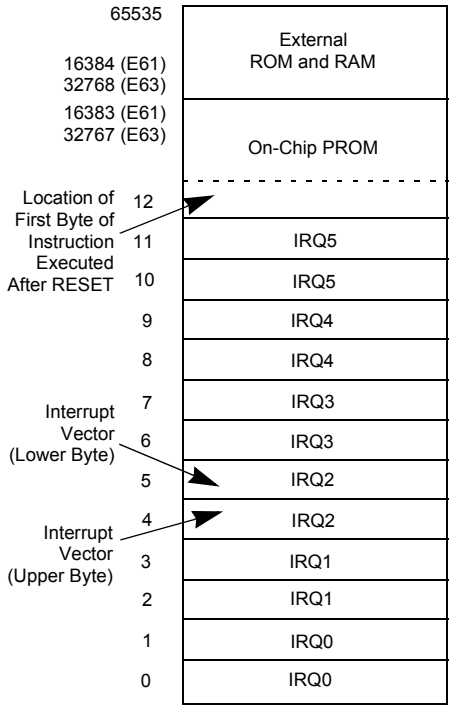


Figure 11. Program Memory Configuration

Data Memory ($\overline{DM}$)

The EPROM version can address up to 48 Kbytes (E61) or 32 Kbytes (E63) of external data memory space beginning at location 16384 (E61) or 32768 (E63). The ROMless version can address up to 64 Kbytes of external data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/0 function that can be programmed to appear on pin P34, is used to distinguish between data and program memory

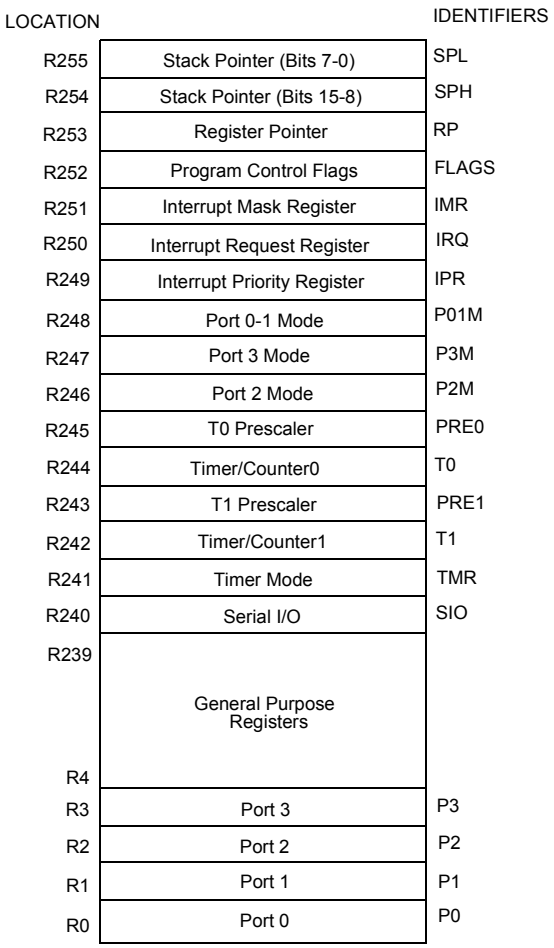


Figure 13. Register File

or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register (refer to Table 21 on page 16).

All Z86E61/E63 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initialized interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

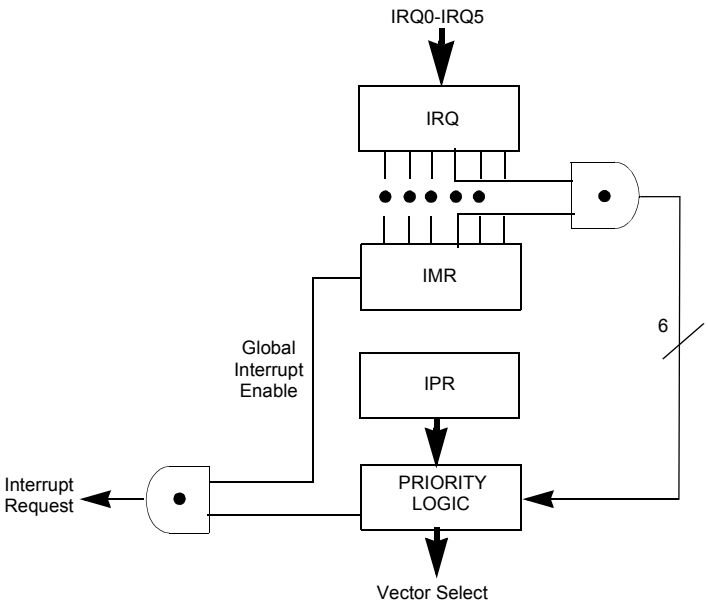


Figure 16. Interrupt Block Diagram

For the ROMless mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the inter-

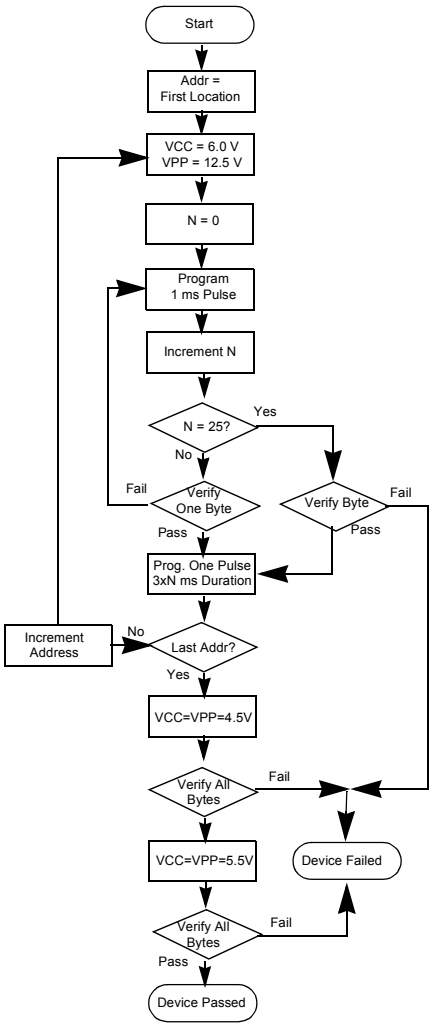


Figure 22. Intelligent Programming Flowchart

ABSOLUTE MAXIMUM RATINGS

Table 24. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage[a]	-0.3	+ 7.0	V
T_{STG}	Storage Temp	-65	+150	°C

Table 24. Absolute Maximum Ratings (Continued)

Symbol	Description	Min	Max	Units
T_A	Operating Ambient Temperature		Note[b]	°C

a. Voltages on all pins with respect to GND.
b. See See “ORDERING INFORMATION” on page 62.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 23).

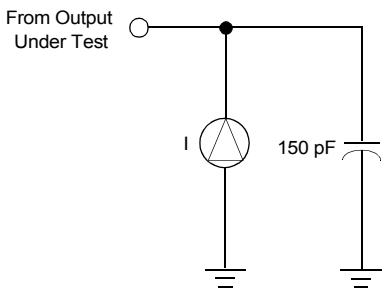


Figure 23. Test Load Diagram

DC CHARACTERISTICS

Table 25. DC Characteristics

Sym	Parameter	T_A = 0 °C to +70°C Min	Max	Typical @ 25 °C	Units	Conditions
	Max Input Voltage		7		V	I_{IN} 250 µA
	Max Input Voltage		13		V	P33-P30 Only
V_{CH}	Clock Input High Voltage	3.8	V_{CC} + 0.3		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	-0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3		V	
V_{IL}	Input Low Voltage	-0.3	0.8		V	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -2.0 mA
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = +2.0 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC} + 0.3		V	
V_{RI}	Reset Input Low Voltage	-0.3	0.8		V	
I_{IL}	Input Leakage	-10	10		µA	0 V V_{IN} + 5.25 V
I_{OL}	Output Leakage	-10	10		µA	0 V V_{IN} + 5.25 V
I_{IR}	Reset Input Current		-50		µA	V_{CC} = + 5.25 V, V_{RL} = 0 V
I_{CC}	Supply Current		50	25	mA	@ 16 MHz
			60	35	mA	@ 20 MHz
I_{CC1}	Standby Current		15	5	mA	HALT Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
			20	10	mA	HALT Mode V_{IN} = 0 V, V_{CC} @ 20 MHz
I_{CC2}[a]	Standby Current		20	5	µA	STOP Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
			20	5	µA	STOP Mode V_{IN} = 0 V, V_{CC} @ 20 MHz

a. ICC2 requires loading TMR (F1Hh) with any value prior to STOP execution.
Use this sequence:
LD TMR,#00
NOP
STOP

AC CHARACTERISTICS

Table 26. External I/O or Memory Read and Write Timing

			TA = 0°C to +70°C					
			16 MHz[a]		20 MHz			
No	Symbol	Parameter	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	20		26		ns	Note[b,c]
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	30		28		ns	Note[b,c]
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid		180		160	ns	Note[b,c,d]
4	TwAS	$\overline{AS}$ Low Width	35		36		ns	Note[b,c]
5	TdAZ(DS)	Address Float to $\overline{DS}$ Fall	0		0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	135		130		ns	Note[b,c,d]
7	TwDSW	$\overline{DS}$ (Write) Low Width	80		75		ns	Note[b,c,d]
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid		75		100	ns	Note[b,c,d]
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	0		0		ns	Note[b,c]
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	35		48		ns	Note[b,c]
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	30		36		ns	Note[b,c]
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	20		32		ns	Note[b,c]
13	TdDS(R/W)	$\overline{DS}$ Rise to R//W Not Valid	30		36		ns	Note[b,c]
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	25		40		ns	Note[b,c]
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	30		40		ns	Note[b,c]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		200		200	ns	Note[b,c,d]
17	TdAS(DS)AS	AS Rise to $\overline{DS}$ Fall Delay	40		48		ns	Note[b,c]
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Fall Delay	30		36		ns	Note[b,c]

a. All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
b. Timing numbers given are for minimum TpC.
c. See Table 11
d. When using extended memory timing add 2 TpC.

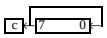
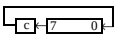
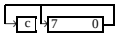
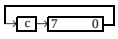
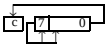
Table 27. Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40 TpC + 0.32
2	TdAS(A)	0.59 TpC - 3.25
3	TdAS(DR)	2.83 TpC + 6.14
4	TwAS	0.66 TpC - 1.65
6	TwDSR	2.33 TpC - 10.56
7	TwDSW	1.27 TpC + 1.67
8	TdDSR(DR)	1.97 TpC - 42.5
10	TdDS(A)	0.8 TpC
11	TdDS(AS)	0.59 TpC - 3.14
12	TdR/W(AS)	0.4 TpC
13	TdDS(R/$\overline{W}$)	0.8 TpC - 15
14	TdDW(DSW)	0.4 sTpC
15	TdDS(DW)	0.88 TpC - 19
16	TdA(DR)	4 TpC - 20
17	TdAS(DS)	0.91 TpC - 10.7
18	TdDM(AS)	0.9 TpC - 26.3

Table 32. Instruction Summary (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
DEC dst	R		00	-	*	*	*	-	-
dst←dst -1	IR		01						
DECW dst	RR		80	-	*	*	*	-	-
dst←dst-1	IR		81						
DI			8F	-	-	-	-	-	-
IMR(7)←0									
DJNZr, dst	RA		rA	-	-	-	-	-	-
r←r -1			r = 0-F						
if r≠0									
PC←PC + dst									
Range: +127,									
-128									
EI			9F	-	-	-	-	-	-
IMR(7)←1									
HALT			7F	-	-	-	-	-	-
INC dst	r		rE	-	*	*	*	-	-
dst←dst + 1			r = 0 - F						
	R		20						
	IR		21						
INCW dst	RR		A0	-	*	*	*	-	-
dst←dst + 1	IR		A1						
IRET			BF	*	*	*	*	*	*
FLAGS←@SP;									
SP←SP + 1									
PC←@SP;									
SP←SP + 2;									
IMR(7)←1									
JP cc, dst	DA		cD	-	-	-	-	-	-

Table 32. Instruction Summary (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
dst←dst OR src									
POP	R		50	-	-	-	-	-	-
dst←@SP;	IR		51						
SP←SP + 1									
PUSH src	R		70	-	-	-	-	-	-
SP←SP-1;	IR		71						
@SP←src									
RCF			CF	0	-	-	-	-	-
C←0									
RET			AF	-	-	-	-	-	-
PC←@SP;									
SP←SP +2									
RL dst	R		90	*	*	*	*	-	-
	IR		91						
RLC dst	R		10	*	*	*	*	-	-
	IR		11						
RR dst	R		E0	*	*	*	*	-	-
	IR		E1						
RRC dst	R		C0	*	*	*	*	-	-
	IR		C1						
SBC dst, src	Note[a]		3[ ]	*	*	*	*	1	*
dst←dst←src←C									
SCF			DF	1	-	-	-	-	-
C←1									
SRA dst	R		D0	*	*	*	0	-	-
	IR		D1						
SRP dst	Im		31	-	-	-	-	-	-

OPCODE MAP

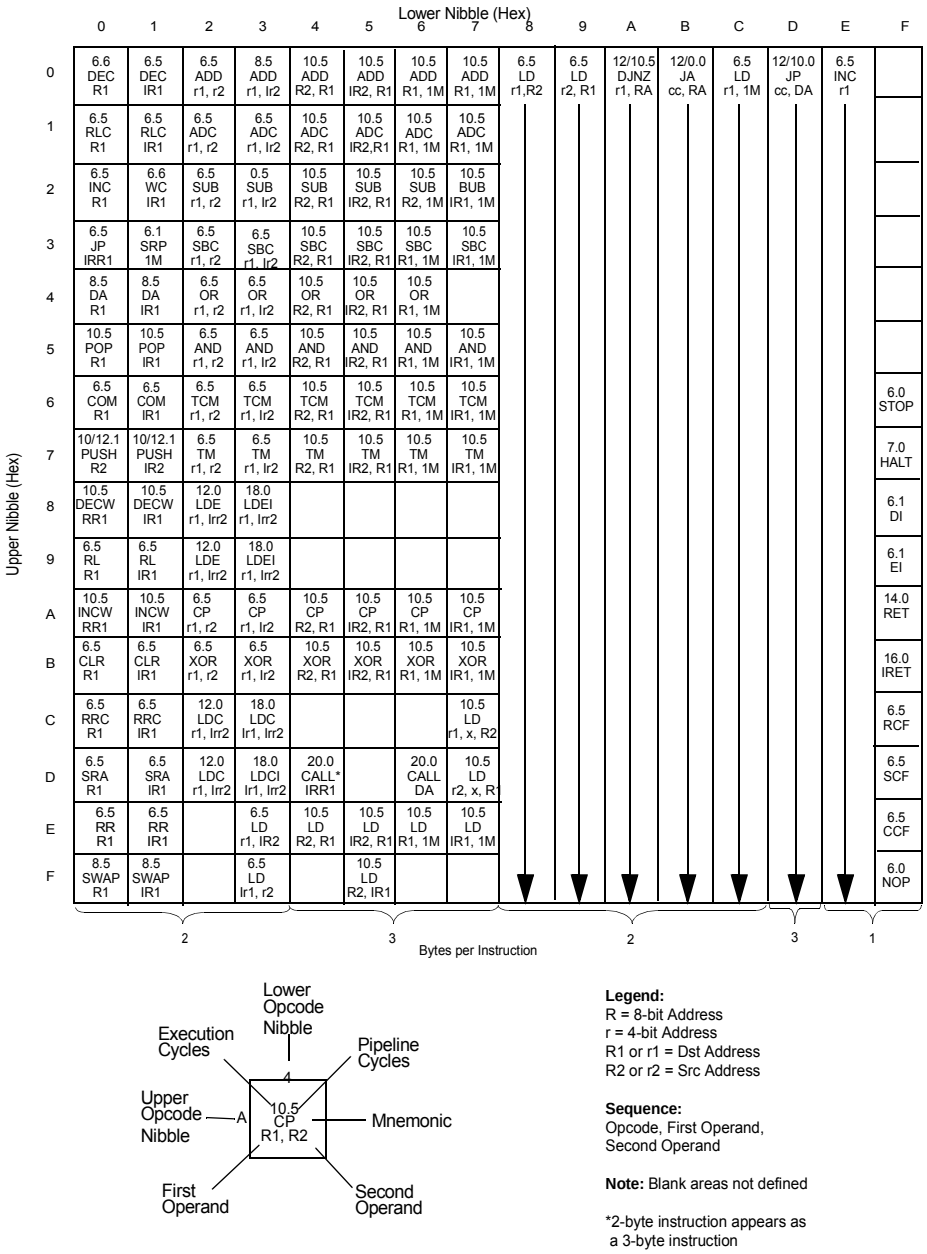
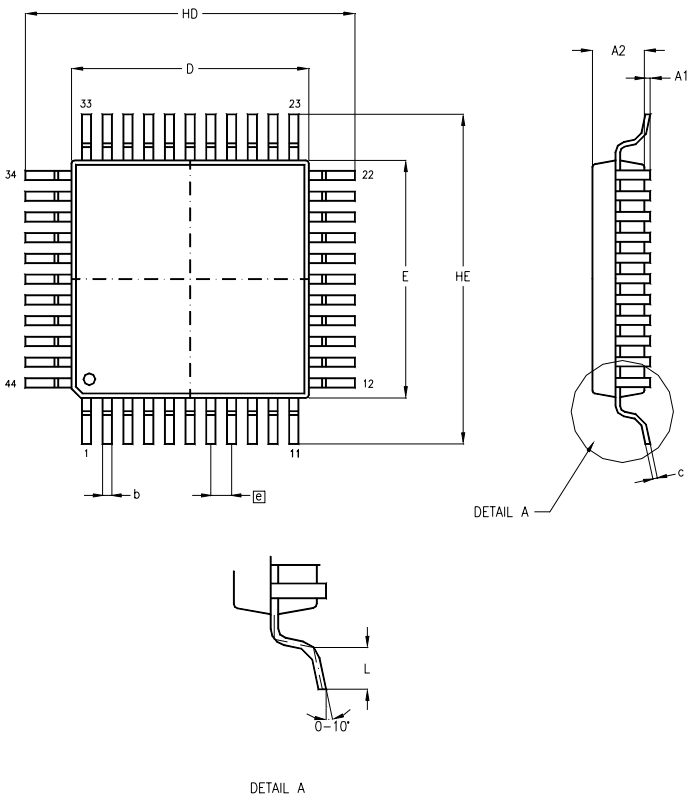


Figure 47. Opcode Map



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 BSC		.0315 BSC	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 (.004")

Figure 50. 44-Pin LQFP Package Diagram

ORDERING INFORMATION

Z86E61			
16 MHz		**20 MHz**	
40-Pin DIP	**44-Pin PLCC**	**40-Pin DIP**	**44-Pin PLCC**
Z86E6116PSC	Z86E6116VSC	Z86E6120PSC	Z86E6120VSC
Z86E63			
16 MHz		**20 MHz**	
40-Pin DIP	**44-Pin PLCC**	**40-Pin DIP**	**44-Pin PLCC**
Z86E6316PSC	Z86E6316VSC	Z86E6320PSC	Z86E6320VSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.