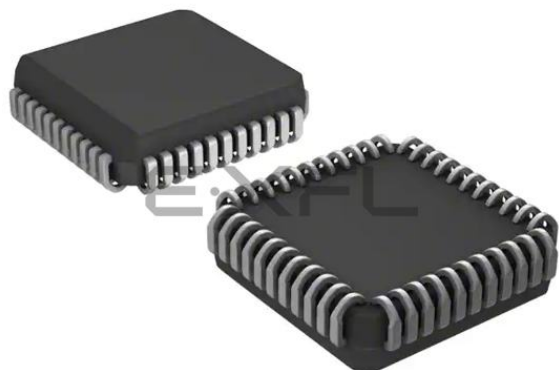




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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                             |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Obsolete                                                                                                                    |
| Core Processor             | Z8                                                                                                                          |
| Core Size                  | 8-Bit                                                                                                                       |
| Speed                      | 16MHz                                                                                                                       |
| Connectivity               | UART/USART                                                                                                                  |
| Peripherals                | -                                                                                                                           |
| Number of I/O              | 32                                                                                                                          |
| Program Memory Size        | 16KB (16K x 8)                                                                                                              |
| Program Memory Type        | OTP                                                                                                                         |
| EEPROM Size                | -                                                                                                                           |
| RAM Size                   | 236 x 8                                                                                                                     |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V                                                                                                                 |
| Data Converters            | -                                                                                                                           |
| Oscillator Type            | Internal                                                                                                                    |
| Operating Temperature      | 0°C ~ 70°C (TA)                                                                                                             |
| Mounting Type              | Surface Mount                                                                                                               |
| Package / Case             | 44-LCC (J-Lead)                                                                                                             |
| Supplier Device Package    | -                                                                                                                           |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/zilog/z86e6116vsc">https://www.e-xfl.com/product-detail/zilog/z86e6116vsc</a> |





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## GENERAL DESCRIPTION

The Z86E61/E63 microcontrollers are members of the Z8® single-chip microcontroller family with 16K/32 Kbytes of EPROM and 236 bytes of general-purpose RAM. Offered in 40-pin DIP, 44-pin PLCC or 44-Pin LQFP package styles, these devices are pin-compatible EPROM versions of the Z86C61/ 63. The ROMless pin option is available on the 44-pin versions only.

With 4 Kbytes of ROM and 236 bytes of general-purpose RAM, the Z86E61/E63 offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

For applications demanding powerful I/O capabilities, the Z86E61/E63 offers 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

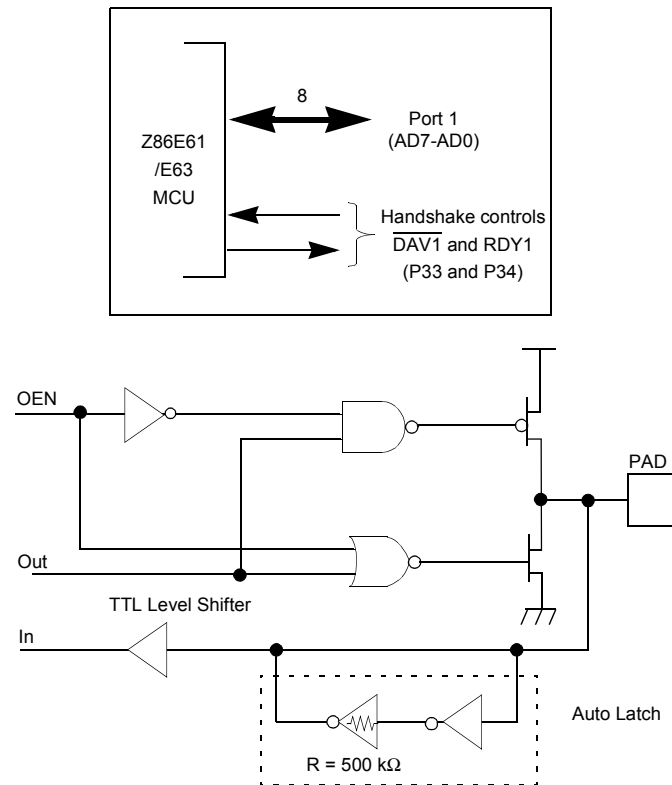
The Z86E61/E63 can address both external memory and preprogrammed ROM, making it well suited for high-volume applications or where code flexibility is required. There are three basic address spaces available to support this configuration: Program Memory, Data Memory, and 236 general-purpose registers.

To unburden the system from coping with real-time tasks such as counting/timing and serial data communication, the Z86E61/E63 offers two on-chip counter/timers with a large number of user selectable modes (Figure 1).

Power connections follow conventional descriptions below:

| Connection | Circuit         | Device          |
|------------|-----------------|-----------------|
| Power      | V <sub>CC</sub> | V <sub>DD</sub> |
| Ground     | GND             | V <sub>SS</sub> |



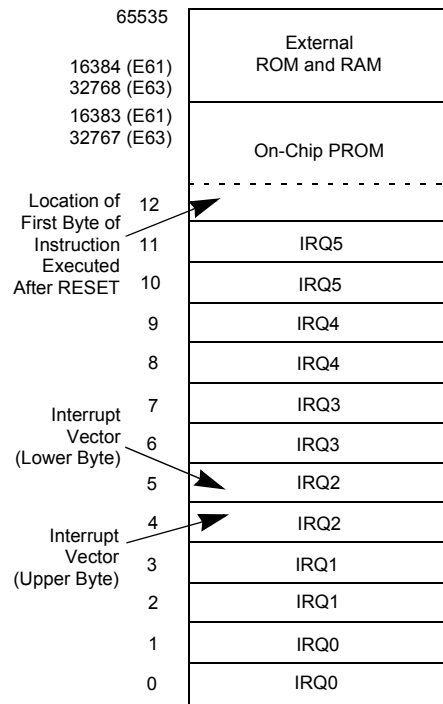


**Figure 7. Port 1 Configuration**

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bi-directional, CMOS compatible port. Each of these eight I/O lines can be independently programmed as an input or output, or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 can be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines  $\overline{\text{DAV2}}$  and RDY2. The handshake signal assignment for Port 3 lines, P31 and P36, is dictated by the direction (input or output) assigned to P27 (Figure 8 and Table 21 on page 16).

## ADDRESS SPACE

**Program Memory.** The Z86E61/E63 can address 48 Kbytes (E61) or 32 Kbytes (E63) of external program memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 13 to byte 16383 (E61) or 32767 (E63) consists of on-chip EPROM. At addresses 16384 (E61) or 32768 (E63) and above, the Z86E61/E63 executes external program memory fetches. In ROMless mode, the Z86E61/E63 can address up to 64 Kbytes of program memory. Program execution begins at external location 000C (HEX) after a reset.



**Figure 11. Program Memory Configuration**

## Data Memory ( $\overline{DM}$ )

The EPROM version can address up to 48 Kbytes (E61) or 32 Kbytes (E63) of external data memory space beginning at location 16384 (E61) or 32768 (E63). The ROMless version can address up to 64 Kbytes of external data memory. External data memory may be included with, or separated from, the external program memory space.  $\overline{DM}$ , an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory

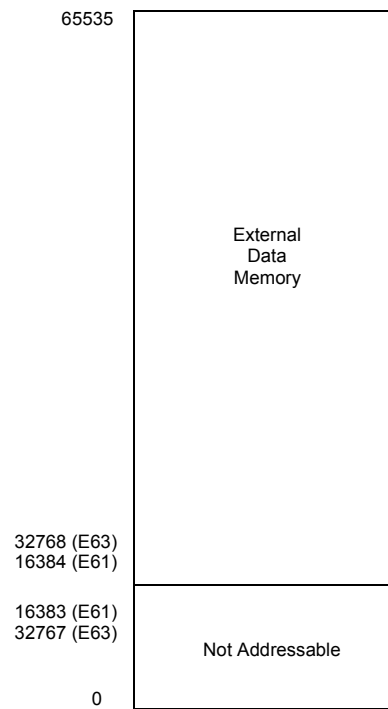


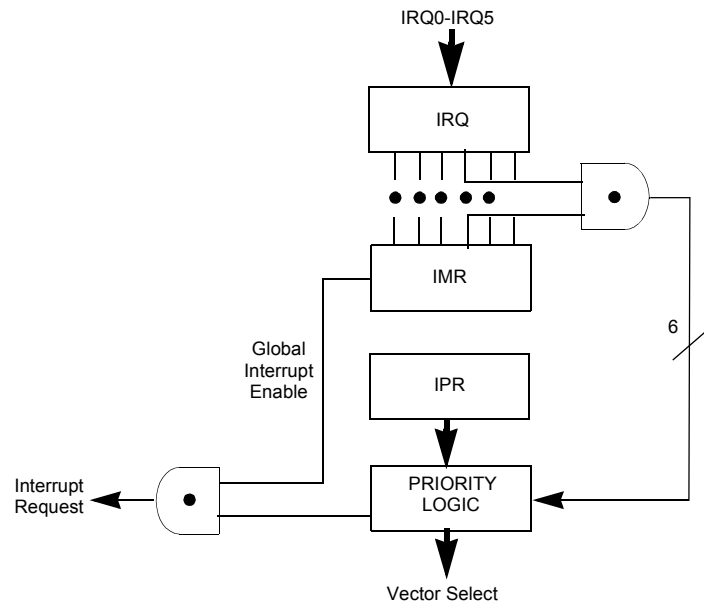
Figure 12. Data Memory Configuration

or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register (refer to Table 21 on page 16).

All Z86E61/E63 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initialized interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.



**Figure 16. Interrupt Block Diagram**

For the ROMless mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the inter-



## XCLK

A clock is required to clock the  $\overline{\text{RESET}}$  signal into the registers before programming.

A constant clock can be applied, or the XCLK input can be toggled a minimum of 12 cycles before any programming or verify function begins. The maximum clock frequency to be applied when in the EPROM mode is 12 MHz.

## $\overline{\text{RESET}}$

The reset input can be held to a constant Low or High value throughout normal programming. It must be held High to program the EPROM protect option bit. Also, any time the  $\overline{\text{RESET}}$  input changes state the XCLK must be clocked a minimum of 12 times to clock the  $\overline{\text{RESET}}$  through the reset filter.

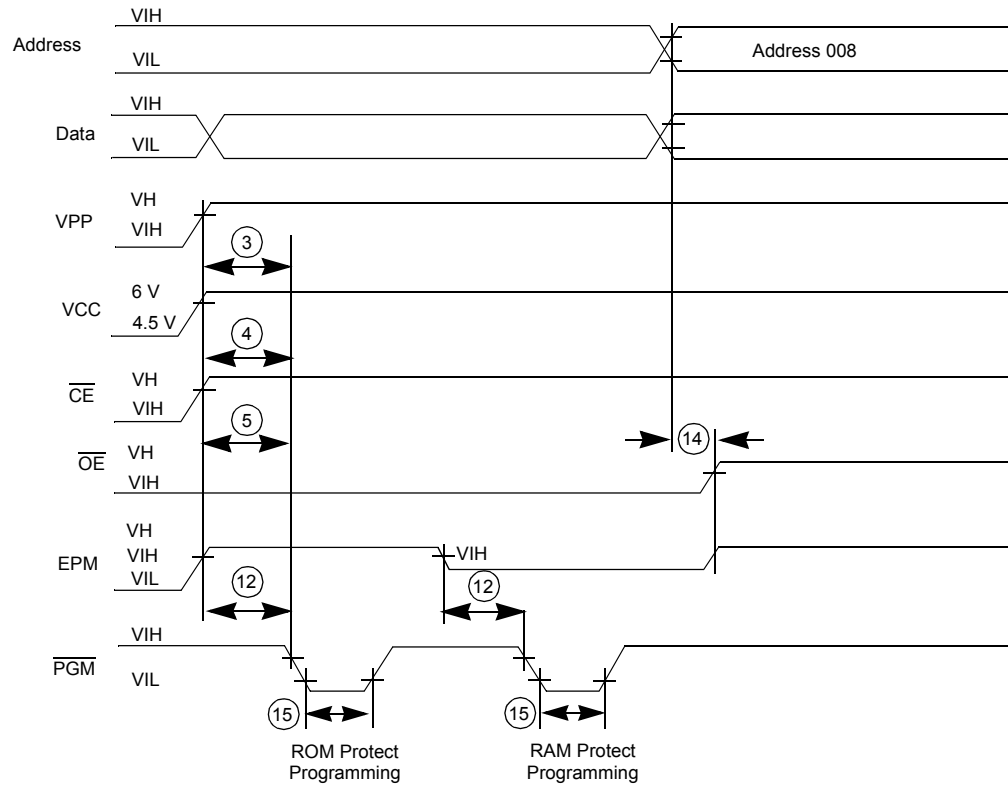
## $\overline{\text{OE}}$

When the device is placed in EPROM mode, the  $\overline{\text{OE}}$  input also serves as the precharge for the sense amp. The precharge signal should be Low for the first half of the stable address and High for the second half. The PRECHG signal is inverted from the  $\overline{\text{OE}}$  signal so the  $\overline{\text{OE}}$  should be High on the first half and Low on the second half, or stable address. The EPROM output data should be sampled during the second half of stable address.

The access time of the EPROM is defined in later sections. This two part calculation of access time is required because this is a precharged sense amp with a precharge clock.

**Table 23. Timing of Programming Waveforms**

| Parameters | Name                              | Min  | Max | Units         |
|------------|-----------------------------------|------|-----|---------------|
| 1          | Address Setup Time                | 2    |     | $\mu\text{s}$ |
| 2          | Data Setup Time                   | 2    |     | $\mu\text{s}$ |
| 3          | $V_{PP}$ Setup                    | 2    |     | $\mu\text{s}$ |
| 4          | $V_{CC}$ Setup Time               | 2    |     | $\mu\text{s}$ |
| 5          | Chip Enable Setup Time            | 2    |     | $\mu\text{s}$ |
| 6          | Program Pulse Width               | 0.95 |     | ms            |
| 7          | Data Hold Time                    | 2    |     | $\mu\text{s}$ |
| 8          | $\overline{\text{OE}}$ Setup Time | 2    |     | $\mu\text{s}$ |
| 9          | Data Access Time                  |      | 200 | ns            |
| 10         | Data Output Float Time            |      | 100 | ns            |



**Figure 21. Programming EPROM, RAM Protect, and 16K Size Selection**

## DC CHARACTERISTICS

Table 25. DC Characteristics

| Sym                           | Parameter                | T <sub>A</sub> = 0 °C to +70°C |                       | Typical<br>@ 25 °C | Units | Conditions                                                |
|-------------------------------|--------------------------|--------------------------------|-----------------------|--------------------|-------|-----------------------------------------------------------|
|                               |                          | Min                            | Max                   |                    |       |                                                           |
|                               | Max Input Voltage        |                                | 7                     |                    | V     | I <sub>IN</sub> 250 µA                                    |
|                               | Max Input Voltage        |                                | 13                    |                    | V     | P33-P30 Only                                              |
| V <sub>CH</sub>               | Clock Input High Voltage | 3.8                            | V <sub>CC</sub> + 0.3 |                    | V     | Driven by External Clock Generator                        |
| V <sub>CL</sub>               | Clock Input Low Voltage  | -0.3                           | 0.8                   |                    | V     | Driven by External Clock Generator                        |
| V <sub>IH</sub>               | Input High Voltage       | 2.0                            | V <sub>CC</sub> + 0.3 |                    | V     |                                                           |
| V <sub>IL</sub>               | Input Low Voltage        | -0.3                           | 0.8                   |                    | V     |                                                           |
| V <sub>OH</sub>               | Output High Voltage      | 2.4                            |                       |                    | V     | I <sub>OH</sub> = -2.0 mA                                 |
| V <sub>OL</sub>               | Output Low Voltage       |                                | 0.4                   |                    | V     | I <sub>OL</sub> = +2.0 mA                                 |
| V <sub>RH</sub>               | Reset Input High Voltage | 3.8                            | V <sub>CC</sub> + 0.3 |                    | V     |                                                           |
| V <sub>RI</sub>               | Reset Input Low Voltage  | -0.3                           | 0.8                   |                    | V     |                                                           |
| I <sub>IL</sub>               | Input Leakage            | -10                            | 10                    |                    | µA    | 0 V V <sub>IN</sub> + 5.25 V                              |
| I <sub>OL</sub>               | Output Leakage           | -10                            | 10                    |                    | µA    | 0 V V <sub>IN</sub> + 5.25 V                              |
| I <sub>IR</sub>               | Reset Input Current      |                                | -50                   |                    | µA    | V <sub>CC</sub> = + 5.25 V, V <sub>RL</sub> = 0 V         |
| I <sub>CC</sub>               | Supply Current           |                                | 50                    | 25                 | mA    | @ 16 MHz                                                  |
|                               |                          |                                | 60                    | 35                 | mA    | @ 20 MHz                                                  |
| I <sub>CC1</sub>              | Standby Current          |                                | 15                    | 5                  | mA    | HALT Mode V <sub>IN</sub> = 0 V, V <sub>CC</sub> @ 16 MHz |
|                               |                          |                                | 20                    | 10                 | mA    | HALT Mode V <sub>IN</sub> = 0 V, V <sub>CC</sub> @ 20 MHz |
| I <sub>CC2</sub> <sup>a</sup> | Standby Current          |                                | 20                    | 5                  | µA    | STOP Mode V <sub>IN</sub> = 0 V, V <sub>CC</sub> @ 16 MHz |
|                               |                          |                                | 20                    | 5                  | µA    | STOP Mode V <sub>IN</sub> = 0 V, V <sub>CC</sub> @ 20 MHz |

- a. ICC2 requires loading TMR (F1Hh) with any value prior to STOP execution.  
Use this sequence:  
LD TMR,#00  
NOP  
STOP

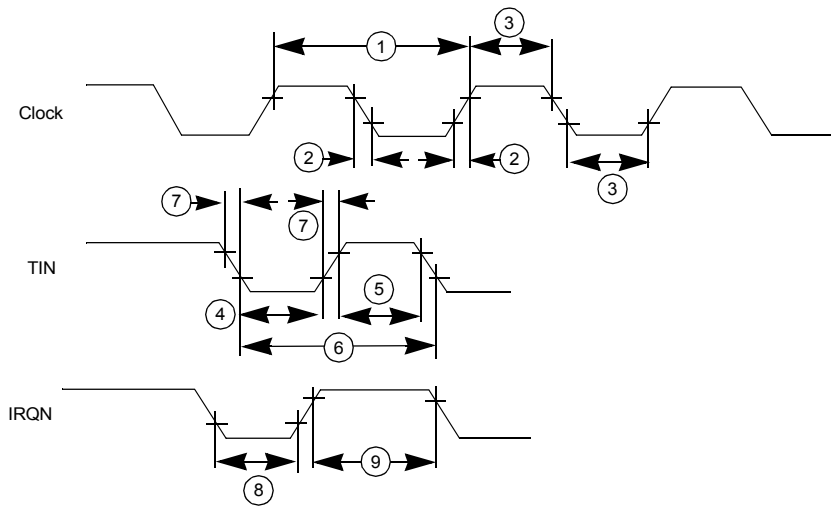


Figure 25. Additional Timing



## AC CHARACTERISTICS

Table 28. Additional Timing

|    |             |                                    | TA = 0°C to +70°C |      |        |      |       |                     |
|----|-------------|------------------------------------|-------------------|------|--------|------|-------|---------------------|
|    |             |                                    | 16 MHz            |      | 20 MHz |      |       |                     |
|    |             |                                    | Min               | Max  | Min    | Max  |       |                     |
| No | Symbol      | Parameter                          | Min               | Max  | Min    | Max  | Units | Notes               |
| 1  | TpC         | Input Clock Period                 | 62.5              | 1000 | 50     | 1000 | ns    | Note <sup>a</sup>   |
| 2  | TrC,TfC     | Clock Input Rise & Fall Times      |                   | 10   |        | 15   | ns    | Note <sup>a</sup>   |
| 3  | TwC         | Input Clock Width                  | 21                |      | 37     |      | ns    | Note <sup>a</sup>   |
| 4  | TwTinL      | Timer Input Low Width              | 50                |      | 75     |      | ns    | Note <sup>b</sup>   |
| 5  | TwTinH      | Timer Input High Width             | 5TpC              |      | 5TpC   |      |       | Note <sup>b</sup>   |
| 6  | TpTin       | Timer Input Period                 | 8TpC              |      | 8TpC   |      |       | Note <sup>b</sup>   |
| 7  | TrTin,TfTin | Timer Input Rise & Fall Times      | 100               |      | 100    |      | ns    | Note <sup>b</sup>   |
| 8A | TwIL        | Interrupt Request Input Low Times  | 70                |      | 50     |      | ns    | Note <sup>b,c</sup> |
| 8B | TwIL        | Interrupt Request Input Low Times  | 5TpC              |      | 5TpC   |      |       | Note <sup>b,d</sup> |
| 9  | TwIH        | Interrupt Request Input High Times | 5TpC              |      | 5TpC   |      |       | Note <sup>b,e</sup> |

- a. Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
- b. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
- c. Interrupt request through Port 3 (P33-P31).
- d. Interrupt request through Port 30.
- e. Interrupt references request through Port 3.

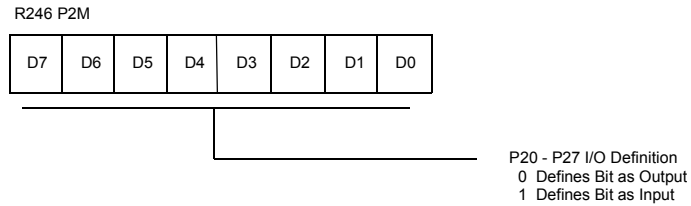


Figure 34. Port 2 Mode Register (F6<sub>H</sub>: Write Only)

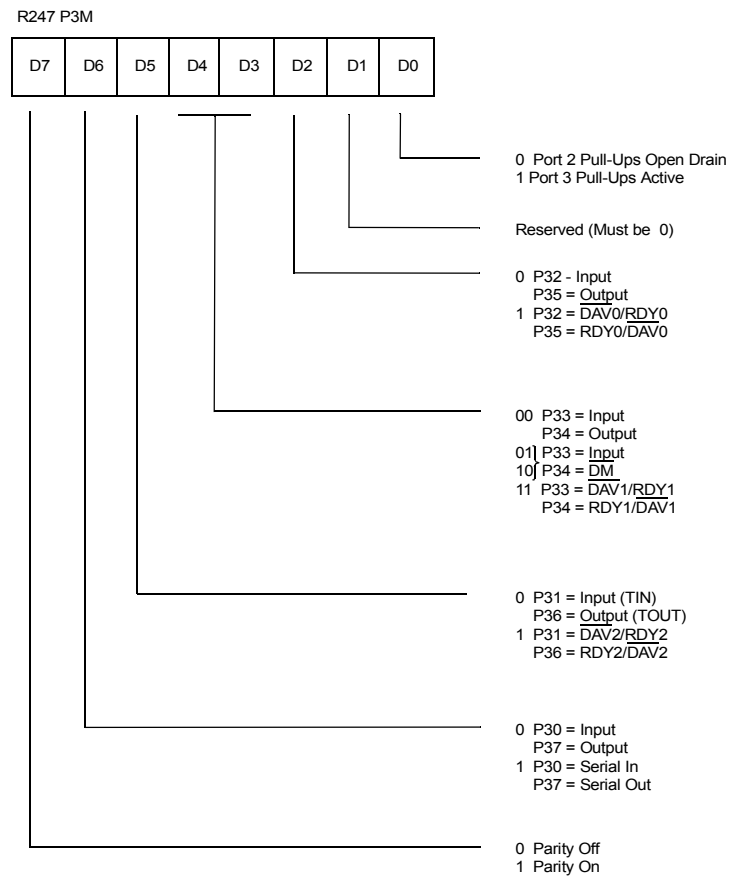


Figure 35. Port 3 Mode Register (F7<sub>H</sub>: Write Only)

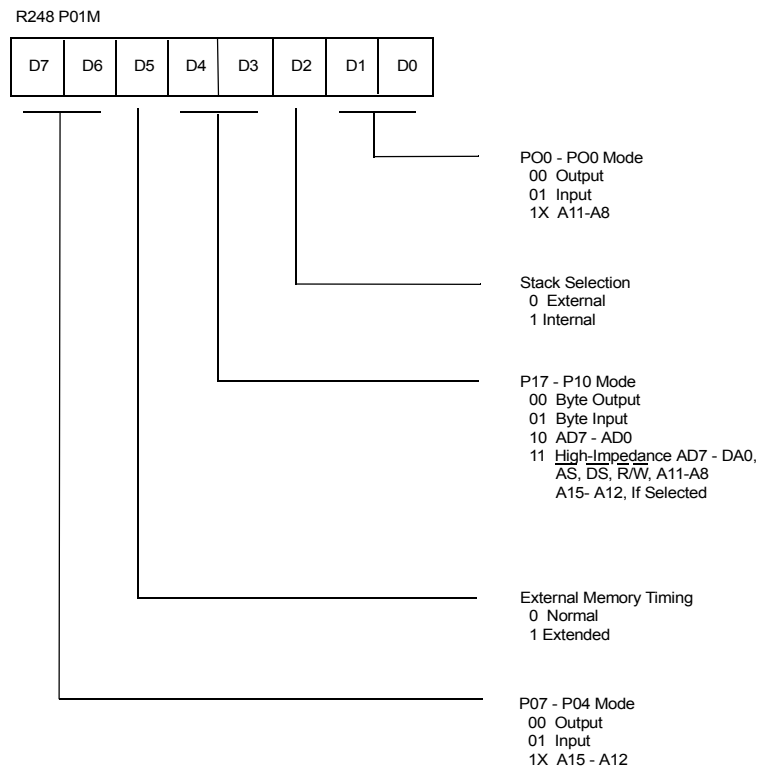


Figure 36. Port 0 and 1 Mode Register (F8<sub>H</sub>: Write Only)

## DC CHARACTERISTICS

### Supply Current

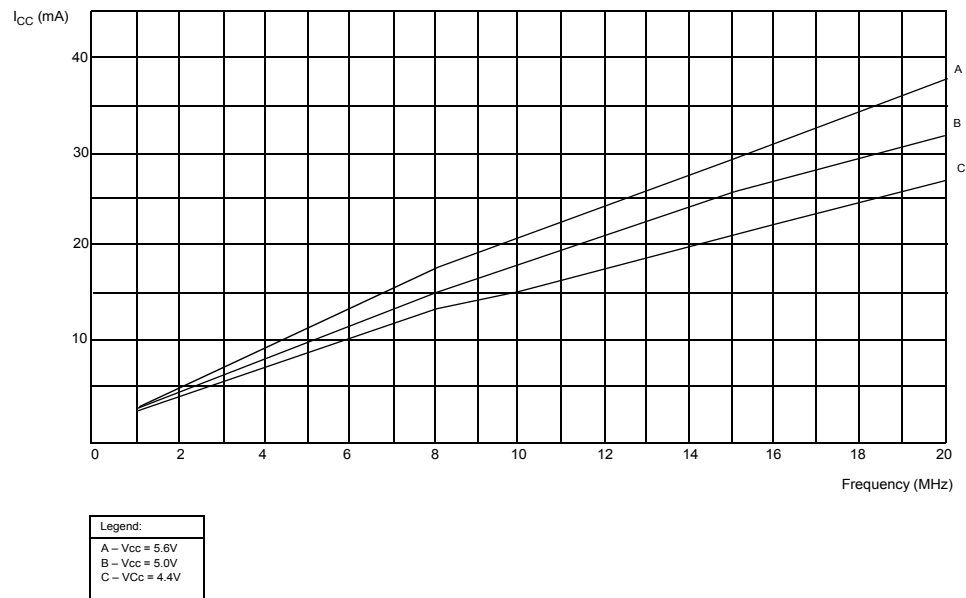


Figure 44. Typical  $I_{CC}$  vs. Frequency

**Flags.** Control register (R252) contains the following six flags:

| Symbol | Meaning             |
|--------|---------------------|
| C      | Carry flag          |
| Z      | Zero flag           |
| S      | Sign flag           |
| V      | Overflow flag       |
| D      | Decimal-adjust flag |
| H      | Half-carry flag     |

Affected flags are indicated by:

| Symbol | Meaning                             |
|--------|-------------------------------------|
| 0      | Clear to zero                       |
| 1      | Set to one                          |
| *      | Set to clear according to operation |
| -      | Unaffected                          |
| x      | Undefined                           |

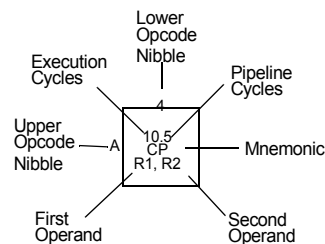
## CONDITION CODES

**Table 31. Condition Codes**

| Value | Mnemonic | Meaning               | Flags Set     |
|-------|----------|-----------------------|---------------|
| 1000  |          | Always True           |               |
| 0111  | C        | Carry                 | C = 1         |
| 1111  | NC       | No Carry              | C = 0         |
| 0110  | Z        | Zero                  | Z = 1         |
| 1110  | NZ       | Not Zero              | Z = 0         |
| 1101  | PL       | Plus                  | S = 0         |
| 0101  | MI       | Minus                 | S = 1         |
| 0100  | OV       | Overflow              | V = 1         |
| 1100  | NOV      | No Overflow           | V = 0         |
| 0110  | EQ       | Equal                 | Z = 1         |
| 1110  | NE       | Not Equal             | Z = 0         |
| 1001  | GE       | Greater Than or Equal | (S XOR V) = 0 |

## OPCODE MAP

| Upper Nibble (Hex) | Lower Nibble (Hex) |                  |                  |                    |                 |                  |                 |                   |               |                       |                     |                 |               |                 |            |           |
|--------------------|--------------------|------------------|------------------|--------------------|-----------------|------------------|-----------------|-------------------|---------------|-----------------------|---------------------|-----------------|---------------|-----------------|------------|-----------|
|                    | 0                  | 1                | 2                | 3                  | 4               | 5                | 6               | 7                 | 8             | 9                     | A                   | B               | C             | D               | E          | F         |
| 0                  | 6.6 DEC R1         | 6.5 DEC IR1      | 6.5 ADD r1, r2   | 8.5 ADD r1, Ir2    | 10.5 ADD R2, R1 | 10.5 ADD IR2, R1 | 10.5 ADD R1, 1M | 10.5 ADD R1, 1M   | 6.5 LD r1, R2 | 6.5 LD r2, R1         | 12/10.5 DJNZ r1, RA | 12/0.0 JACC, RA | 6.5 LD r1, 1M | 12/10.0 JPC, DA | 6.5 INC r1 |           |
| 1                  | 6.5 RLC R1         | 6.5 RLC IR1      | 6.5 ADC r1, r2   | 6.5 ADC r1, Ir2    | 10.5 ADC R2, R1 | 10.5 ADC IR2, R1 | 10.5 ADC R1, 1M | 10.5 ADC R1, 1M   |               |                       |                     |                 |               |                 |            |           |
| 2                  | 6.5 INC R1         | 6.6 WC IR1       | 6.5 SUB r1, r2   | 0.5 SUB r1, Ir2    | 10.5 SUB R2, R1 | 10.5 SUB IR2, R1 | 10.5 SUB R2, 1M | 10.5 SUB IR1, 1M  |               |                       |                     |                 |               |                 |            |           |
| 3                  | 6.5 JP IRR1        | 6.1 SRP 1M       | 6.5 SBC r1, r2   | 6.5 SBC r1, Ir2    | 10.5 SBC R2, R1 | 10.5 SBC IR2, R1 | 10.5 SBC R1, 1M | 10.5 SBC IR1, 1M  |               |                       |                     |                 |               |                 |            |           |
| 4                  | 8.5 DA R1          | 8.5 DA IR1       | 6.5 OR r1, r2    | 6.5 OR r1, Ir2     | 10.5 OR R2, R1  | 10.5 OR IR2, R1  | 10.5 OR R1, 1M  |                   |               |                       |                     |                 |               |                 |            |           |
| 5                  | 10.5 POP R1        | 10.5 POP IR1     | 6.5 AND r1, r2   | 6.5 AND r1, Ir2    | 10.5 AND R2, R1 | 10.5 AND IR2, R1 | 10.5 AND R1, 1M | 10.5 AND IR1, 1M  |               |                       |                     |                 |               |                 |            |           |
| 6                  | 6.5 COM R1         | 6.5 COM IR1      | 6.5 TCM r1, r2   | 6.5 TCM r1, Ir2    | 10.5 TCM R2, R1 | 10.5 TCM IR2, R1 | 10.5 TCM R1, 1M | 10.5 TCM IR1, 1M  |               |                       |                     |                 |               |                 |            | 6.0 STOP  |
| 7                  | 10/12.1 PUSH R2    | 10/12.1 PUSH IR2 | 6.5 TM r1, r2    | 6.5 TM r1, Ir2     | 10.5 TM R2, R1  | 10.5 TM IR2, R1  | 10.5 TM R1, 1M  | 10.5 TM IR1, 1M   |               |                       |                     |                 |               |                 |            | 7.0 HALT  |
| 8                  | 10.5 DECW RR1      | 10.5 DECW IR1    | 12.0 LDE r1, r2  | 18.0 LDEI r1, Ir2  |                 |                  |                 |                   |               |                       |                     |                 |               |                 |            | 6.1 DI    |
| 9                  | 6.5 RL R1          | 6.5 RL IR1       | 12.0 LDE r1, Ir2 | 18.0 LDEI r1, Ir2  |                 |                  |                 |                   |               |                       |                     |                 |               |                 |            | 6.1 EI    |
| A                  | 10.5 INCW RR1      | 10.5 INCW IR1    | 6.5 CP r1, r2    | 6.5 CP r1, Ir2     | 10.5 CP R2, R1  | 10.5 CP IR2, R1  | 10.5 CP R1, 1M  | 10.5 CP IR1, 1M   |               |                       |                     |                 |               |                 |            | 14.0 RET  |
| B                  | 6.5 CLR R1         | 6.5 CLR IR1      | 6.5 XOR r1, r2   | 6.5 XOR r1, Ir2    | 10.5 XOR R2, R1 | 10.5 XOR IR2, R1 | 10.5 XOR R1, 1M | 10.5 XOR IR1, 1M  |               |                       |                     |                 |               |                 |            | 16.0 IRET |
| C                  | 6.5 RRC R1         | 6.5 RRC IR1      | 12.0 LDC r1, r2  | 18.0 LDC Ir1, Ir2  |                 |                  |                 | 10.5 LD r1, x, R2 |               |                       |                     |                 |               |                 |            | 6.5 RCF   |
| D                  | 6.5 SRA R1         | 6.5 SRA IR1      | 12.0 LDC r1, Ir2 | 18.0 LDCI Ir1, Ir2 | 20.0 CALL* IRR1 |                  | 20.0 CALL DA    | 10.5 LD r2, x, R  |               |                       |                     |                 |               |                 |            | 6.5 SCF   |
| E                  | 6.5 RR R1          | 6.5 RR IR1       |                  | 6.5 LD r1, R2      | 10.5 LD R2, R1  | 10.5 LD IR2, R1  | 10.5 LD R1, 1M  | 10.5 LD IR1, 1M   |               |                       |                     |                 |               |                 |            | 6.5 CCF   |
| F                  | 8.5 SWAP R1        | 8.5 SWAP IR1     |                  | 6.5 LD Ir1, r2     |                 | 10.5 LD R2, IR1  |                 |                   |               |                       |                     |                 |               |                 |            | 6.0 NOP   |
|                    |                    |                  |                  |                    |                 |                  |                 |                   |               | 2                     | 2                   | 2               | 2             | 3               | 1          |           |
|                    |                    |                  |                  |                    |                 |                  |                 |                   |               | Bytes per Instruction |                     |                 |               |                 |            |           |



### Legend:

R = 8-bit Address  
r = 4-bit Address  
R1 or r1 = Dst Address  
R2 or r2 = Src Address

### Sequence:

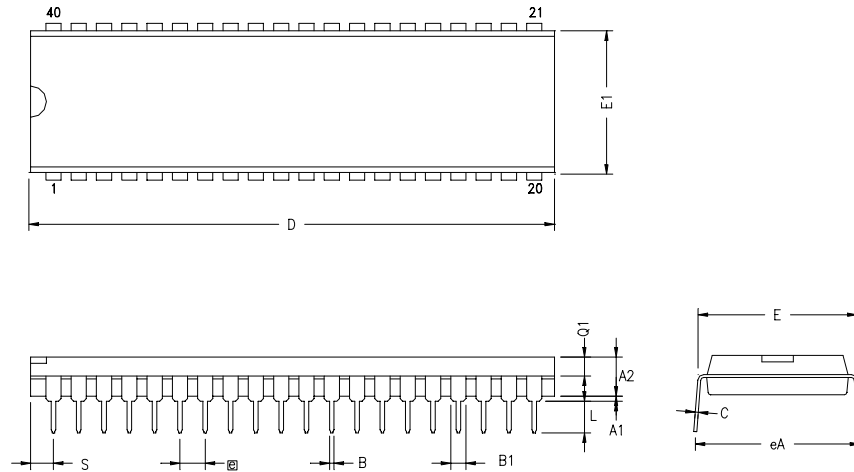
Opcode, First Operand,  
Second Operand

**Note:** Blank areas not defined

\*2-byte instruction appears as  
a 3-byte instruction

Figure 47. Opcode Map

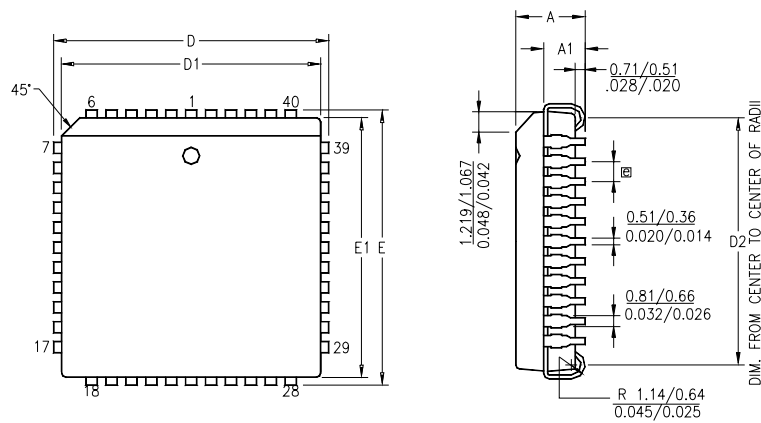
## PACKAGE INFORMATION



| SYMBOL | MILLIMETER |       | INCH     |       |
|--------|------------|-------|----------|-------|
|        | MIN        | MAX   | MIN      | MAX   |
| A1     | 0.51       | 1.02  | .020     | .040  |
| A2     | 3.18       | 3.94  | .125     | .155  |
| B      | 0.38       | 0.53  | .015     | .021  |
| B1     | 1.02       | 1.52  | .040     | .060  |
| C      | 0.23       | 0.38  | .009     | .015  |
| D      | 52.07      | 52.58 | 2.050    | 2.070 |
| E      | 15.24      | 15.75 | .600     | .620  |
| E1     | 13.59      | 14.22 | .535     | .560  |
| □      | 2.54 TYP   |       | .100 TYP |       |
| eA     | 15.49      | 16.76 | .610     | .660  |
| L      | 3.05       | 3.81  | .120     | .150  |
| Q1     | 1.40       | 1.91  | .055     | .075  |
| S      | 1.52       | 2.29  | .060     | .090  |

CONTROLLING DIMENSIONS : INCH

Figure 48. 40-Pin DIP Package Diagram



| SYMBOL | MILLIMETER |       | INCH      |       |
|--------|------------|-------|-----------|-------|
|        | MIN        | MAX   | MIN       | MAX   |
| A      | 4.27       | 4.57  | 0.168     | 0.180 |
| A1     | 2.41       | 2.92  | 0.095     | 0.115 |
| D/E    | 17.40      | 17.65 | 0.685     | 0.695 |
| D1/E1  | 16.51      | 16.66 | 0.650     | 0.656 |
| D2     | 15.24      | 16.00 | 0.600     | 0.630 |
| □      | 1.27 BSC   |       | 0.050 BSC |       |

- NOTES:  
1. CONTROLLING DIMENSION : INCH  
2. LEADS ARE COPLANAR WITHIN 0.004".  
3. DIMENSION :  $\frac{MM}{INCH}$

Figure 49. 44-Pin PLCC Package Diagram