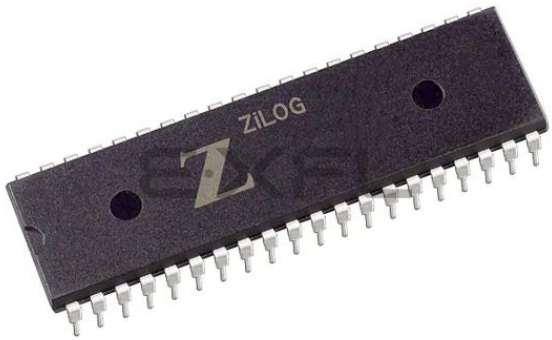

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e6316psc

Warning: DO NOT USE IN LIFE SUPPORT

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As used herein

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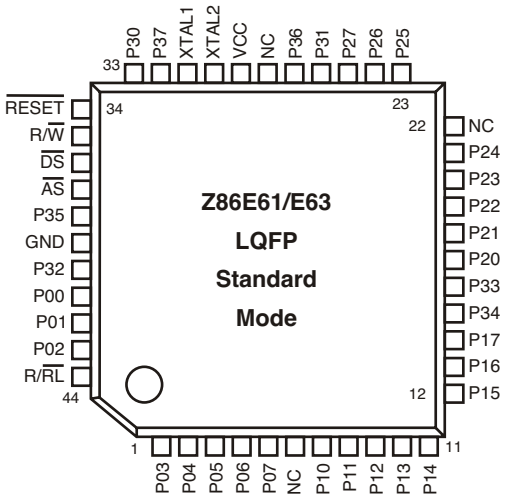
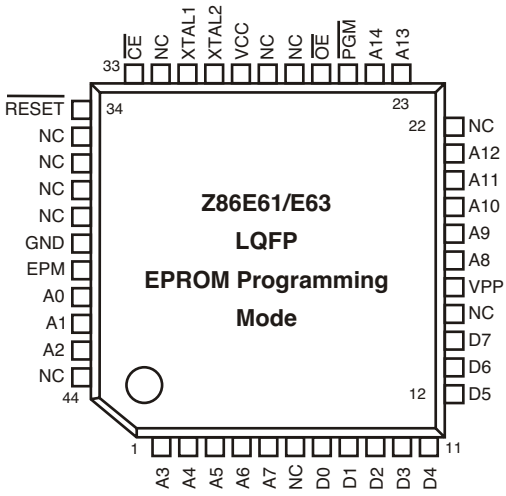


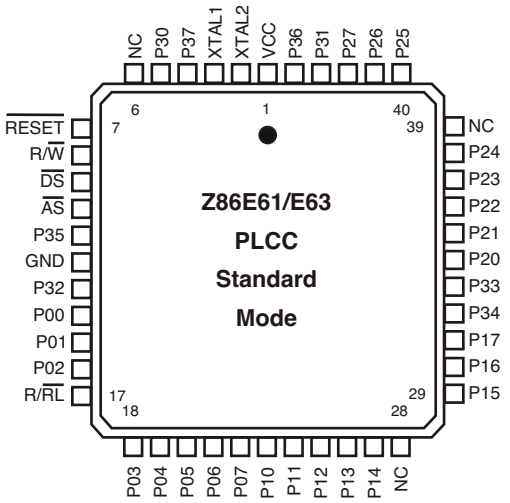
Pin Description - Standard Mode

XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{RESET}}$	Reset	Input
R/$\overline{\text{W}}$	Read/Write	Output
$\overline{\text{DS}}$	Data Strobe	Output
$\overline{\text{AS}}$	Address Strobe	Output
P00-P07 Port 0	8 bit Genaral IO	Input/Output
P10-P17 Port 1	8 bit Genaral IO	Input/Output
P20-P27 Port 2	8 bit Genaral IO	Input/Output
P30-P33 Port 3	4 bit Input	Input
P34-P37 Port 3	4 bit Output	Output
R/$\overline{\text{RL}}$	ROM/ROMless Ctrl	Input
GND	Ground	Input
VCC	Power Supply	Input



Pin Description - EPROM Programming Mode

XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{CE}}$	Chip Enable	Input
$\overline{\text{RESET}}$	Reset	Input
EPM	EPROM Prog Mode	Input
A0-A14	15-bit Address bus	Input
D7-D0	8-bit Data bus	Input/Output
VPP	Prog Voltage	Input
$\overline{\text{PGM}}$	Prog Mode	Input
$\overline{\text{OE}}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
VCC	Power Supply	Input



Pin Description - Standard Mode

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R/$\overline{\text{W}}$	Read/Write	Output
$\overline{\text{DS}}$	Data Strobe	Output
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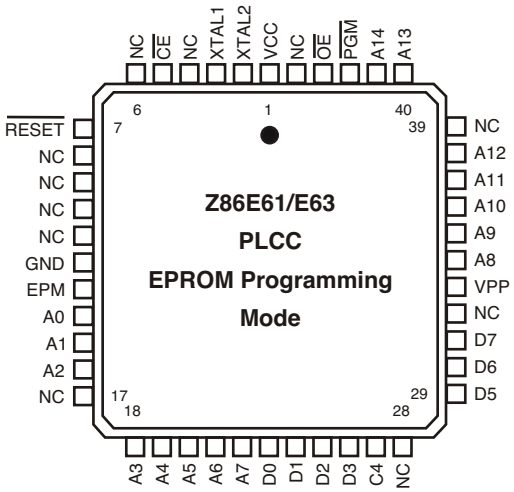
P10-P17 Port 1	8 bit Genaral IO	Input/Output
P20-P27 Port 2	8 bit Genaral IO	Input/Output
P30-P33 Port 3	4 bit Input	Input
P34-P37 Port 3	4 bit Output	Output
R/$\overline{\text{RL}}$	ROM/ROMless Ctrl	Input
GND	Ground	Input
VCC	Power Supply	Input



Pin Description - EPROM Programming Mode

XTAL2	Crystal Oscillator Clock	Output
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$\overline{\text{CE}}$	Chip Enable	Input
$\overline{\text{RESET}}$	Reset	Input
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VPP	Prog Voltage	Input
$\overline{\text{PGM}}$	Prog Mode	Input
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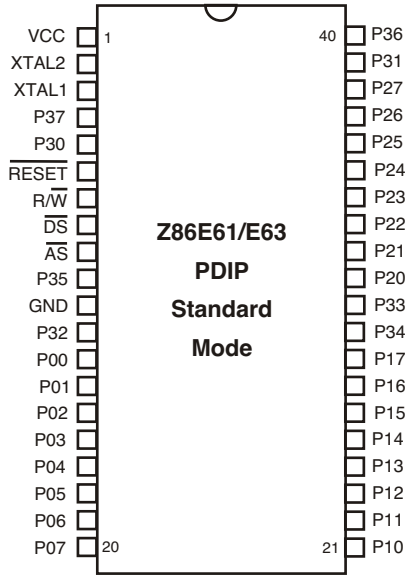

Pin Description - Standard Mode

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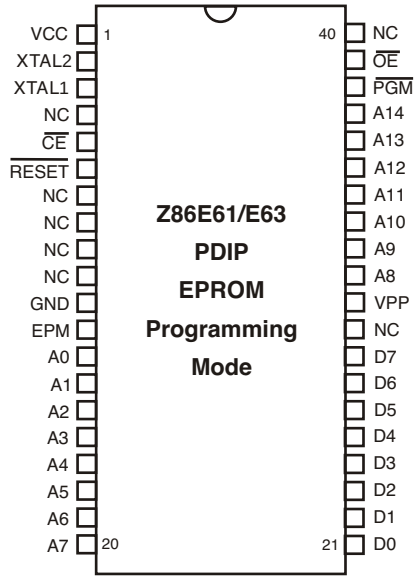
P30-P33 Port 3	4 bit Input	Input
P34-P37 Port 3	4 bit Output	Output
GND	Ground	Input
VCC	Power Supply	Input



Pin Description - EPROM Programming Mode

XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
CE	Chip Enable	Input
$\overline{RESET}$	Reset	Input
$\overline{EPM}$	EPROM Prog Mode	Input
A0-A14	15-bit Address bus	Input
D7-D0	8-bit Data bus	Input/Output
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PGM	Prog Mode	Input
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$\overline{NC}$	Not Connected	Input
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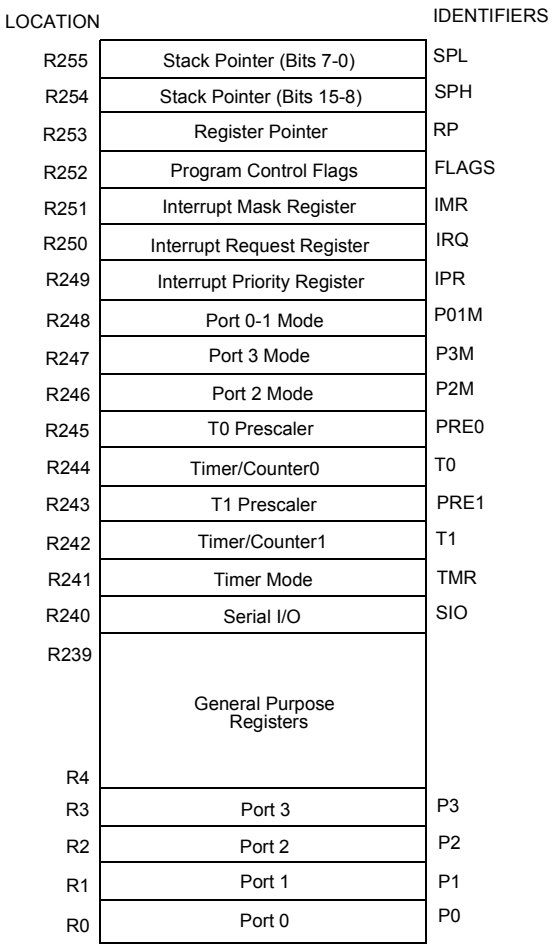


Figure 13. Register File

(single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counter, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 also serves as a timer output (TOUT) through which T0, T1, or the internal clock can be output. The counter/timers are cascaded by connecting the TO output to the input of T1.

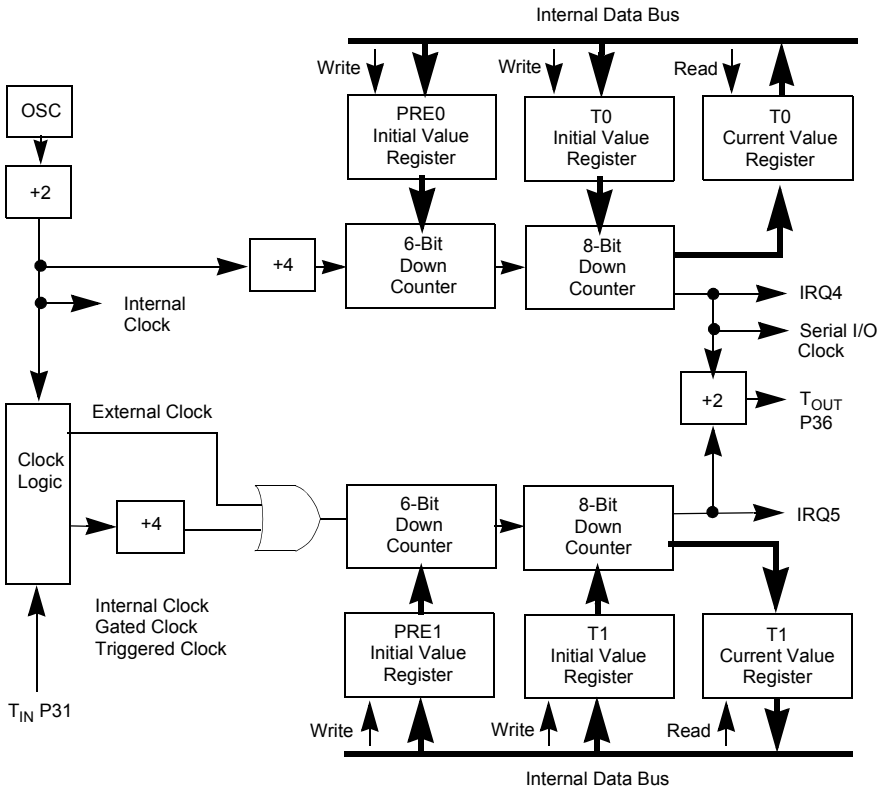


Figure 15. Counter/Timers Block Diagram

Interrupts

The Z86E61/E63 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, one in Serial Out, one in Serial In, and two in the counter/timers (Figure 16). The Interrupt Mask Register globally

User Modes 4 and 5: EPROM and RAM Protect

To extend program security, EPROM and RAM protect cycles are provided for the Z86E61/E63. Execution of the EPROM protect cycle prohibits proper execution of the EPROM Read, EPROM Verify, and EPROM programming cycles. Execution of the RAM protect cycle disables accesses to the upper 128 bytes of register memory (excluding mode and configuration registers), but first the user's program must set bit 6 of the IMR (R251). Timing is shown in Figure 20 and Figure 21.

User Modes. Table 6 shows the programming voltage of each mode of the Z86E61/E63.

Table 22. OTP Programming[a]

User/Test Mode	Device Pins							Port 1
Device Pin No.	P33	P32	P30	P31	P20			CNFG
User Modes	V_{PP}	EPM	CE	OE	PGM	ADDR	V_{CC}	Data
EPROM Read	V_{IH}	V_H[c]	V_{IL}[d]	V_{IL}	V_{IH}	Addr	5.0V	Out
Program	V_{PP}[b]	X	V_{IL}	V_{IH}[e]	V_{IL}	Addr	6.0V	In
Program Verify	V_{PP}[b]	X	V_{IL}	V_{IL}	V_{IH}	Addr	6.0V	Out
EPROM Protect	V_{PP}[b]	V_H	V_H	V_{IH}	V_{IL}	XX[f]	6.0V	XX
RAM Protect	V_{PP}	X	V_H	V_{IH}	V_{IL}	XX[f]	6.0V	XX

a. I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum.
b. V_{PP} = 12.0 ± 0.5 V.
c. V_H = 12.0 ± 0.5 V
d. V_{IL} = 0 V
e. V_{IH} = 5 V.
f. XX = Irrelevant.

Z86E63 Signal Description for EPROM Program/Read

The following signals are required to correctly program or read the Z86E63 device.

ADDR

The address must remain stable throughout the program read cycle.

DATA

The I/O data bus must be stable during programming ($\overline{OE}$ High, $\overline{PGM}$ Low, VPP High). During read the data bus outputs data.

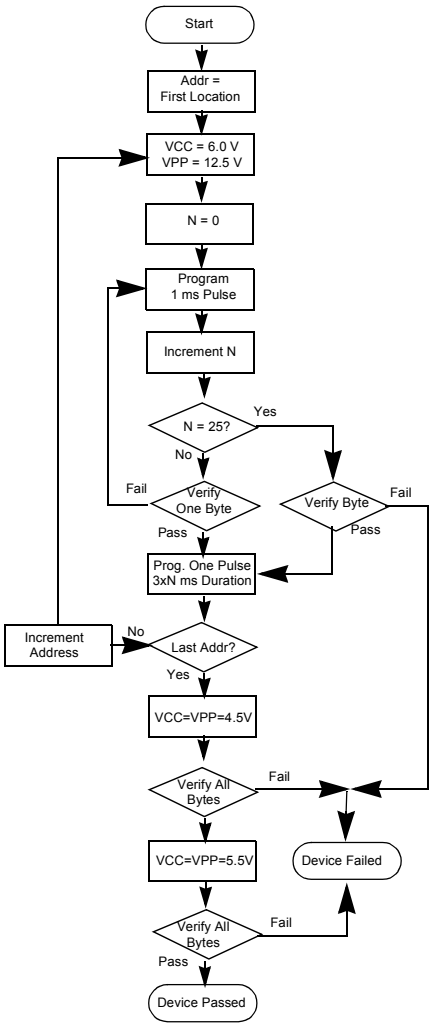


Figure 22. Intelligent Programming Flowchart

ABSOLUTE MAXIMUM RATINGS

Table 24. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage[a]	-0.3	+ 7.0	V
T_{STG}	Storage Temp	-65	+150	°C

Table 24. Absolute Maximum Ratings (Continued)

Symbol	Description	Min	Max	Units
T_A	Operating Ambient Temperature		Note[b]	°C

a. Voltages on all pins with respect to GND.
b. See See “ORDERING INFORMATION” on page 62.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 23).

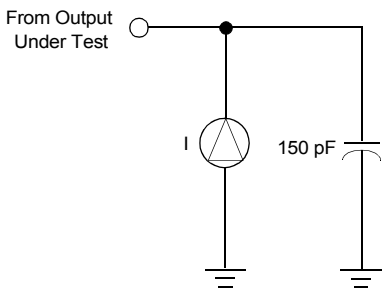


Figure 23. Test Load Diagram

DC CHARACTERISTICS

Table 25. DC Characteristics

Sym	Parameter	T_A = 0 °C to +70°C Min	Max	Typical @ 25 °C	Units	Conditions
	Max Input Voltage		7		V	I_{IN} 250 µA
	Max Input Voltage		13		V	P33-P30 Only
V_{CH}	Clock Input High Voltage	3.8	V_{CC} + 0.3		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	-0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3		V	
V_{IL}	Input Low Voltage	-0.3	0.8		V	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -2.0 mA
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = +2.0 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC} + 0.3		V	
V_{RI}	Reset Input Low Voltage	-0.3	0.8		V	
I_{IL}	Input Leakage	-10	10		µA	0 V V_{IN} + 5.25 V
I_{OL}	Output Leakage	-10	10		µA	0 V V_{IN} + 5.25 V
I_{IR}	Reset Input Current		-50		µA	V_{CC} = + 5.25 V, V_{RL} = 0 V
I_{CC}	Supply Current		50	25	mA	@ 16 MHz
			60	35	mA	@ 20 MHz
I_{CC1}	Standby Current		15	5	mA	HALT Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
			20	10	mA	HALT Mode V_{IN} = 0 V, V_{CC} @ 20 MHz
I_{CC2}[a]	Standby Current		20	5	µA	STOP Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
			20	5	µA	STOP Mode V_{IN} = 0 V, V_{CC} @ 20 MHz

a. ICC2 requires loading TMR (F1Hh) with any value prior to STOP execution.
Use this sequence:
LD TMR,#00
NOP
STOP

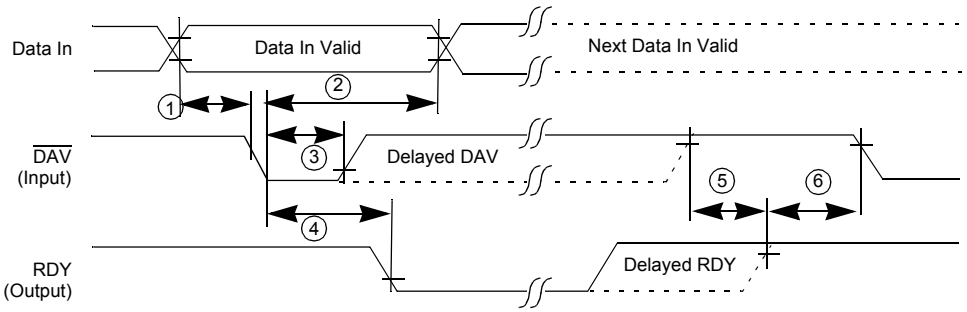


Figure 26. Input Handshake Timing

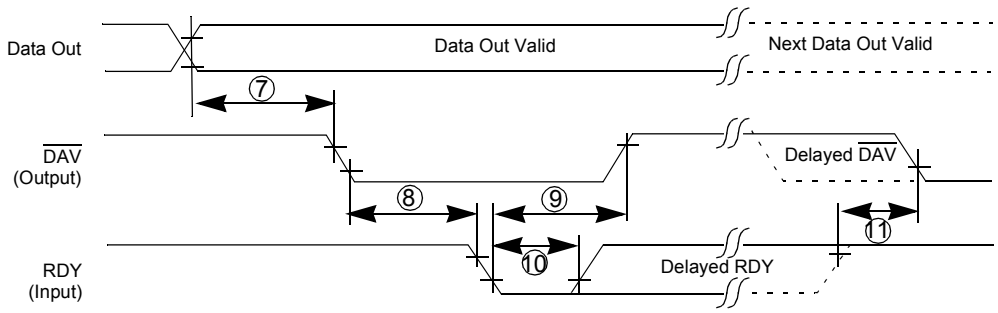


Figure 27. Output Handshake Timing

Table 29. Handshake Timing

			T_A = 0°C to +70°C				
			16 MHz		20 MHz		
No	Symbol	Parameter	Min	Max	Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay		115		115	IN
6	TdRDY0(DAV)	RDY Rise to DAV Fall Delay	0		0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay		TpC		TpC	OUT

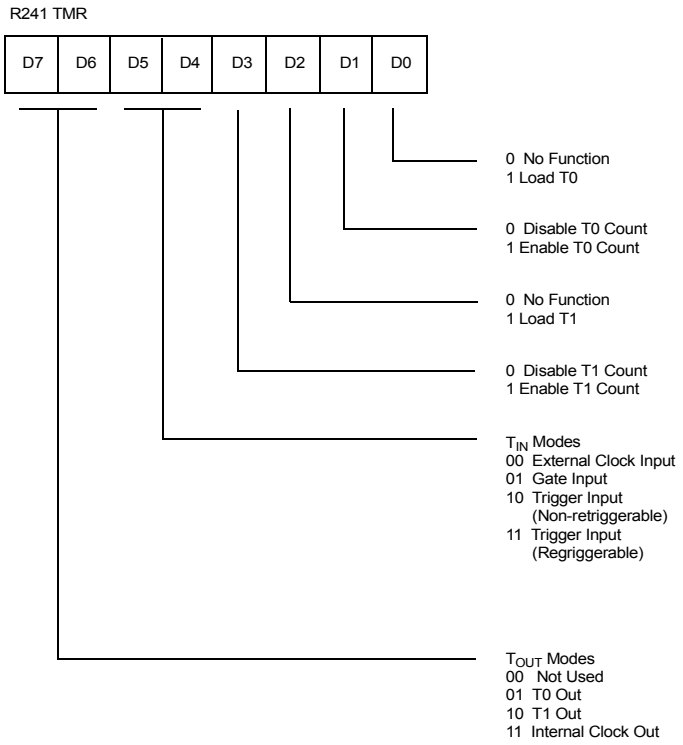


Figure 29. Timer Mode Register ($F1_H$: Read/Write)

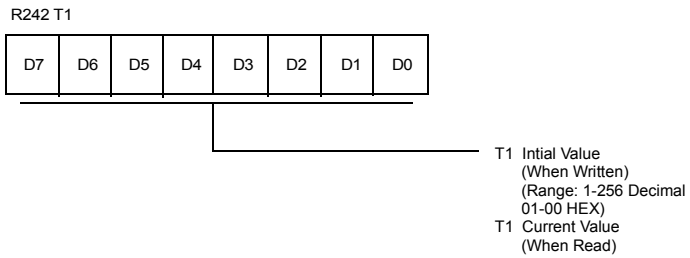


Figure 30. Counter/Timer 1 Register ($F2_H$: Read/Write)

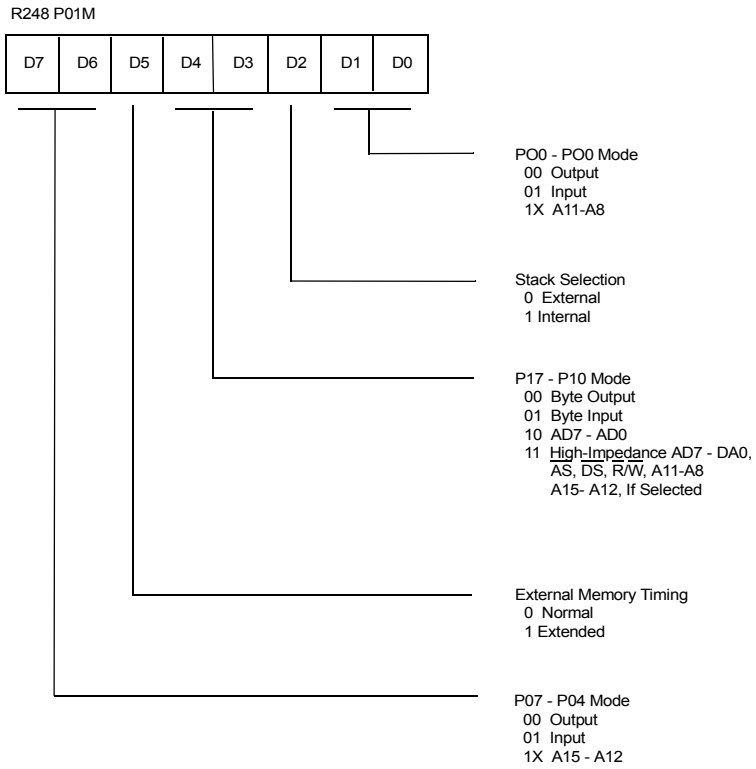


Figure 36. Port 0 and 1 Mode Register ($F8_H$: Write Only)

DC CHARACTERISTICS

Supply Current

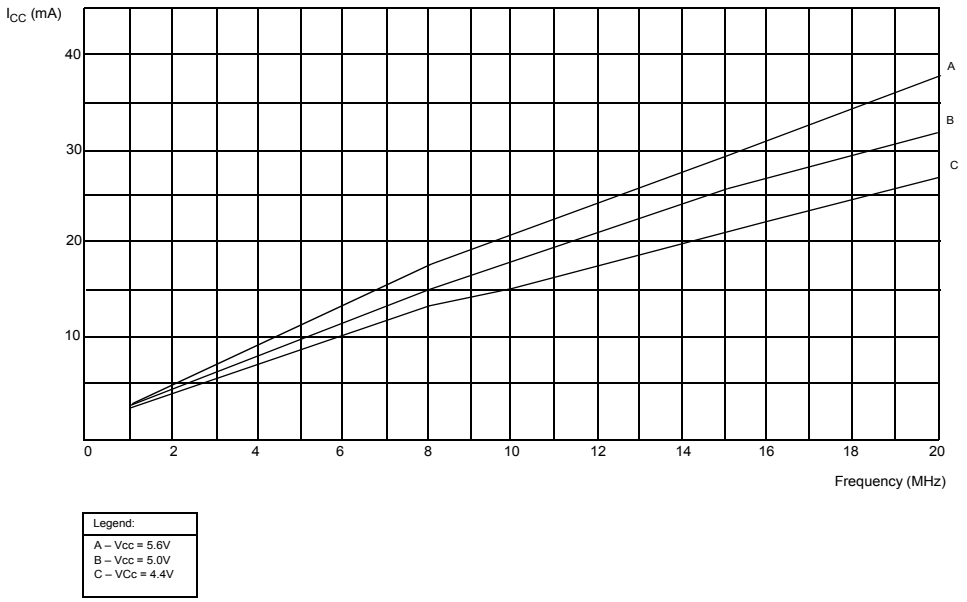


Figure 44. Typical I_{CC} vs. Frequency

Standby Current

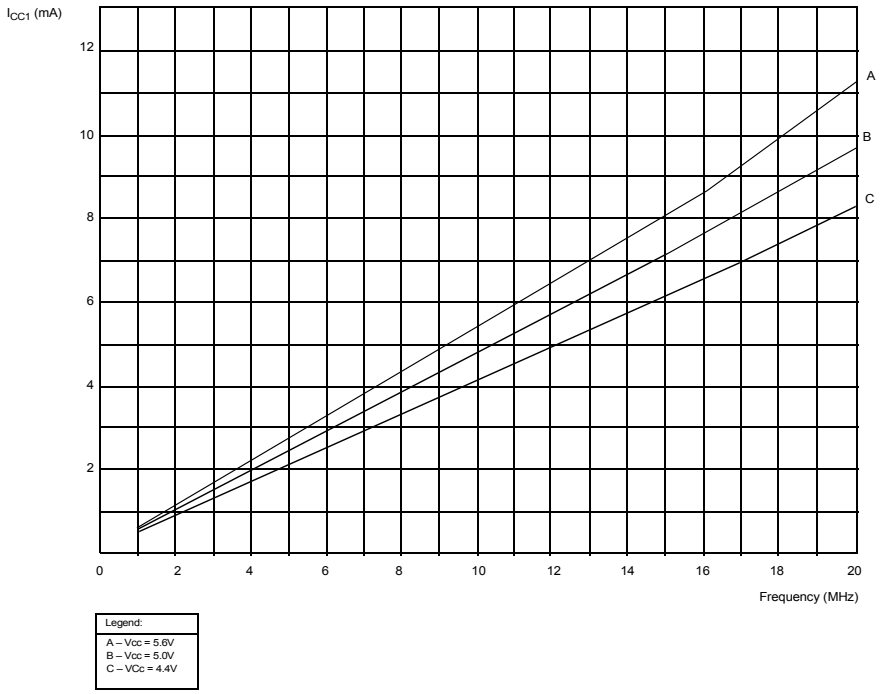
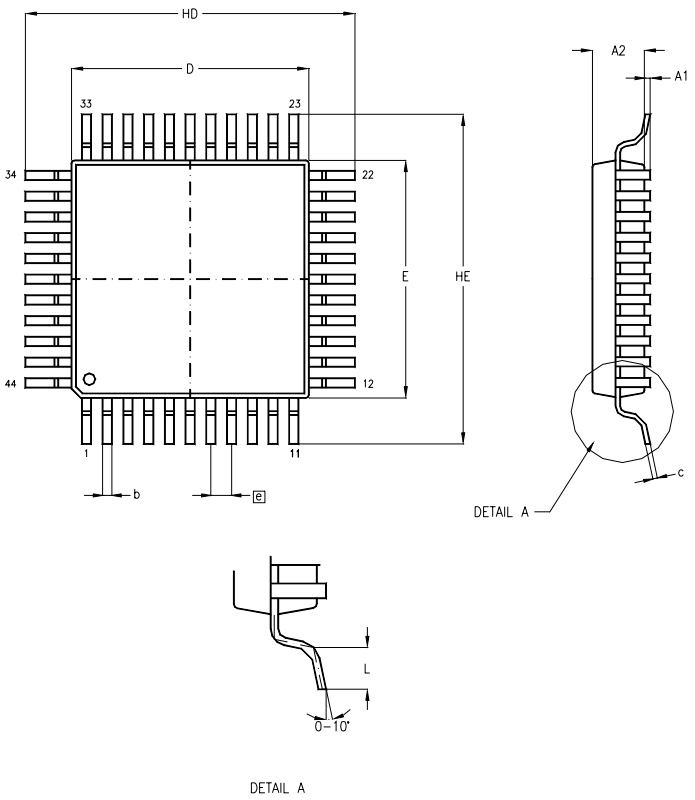


Figure 45. Typical I_{CC1} vs. Frequency

Table 32. Instruction Summary (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
DEC dst	R		00	-	*	*	*	-	-
dst←dst -1	IR		01						
DECW dst	RR		80	-	*	*	*	-	-
dst←dst-1	IR		81						
DI			8F	-	-	-	-	-	-
IMR(7)←0									
DJNZr, dst	RA		rA	-	-	-	-	-	-
r←r -1			r = 0-F						
if r≠0									
PC←PC + dst									
Range: +127,									
-128									
EI			9F	-	-	-	-	-	-
IMR(7)←1									
HALT			7F	-	-	-	-	-	-
INC dst	r		rE	-	*	*	*	-	-
dst←dst + 1			r = 0 - F						
	R		20						
	IR		21						
INCW dst	RR		A0	-	*	*	*	-	-
dst←dst + 1	IR		A1						
IRET			BF	*	*	*	*	*	*
FLAGS←@SP;									
SP←SP + 1									
PC←@SP;									
SP←SP + 2;									
IMR(7)←1									
JP cc, dst	DA		cD	-	-	-	-	-	-



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 BSC		.0315 BSC	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 (.004")

Figure 50. 44-Pin LQFP Package Diagram

ORDERING INFORMATION

Z86E61			
16 MHz		**20 MHz**	
40-Pin DIP	**44-Pin PLCC**	**40-Pin DIP**	**44-Pin PLCC**
Z86E6116PSC	Z86E6116VSC	Z86E6120PSC	Z86E6120VSC
Z86E63			
16 MHz		**20 MHz**	
40-Pin DIP	**44-Pin PLCC**	**40-Pin DIP**	**44-Pin PLCC**
Z86E6316PSC	Z86E6316VSC	Z86E6320PSC	Z86E6320VSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

- Preferred Package
  P = Plastic DIP
  V = Plastic Chip Carrier
- Temperature
  S = 0°C to +70°C
- Speeds
  12 = 16 MHz
  16 = 20 MHz
- Environmental
  C = Plastic Standard

Example: