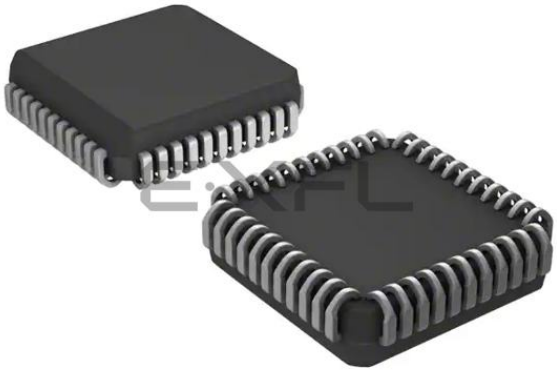


Welcome to E-XFL.COM

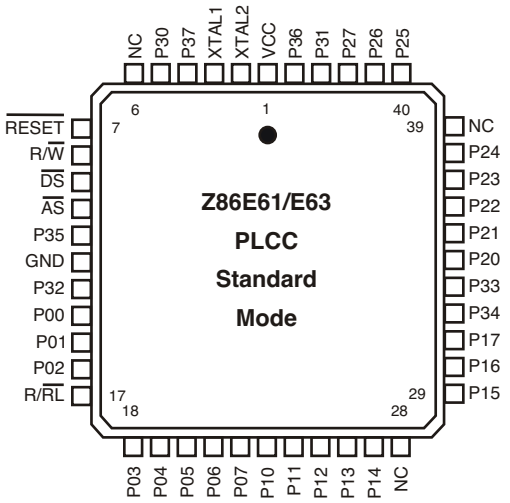
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

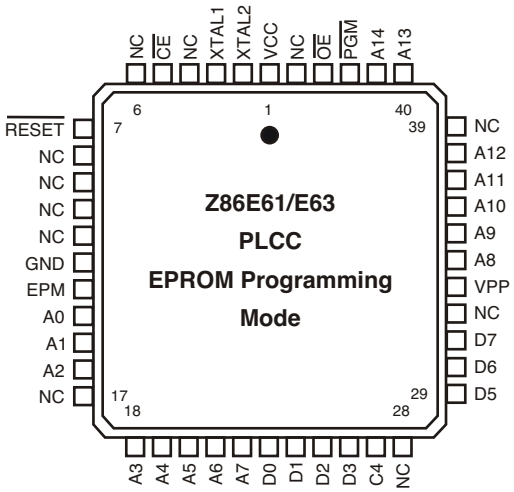
Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e6316vsc

List of Figures



Pin Description - Standard Mode

XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{RESET}}$	Reset	Input
R/$\overline{\text{W}}$	Read/Write	Output
$\overline{\text{DS}}$	Data Strobe	Output
$\overline{\text{AS}}$	Address Strobe	Output
P00-P07 Port 0	8 bit Genaral IO	Input/Output
P10-P17 Port 1	8 bit Genaral IO	Input/Output
P20-P27 Port 2	8 bit Genaral IO	Input/Output
P30-P33 Port 3	4 bit Input	Input
P34-P37 Port 3	4 bit Output	Output
R/$\overline{\text{RL}}$	ROM/ROMless Ctrl	Input
GND	Ground	Input
VCC	Power Supply	Input



Pin Description - EPROM Programming Mode

XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{CE}}$	Chip Enable	Input
$\overline{\text{RESET}}$	Reset	Input
EPM	EPROM Prog Mode	Input
A0-A14	15-bit Address bus	Input
D7-D0	8-bit Data bus	Input/Output
VPP	Prog Voltage	Input
$\overline{\text{PGM}}$	Prog Mode	Input
$\overline{\text{OE}}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
VCC	Power Supply	Input

PIN FUNCTIONS

ROMless (Input, Active Low).

Connecting this pin to GND disables the internal ROM and forces the device to function as a Z86C91 ROMless Z8 (see the Z86C91 product specification for more information). When pulled High to V_{CC}, the device functions as a normal Z86E61/E63 EPROM version.

Note: This pin is only available on the 44-pin versions of the Z86E61/E63.

$\overline{DS}$ (Output, Active Low).

Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{DS}$. For WRITE operations, the falling edge of $\overline{DS}$ indicates that output data is valid.

$\overline{AS}$ (Output, Active Low).

Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{AS}$. Under program control, $\overline{AS}$ can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL2, XTAL1

Crystal 2, Crystal 1 (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R/$\overline{W}$ (Output, Write Low).

The Read/Write signal is Low when the MCU is writing to the external program or data memory.

$\overline{RESET}$ (Input, Active Low).

To avoid asynchronous and noisy reset problems, the Z86E61/E63 is equipped with a reset filter of four external clocks (4TpC). If the external $\overline{RESET}$ signal is less than 4TpC in duration, no reset occurs.

Port 1 can be placed in high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the MCU to share common resources in multiprocessor and DMA applications. Data transfers are controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus Request output (Figure 7).

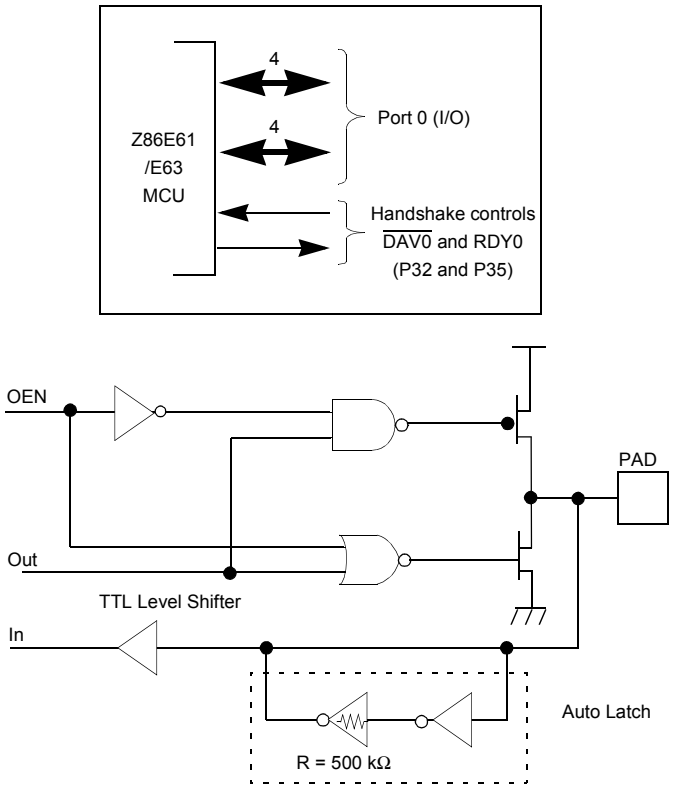


Figure 6. Port 0 Configuration

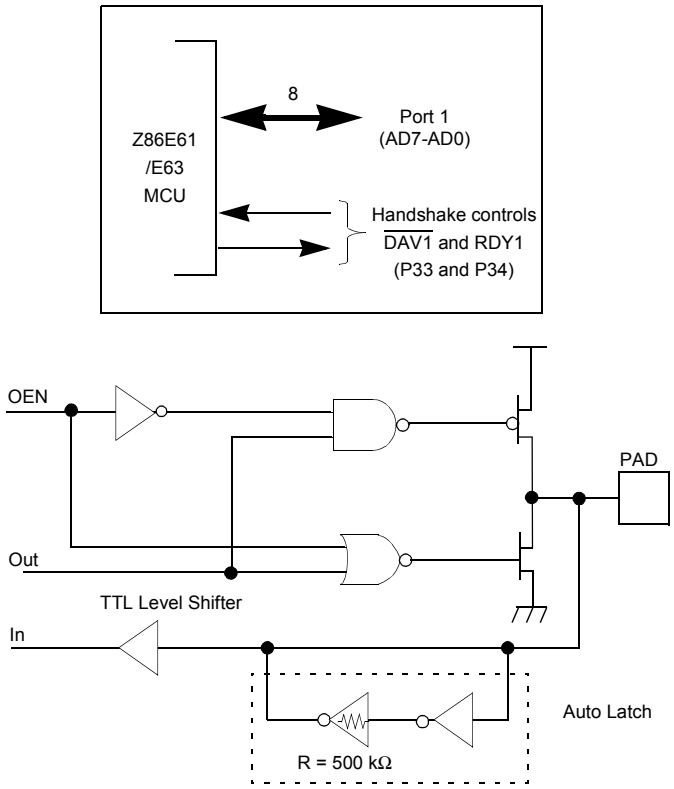


Figure 7. Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bi-directional, CM0S compatible port. Each of these eight I/0 lines can be independently programmed as an input or output, or globally as an open-drain output. Port 2 is always available for I/0 operation. When used as an I/0 port, Port 2 can be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines DAV2 and RDY2. The handshake signal assignment for Port 3 lines, P31 and P36, is dictated by the direction (input or output) assigned to P27 (Figure 8 and Table 21 on page 16).

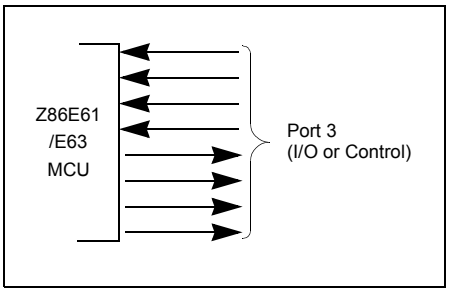


Figure 9. Port 3 Configuration

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (TIN and TOUT) Data Memory Select (/DM) and EPROM control signals (P30 = $\overline{CE}$, P31 = $\overline{OE}$, P32 = EPM and P33 = VPP).

Table 21. Port 3 Pin Assignments

Pin	I/O	CTCI	Int.	P0 HS	P1 HS	P2 HS	UART	Ext	EPROM
P30	IN	T_{IN}	IRQ3				Serial In		$\overline{CE}$
P31	IN	T_{IN}	IRQ2			D/R			$\overline{OE}$
P32	IN	T_{IN}	IRQ0	D/R					EPM
P33	IN	T_{IN}	IRQ1		D/R				V_{PP}
P34	OUT	T_{OUT}			R/D			DM	
P35	OUT	T_{OUT}		R/D					
P36	OUT	T_{OUT}				R/D			
P37	OUT	T_{OUT}					Serial Out		
T0			IRQ4						
T1			IRQ5						

1. HS = Handshake Signals D = Data Available R = Ready

ADDRESS SPACE

Program Memory. The Z86E61/E63 can address 48 Kbytes (E61) or 32 Kbytes (E63) of external program memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 13 to byte 16383 (E61) or 32767 (E63) consists of on-chip EPROM. At addresses 16384 (E61) or 32768 (E63) and above, the Z86E61/E63 executes external program memory fetches. In ROMless mode, the Z86E61/E63 can address up to 64 Kbytes of program memory. Program execution begins at external location 000C (HEX) after a reset.

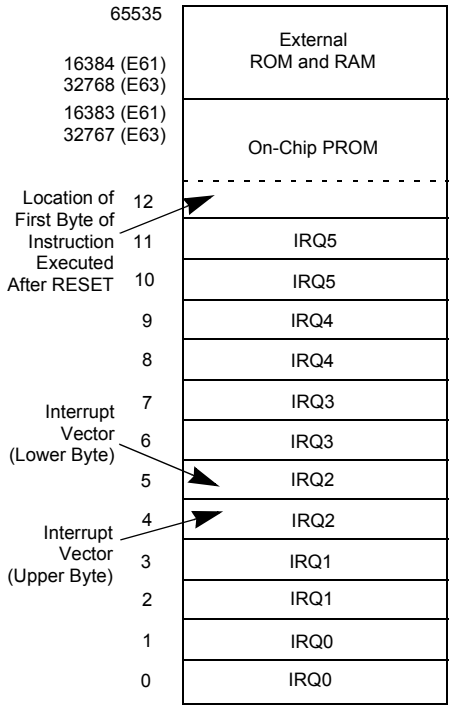


Figure 11. Program Memory Configuration

Data Memory ($\overline{DM}$)

The EPROM version can address up to 48 Kbytes (E61) or 32 Kbytes (E63) of external data memory space beginning at location 16384 (E61) or 32768 (E63). The ROMless version can address up to 64 Kbytes of external data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/0 function that can be programmed to appear on pin P34, is used to distinguish between data and program memory

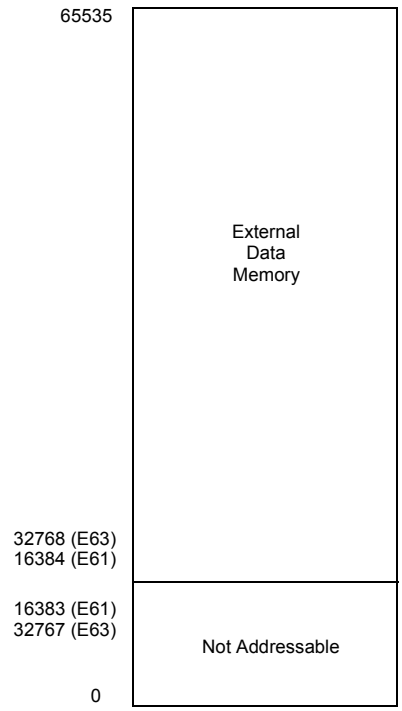


Figure 12. Data Memory Configuration

must execute a NOP (opcode = 0FFH) immediately before the appropriate SLEEP instruction. i.e.,

```
FF              NOP         ; clear the pipeline
6F              STOP        ; enter STOP mode
                or
FF              NOP         ; clear the pipeline
7F              HALT        ; enter HALT mode
```

PROGRAMMING

Z86E61/E63 User Modes

The Z86E61/E63 uses separate AC timing cycles for the different User Modes available. Table 22 on page 27 shows the Z86E61/E63 User Modes. Table 23 on page 28 shows the timing of the programming waveforms.

User MODE 1 EPROM Read

The Z86E61 /E63 EPROM read cycle is provided so that the user may read the Z86E61 /E63 as a standard 27128 (E61) or 27256 (E63) EPROM. This is accomplished by driving the $\overline{EPM}$ pin (P32) to VH and activating $\overline{CE}$ and $\overline{OE}$. $\overline{PGM}$ remains inactive. This mode is not valid after execution of an EPROM protect cycle. Timing for the EPROM read cycle is shown in Figure 18.

User MODE 2 EPROM Program

The Z86E61/E63 Program function conforms to the Intelligent programming algorithm. The device is programmed with V_{cc}, at 6.0V and V_{PP} = 12.5V. Programming pulses are applied in 1 ms increments to a maximum of 25 pulses before proper verification. After verification, a programming pulse of three times the duration of the cycles necessary to program the device is issued to ensure proper programming. After all addresses are programmed, a final data comparison is executed and the programming cycle is complete. Timing for the Z86E61/E63 programming cycle is shown in Figure 18.

User Mode 3: PROM Verify

The Program Verify cycle is used as part of the intelligent programming algorithm to insure data integrity under worst-case conditions. It differs from the EPROM Read cycle in that Vpp is active and V_{CC} must be driven to 6.0V. Timing is shown in Figure 18.

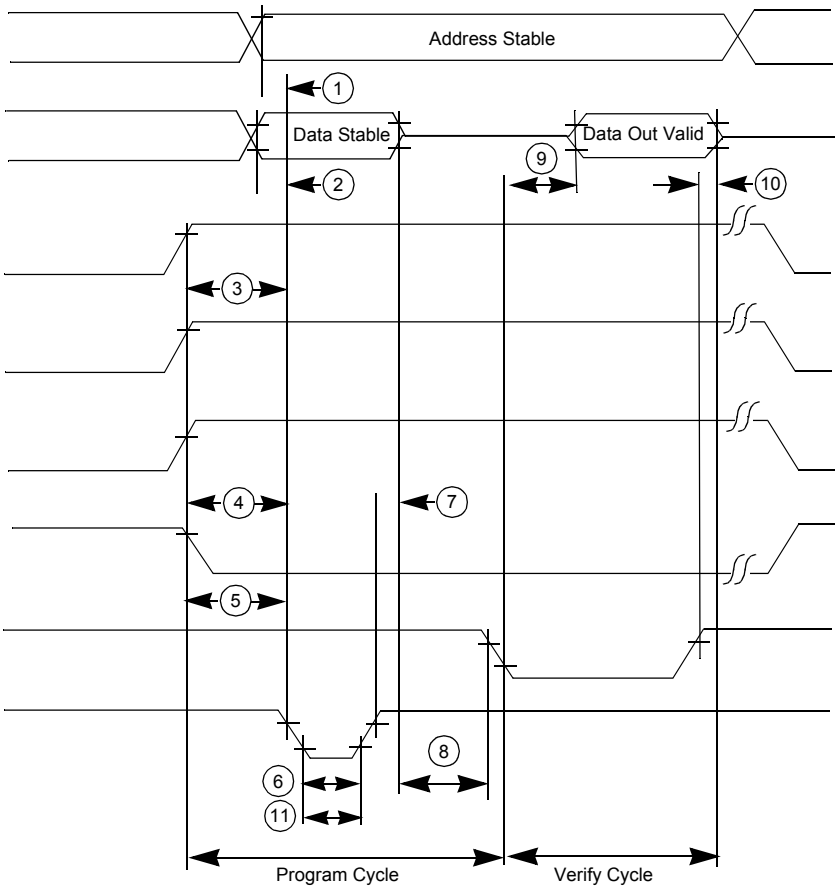


Figure 19. EPROM Program and Verity

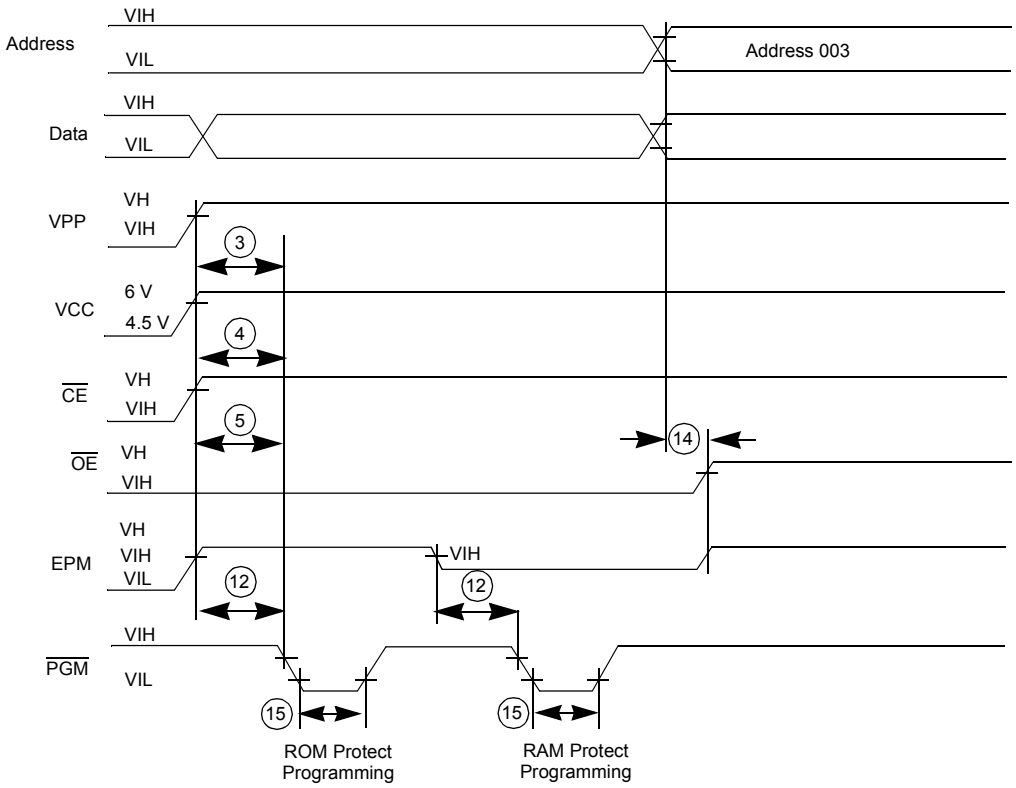


Figure 20. Programming EPROM, RAM Protect, and 4K Size Selection

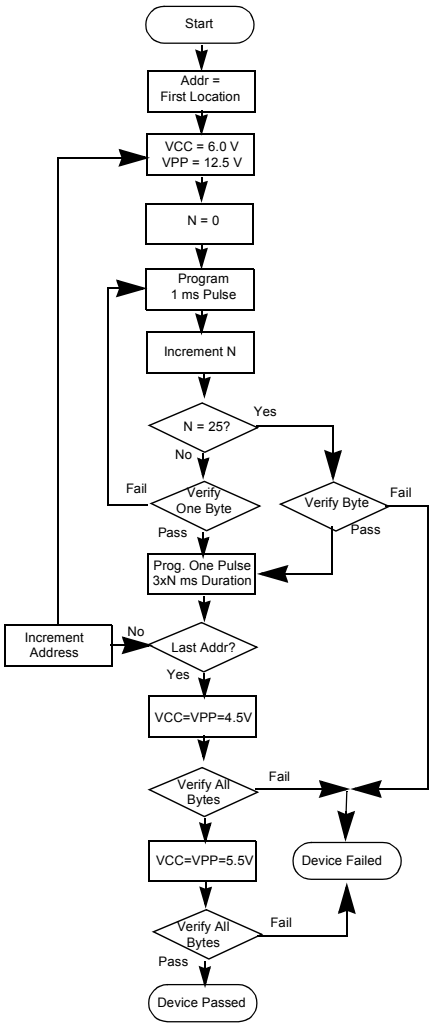


Figure 22. Intelligent Programming Flowchart

ABSOLUTE MAXIMUM RATINGS

Table 24. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage[a]	-0.3	+ 7.0	V
T_{STG}	Storage Temp	-65	+150	°C

Table 24. Absolute Maximum Ratings (Continued)

Symbol	Description	Min	Max	Units
T_A	Operating Ambient Temperature		Note[b]	°C

a. Voltages on all pins with respect to GND.
b. See See “ORDERING INFORMATION” on page 62.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 23).

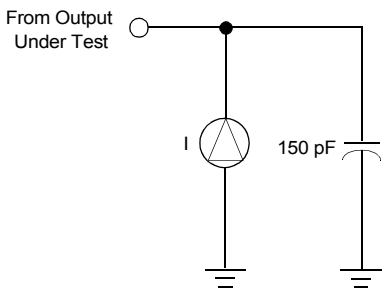


Figure 23. Test Load Diagram

AC CHARACTERISTICS

Table 26. External I/O or Memory Read and Write Timing

			TA = 0°C to +70°C					
			16 MHz[a]		20 MHz			
No	Symbol	Parameter	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	20		26		ns	Note[b,c]
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	30		28		ns	Note[b,c]
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid		180		160	ns	Note[b,c,d]
4	TwAS	$\overline{AS}$ Low Width	35		36		ns	Note[b,c]
5	TdAZ(DS)	Address Float to $\overline{DS}$ Fall	0		0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	135		130		ns	Note[b,c,d]
7	TwDSW	$\overline{DS}$ (Write) Low Width	80		75		ns	Note[b,c,d]
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid		75		100	ns	Note[b,c,d]
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	0		0		ns	Note[b,c]
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	35		48		ns	Note[b,c]
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	30		36		ns	Note[b,c]
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	20		32		ns	Note[b,c]
13	TdDS(R/W)	$\overline{DS}$ Rise to R//W Not Valid	30		36		ns	Note[b,c]
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	25		40		ns	Note[b,c]
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	30		40		ns	Note[b,c]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		200		200	ns	Note[b,c,d]
17	TdAS(DS)AS	AS Rise to $\overline{DS}$ Fall Delay	40		48		ns	Note[b,c]
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Fall Delay	30		36		ns	Note[b,c]

a. All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
b. Timing numbers given are for minimum TpC.
c. See Table 11
d. When using extended memory timing add 2 TpC.

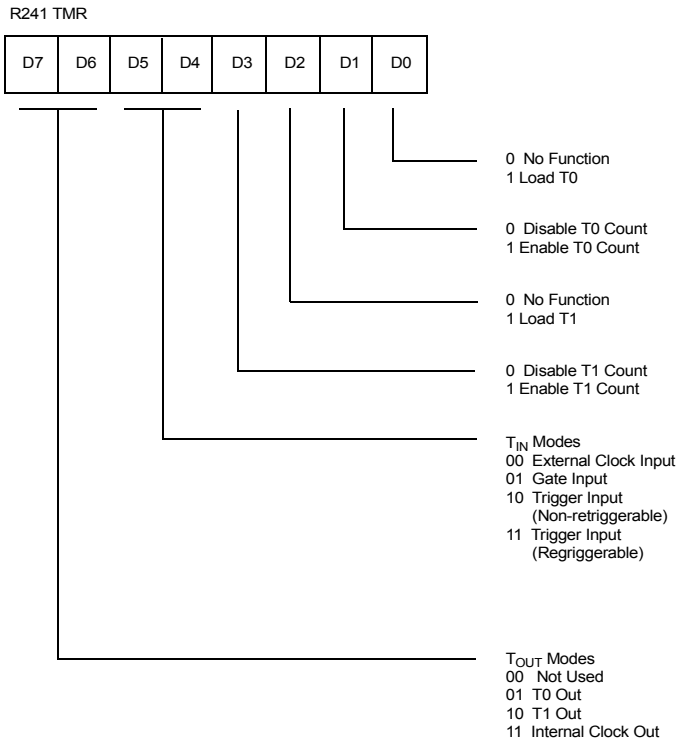


Figure 29. Timer Mode Register ($F1_H$: Read/Write)

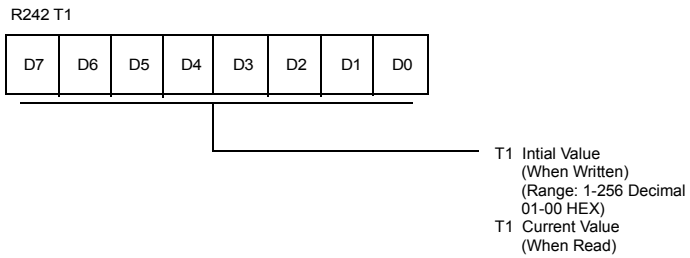


Figure 30. Counter/Timer 1 Register ($F2_H$: Read/Write)

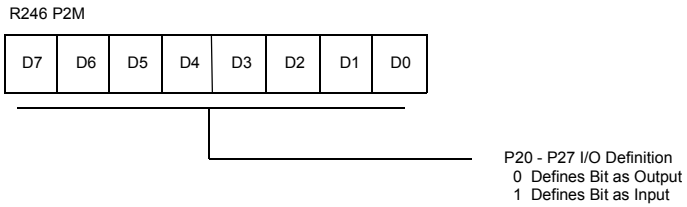


Figure 34. Port 2 Mode Register ($F6_H$: Write Only)

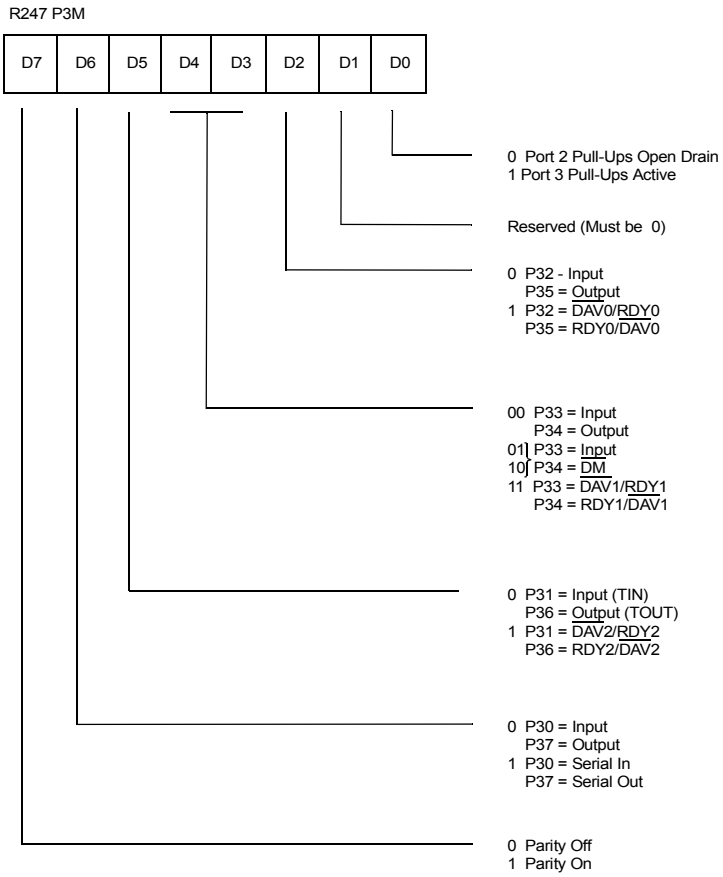


Figure 35. Port 3 Mode Register ($F7_H$: Write Only)

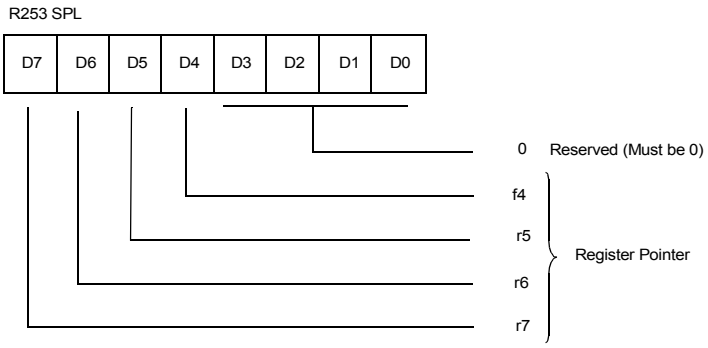


Figure 41. Register Pointer Register (FD_H: Read/Write)

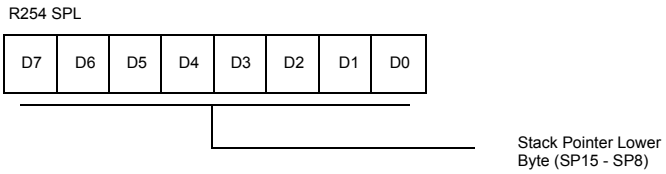


Figure 42. Stack Pointer Register (FE_H: Read/Write)

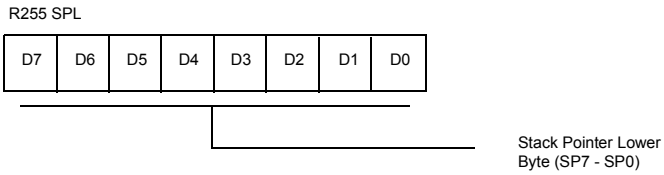


Figure 43. Stack Pointer Register (FF_H: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary (Table 14).

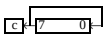
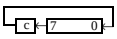
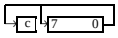
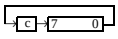
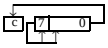
Table 30. Instruction Set Notation

Symbol	Meaning
IRR	Indirect register pair or indirect working register pair address
Irr	Indirect working register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working register address
r	Working register address only
IR	Indirect register or indirect working register address
Ir	Indirect working register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition Code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag Register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt Mask Register (R251)

Table 32. Instruction Summary (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
dst←dst OR src									
POP	R		50	-	-	-	-	-	-
dst←@SP;	IR		51						
SP←SP + 1									
PUSH src	R		70	-	-	-	-	-	-
SP←SP-1;	IR		71						
@SP←src									
RCF			CF	0	-	-	-	-	-
C←0									
RET			AF	-	-	-	-	-	-
PC←@SP;									
SP←SP +2									
RL dst	R		90	*	*	*	*	-	-
	IR		91						
RLC dst	R		10	*	*	*	*	-	-
	IR		11						
RR dst	R		E0	*	*	*	*	-	-
	IR		E1						
RRC dst	R		C0	*	*	*	*	-	-
	IR		C1						
SBC dst, src	Note[a]		3[ ]	*	*	*	*	1	*
dst←dst←src←C									
SCF			DF	1	-	-	-	-	-
C←1									
SRA dst	R		D0	*	*	*	0	-	-
	IR		D1						
SRP dst	Im		31	-	-	-	-	-	-

CODES

- Preferred Package
  P = Plastic DIP
  V = Plastic Chip Carrier
- Temperature
  S = 0°C to +70°C
- Speeds
  12 = 16 MHz
  16 = 20 MHz
- Environmental
  C = Plastic Standard

Example: