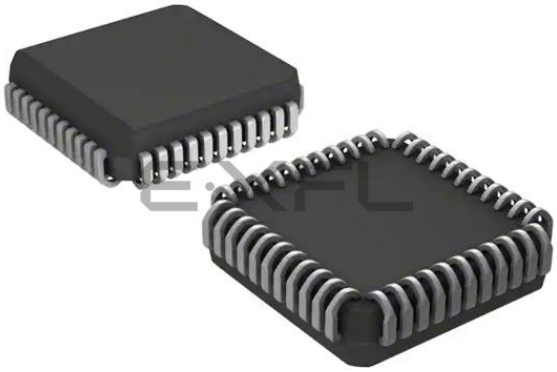

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e6316vsc00tr

GENERAL DESCRIPTION

The Z86E61/E63 microcontrollers are members of the Z8® single-chip microcontroller family with 16K/32 Kbytes of EPROM and 236 bytes of general-purpose RAM. Offered in 40-pin DIP, 44-pin PLCC or 44-Pin LQFP package styles, these devices are pin-compatible EPROM versions of the Z86C61/ 63. The ROMless pin option is available on the 44-pin versions only.

With 4 Kbytes of ROM and 236 bytes of general-purpose RAM, the Z86E61/E63 offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

For applications demanding powerful I/O capabilities, the Z86E61/E63 offers 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

The Z86E61/E63 can address both external memory and preprogrammed ROM, making it well suited for high-volume applications or where code flexibility is required. There are three basic address spaces available to support this configuration: Program Memory, Data Memory, and 236 general-purpose registers.

To unburden the system from coping with real-time tasks such as counting/timing and serial data communication, the Z86E61/E63 offers two on-chip counter/timers with a large number of user selectable modes (Figure 1).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Port 1 can be placed in high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the MCU to share common resources in multiprocessor and DMA applications. Data transfers are controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus Request output (Figure 7).

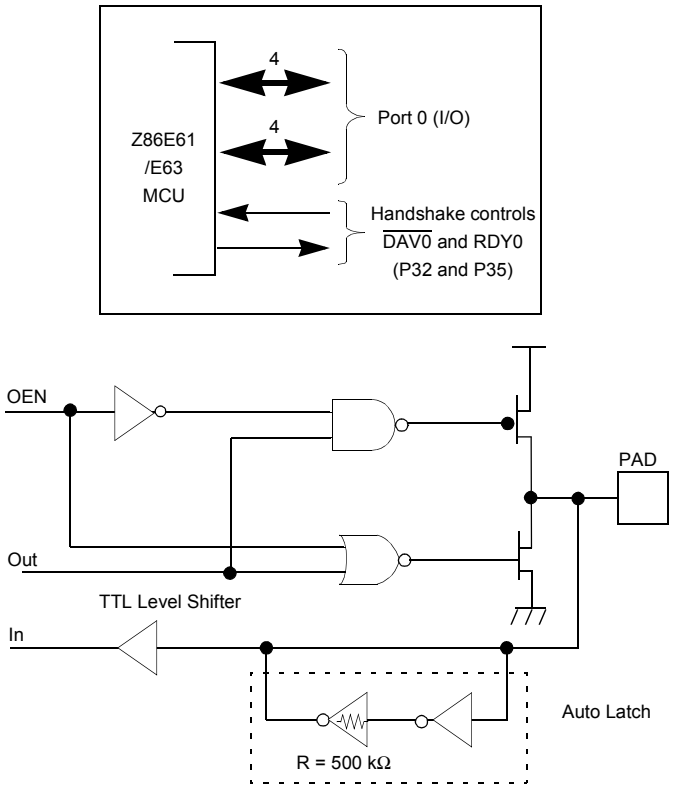


Figure 6. Port 0 Configuration

UART OPERATION

Port 3 lines, P37 and P30, are programmed as serial I/0 lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/ Timer0.

The Z86E61/E63 automatically adds a start bit and two stop bits to transmitted data (Figure 10). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits, and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

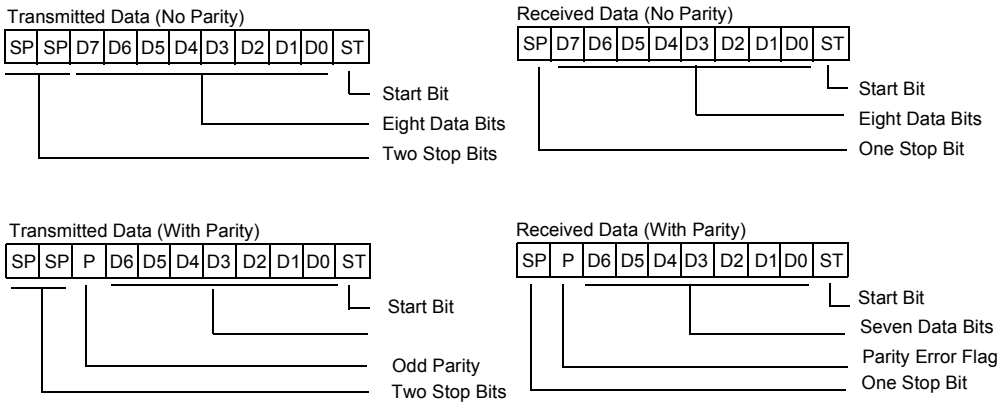


Figure 10. Serial Data Formats

Auto Latch

The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not driven by any source.

Note: P33-P30 inputs differ from the Z86C61/C63 in that there is no clamping diode to V_{CC} because of the EPROM high voltage detection circuits. Exceeding the VIH maximum specification during standard operating mode may cause the device to enter EPROM mode.

ADDRESS SPACE

Program Memory. The Z86E61/E63 can address 48 Kbytes (E61) or 32 Kbytes (E63) of external program memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 13 to byte 16383 (E61) or 32767 (E63) consists of on-chip EPROM. At addresses 16384 (E61) or 32768 (E63) and above, the Z86E61/E63 executes external program memory fetches. In ROMless mode, the Z86E61/E63 can address up to 64 Kbytes of program memory. Program execution begins at external location 000C (HEX) after a reset.

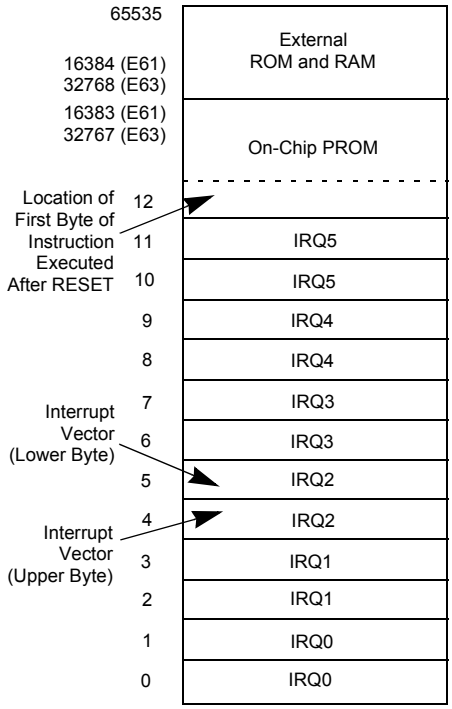


Figure 11. Program Memory Configuration

Data Memory ($\overline{DM}$)

The EPROM version can address up to 48 Kbytes (E61) or 32 Kbytes (E63) of external data memory space beginning at location 16384 (E61) or 32768 (E63). The ROMless version can address up to 64 Kbytes of external data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/0 function that can be programmed to appear on pin P34, is used to distinguish between data and program memory

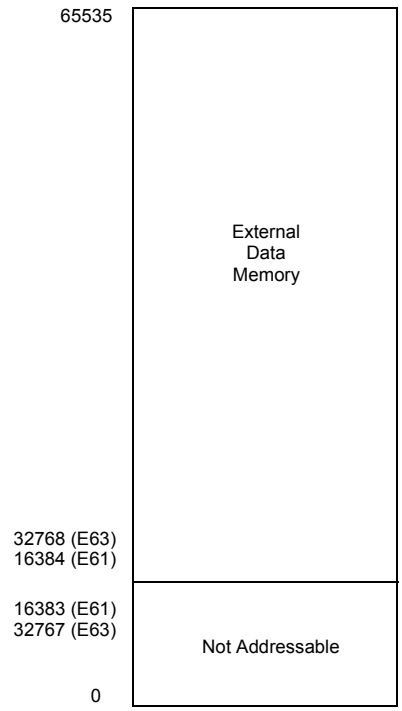


Figure 12. Data Memory Configuration

(single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counter, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 also serves as a timer output (TOUT) through which T0, T1, or the internal clock can be output. The counter/timers are cascaded by connecting the TO output to the input of T1.

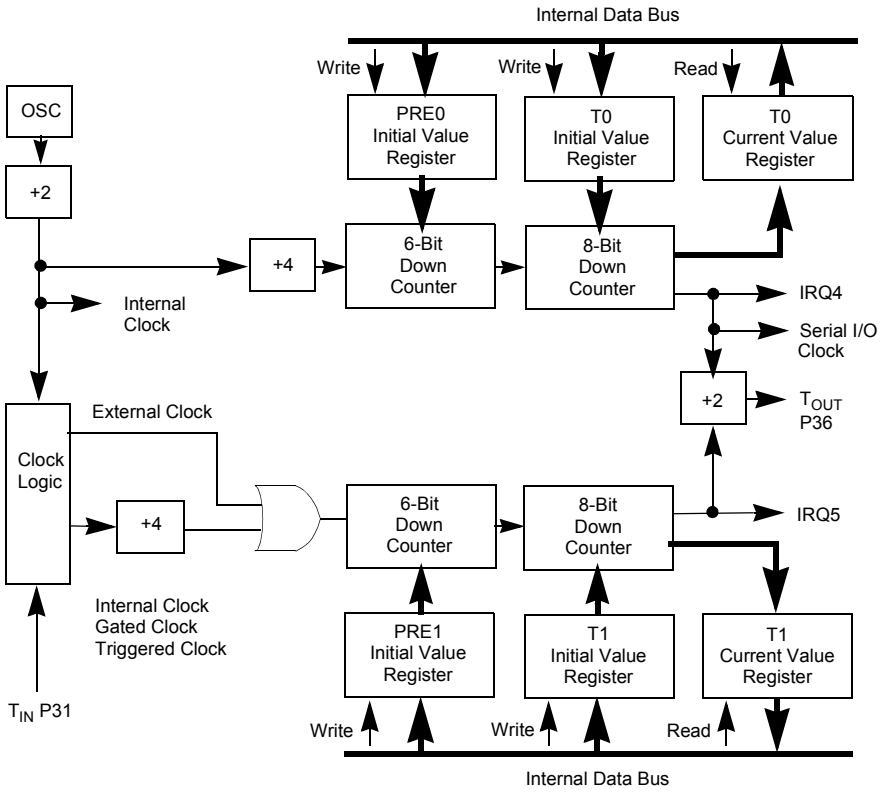


Figure 15. Counter/Timers Block Diagram

Interrupts

The Z86E61/E63 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, one in Serial Out, one in Serial In, and two in the counter/timers (Figure 16). The Interrupt Mask Register globally

XCLK

A clock is required to clock the $\overline{\text{RESET}}$ signal into the registers before programming.

A constant clock can be applied, or the XCLK input can be toggled a minimum of 12 cycles before any programming or verify function begins. The maximum clock frequency to be applied when in the EPROM mode is 12 MHz.

$\overline{\text{RESET}}$

The reset input can be held to a constant Low or High value throughout normal programming. It must be held High to program the EPROM protect option bit. Also, any time the $\overline{\text{RESET}}$ input changes state the XCLK must be clocked a minimum of 12 times to clock the $\overline{\text{RESET}}$ through the reset filter.

$\overline{\text{OE}}$

When the device is placed in EPROM mode, the $\overline{\text{OE}}$ input also serves as the precharge for the sense amp. The precharge signal should be Low for the first half of the stable address and High for the second half. The PRECHG signal is inverted from the $\overline{\text{OE}}$ signal so the $\overline{\text{OE}}$ should be High on the first half and Low on the second half, or stable address. The EPROM output data should be sampled during the second half of stable address.

The access time of the EPROM is defined in later sections. This two part calculation of access time is required because this is a precharged sense amp with a precharge clock.

Table 23. Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		µs
8	$\overline{\text{OE}}$ Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns

Table 23. Timing of Programming Waveforms (Continued)

Parameters	Name	Min	Max	Units
11	Over program Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	$\overline{PGM}$ Setup Time	2		µs
14	Address to $\overline{OE}$ Setup Time	2		µs
15	Option Program Pulse Width	78		ms

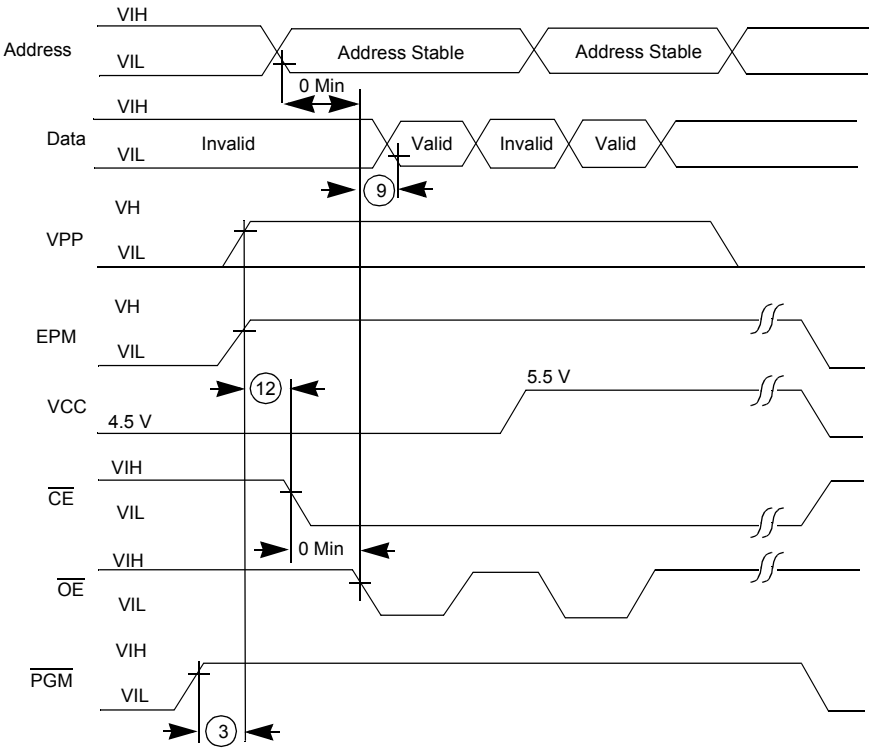


Figure 18. EPROM Read

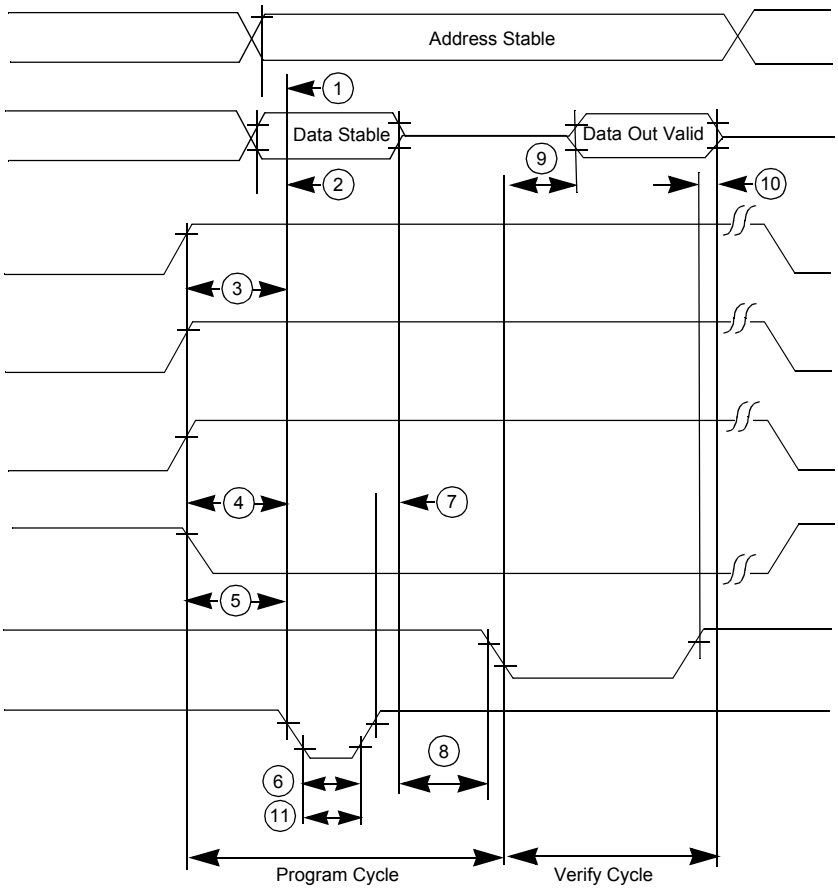


Figure 19. EPROM Program and Verity

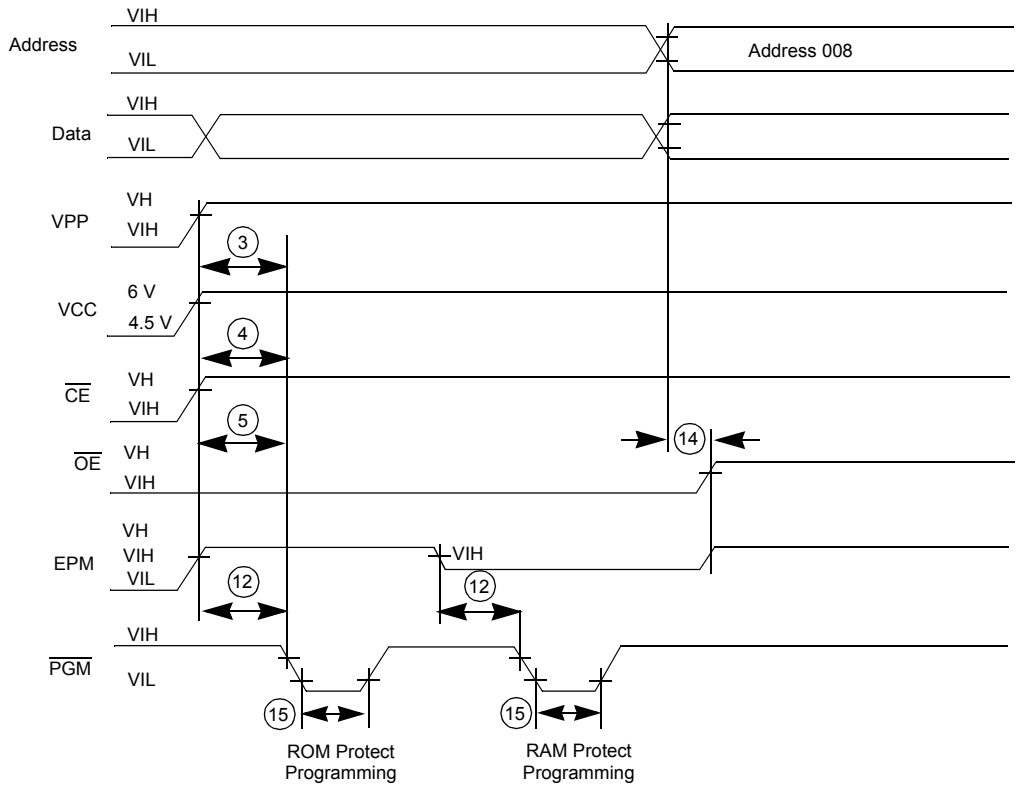


Figure 21. Programming EPROM, RAM Protect, and 16K Size Selection

DC CHARACTERISTICS

Table 25. DC Characteristics

Sym	Parameter	T_A = 0 °C to +70°C Min	Max	Typical @ 25 °C	Units	Conditions
	Max Input Voltage		7		V	I_{IN} 250 µA
	Max Input Voltage		13		V	P33-P30 Only
V_{CH}	Clock Input High Voltage	3.8	V_{CC} + 0.3		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	-0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3		V	
V_{IL}	Input Low Voltage	-0.3	0.8		V	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -2.0 mA
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = +2.0 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC} + 0.3		V	
V_{RI}	Reset Input Low Voltage	-0.3	0.8		V	
I_{IL}	Input Leakage	-10	10		µA	0 V V_{IN} + 5.25 V
I_{OL}	Output Leakage	-10	10		µA	0 V V_{IN} + 5.25 V
I_{IR}	Reset Input Current		-50		µA	V_{CC} = + 5.25 V, V_{RL} = 0 V
I_{CC}	Supply Current		50	25	mA	@ 16 MHz
			60	35	mA	@ 20 MHz
I_{CC1}	Standby Current		15	5	mA	HALT Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
			20	10	mA	HALT Mode V_{IN} = 0 V, V_{CC} @ 20 MHz
I_{CC2}[a]	Standby Current		20	5	µA	STOP Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
			20	5	µA	STOP Mode V_{IN} = 0 V, V_{CC} @ 20 MHz

a. ICC2 requires loading TMR (F1Hh) with any value prior to STOP execution.
Use this sequence:
LD TMR,#00
NOP
STOP

Table 27. Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40 TpC + 0.32
2	TdAS(A)	0.59 TpC - 3.25
3	TdAS(DR)	2.83 TpC + 6.14
4	TwAS	0.66 TpC - 1.65
6	TwDSR	2.33 TpC - 10.56
7	TwDSW	1.27 TpC + 1.67
8	TdDSR(DR)	1.97 TpC - 42.5
10	TdDS(A)	0.8 TpC
11	TdDS(AS)	0.59 TpC - 3.14
12	TdR/W(AS)	0.4 TpC
13	TdDS(R/$\overline{W}$)	0.8 TpC - 15
14	TdDW(DSW)	0.4 sTpC
15	TdDS(DW)	0.88 TpC - 19
16	TdA(DR)	4 TpC - 20
17	TdAS(DS)	0.91 TpC - 10.7
18	TdDM(AS)	0.9 TpC - 26.3

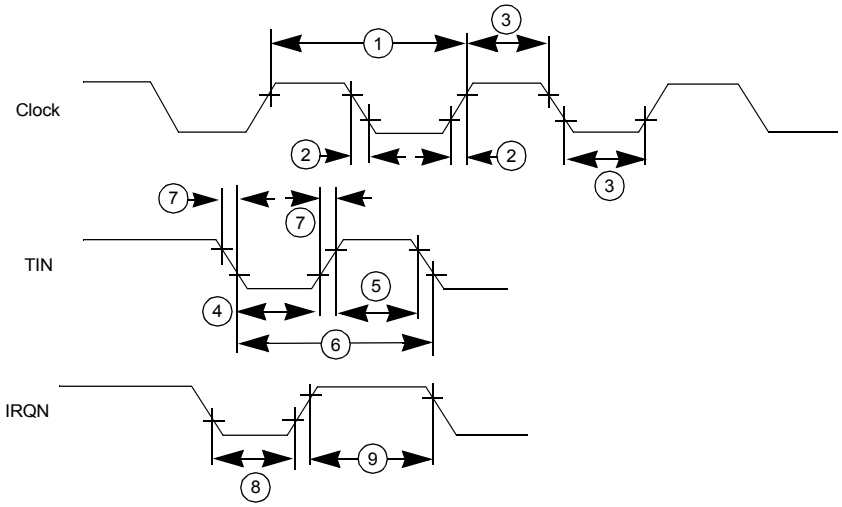


Figure 25. Additional Timing

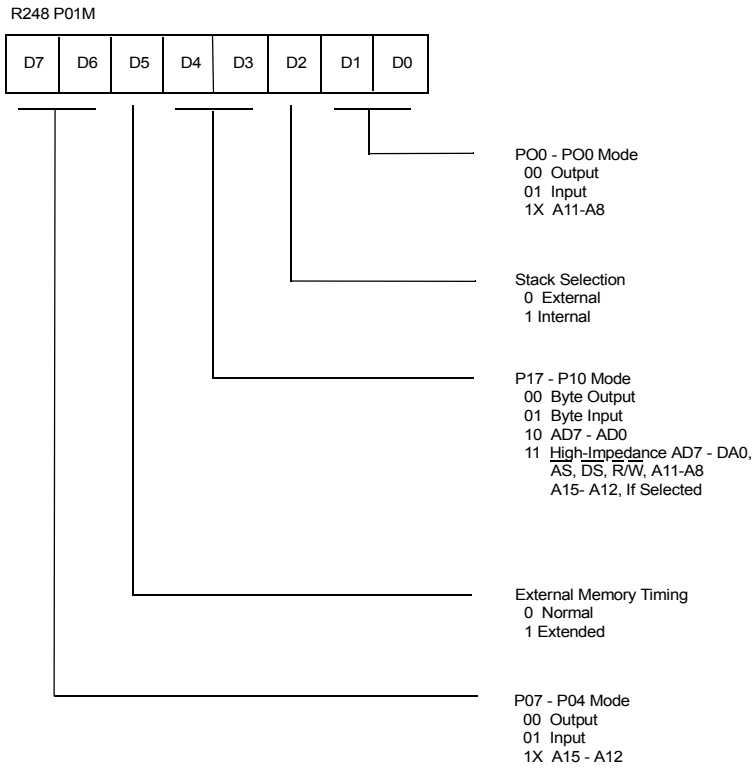


Figure 36. Port 0 and 1 Mode Register ($F8_H$: Write Only)

Table 32. Instruction Summary (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
if cc is true,			c = 0 - F						
PC←dst	IRR		30						
JR cc, dst	RA		cB	-	-	-	-	-	-
if cc is true,			c = 0 - F						
PC←PC + dst									
Range: +127,									
-128									
LD dst, src	r	Im	rC	-	-	-	-	-	-
dst←src	r	R	r8						
	R	r	r9						
			r = 0-F						
	r	X	C7						
	X	r	D7						
	r	Ir	E3						
	Ir	r	F3						
	R	R	E4						
	R	IR	E5						
	R	IM	E6						
	IR	IM	E7						
	IR	R	F5						
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
dst←src									
LDCI dst, src	Ir	Irr	C3	-	-	-	-	-	-
dst←src									
r←r + 1;									
rr←rr + 1									
NOP			FF	-	-	-	-	-	-
OR dst, src	Note[a]		4[1	-	*	*	0	-	-

OPCODE MAP

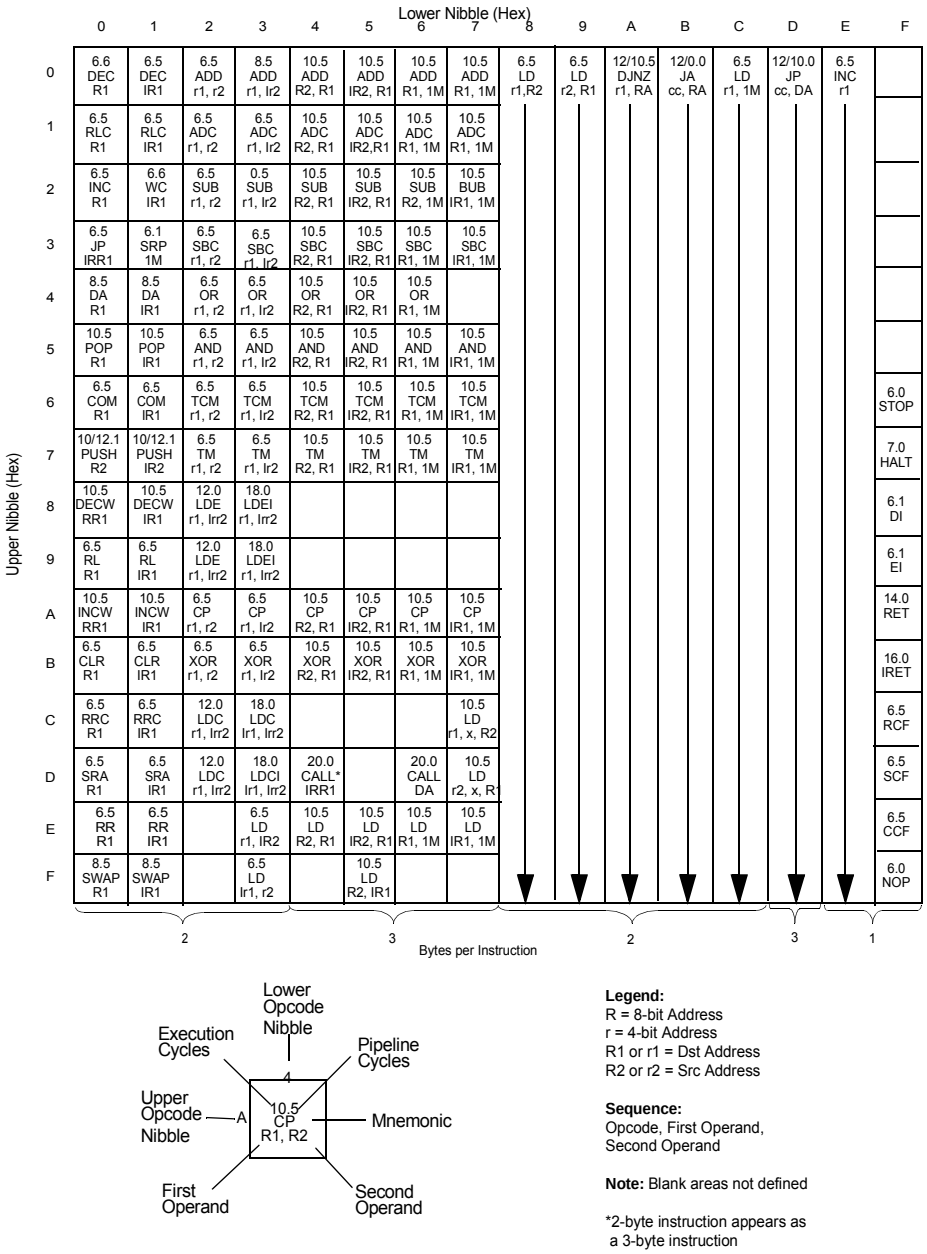
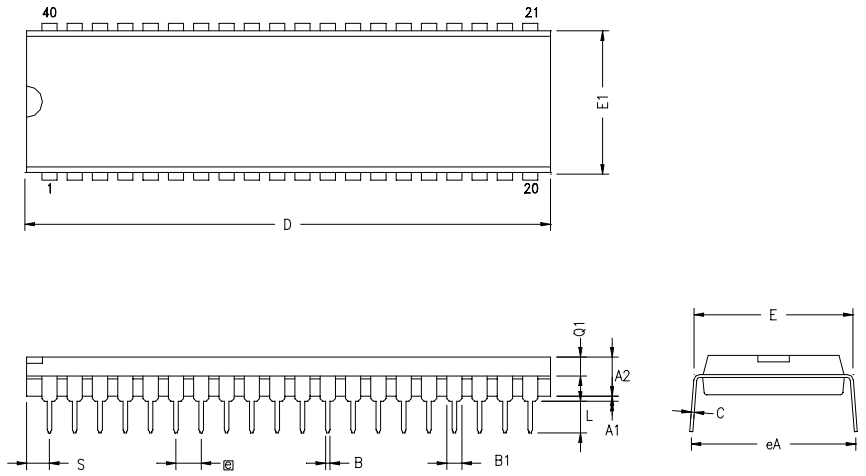


Figure 47. Opcode Map

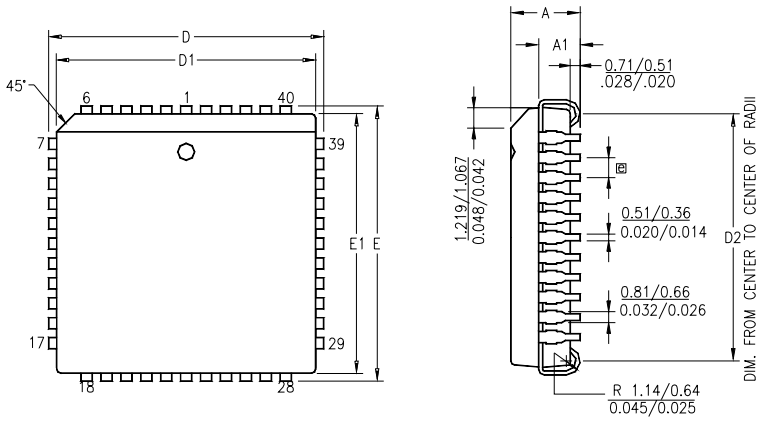
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

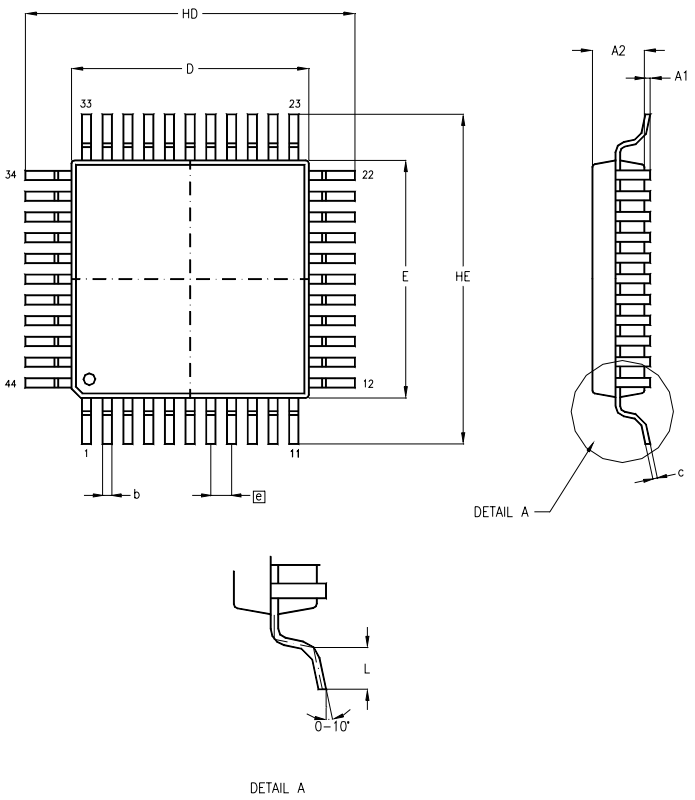
Figure 48. 40-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 BSC		0.050 BSC	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM
   INCH

Figure 49. 44-Pin PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 BSC		.0315 BSC	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 (.004")

Figure 50. 44-Pin LQFP Package Diagram

ORDERING INFORMATION

Z86E61			
16 MHz		**20 MHz**	
40-Pin DIP	**44-Pin PLCC**	**40-Pin DIP**	**44-Pin PLCC**
Z86E6116PSC	Z86E6116VSC	Z86E6120PSC	Z86E6120VSC
Z86E63			
16 MHz		**20 MHz**	
40-Pin DIP	**44-Pin PLCC**	**40-Pin DIP**	**44-Pin PLCC**
Z86E6316PSC	Z86E6316VSC	Z86E6320PSC	Z86E6320VSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

- Preferred Package
  P = Plastic DIP
  V = Plastic Chip Carrier
- Temperature
  S = 0°C to +70°C
- Speeds
  12 = 16 MHz
  16 = 20 MHz
- Environmental
  C = Plastic Standard

Example: