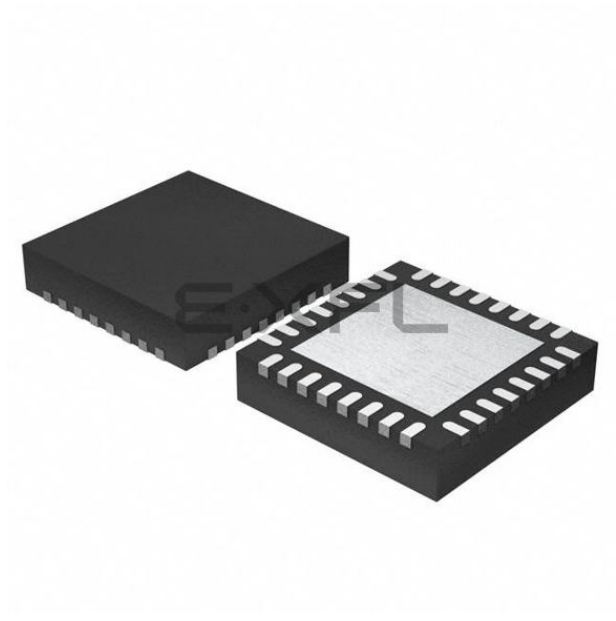

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	29
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc822m101jhi33e

5. Marking

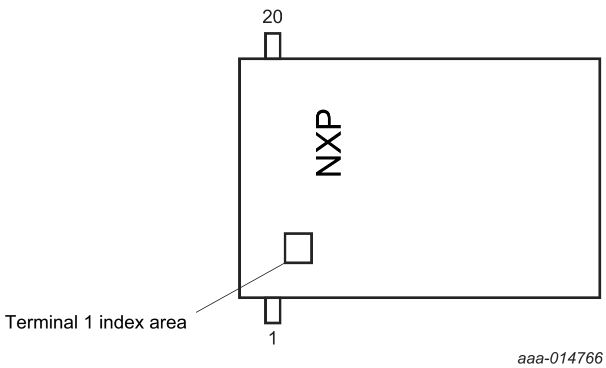


Fig 1. TSSOP20 package marking

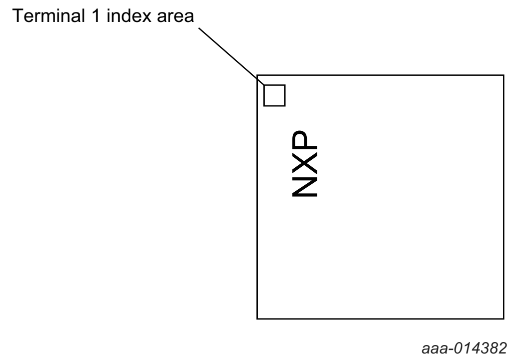


Fig 2. HVQFN33 package marking

The HVQFN33 packages typically have the following top-side marking:

82xJ

xx xx

yywwxR

The TSSOP20 packages typically have the following top-side marking:

LPC82x

Mx01J

xxxxxxxx

zzywwxR

In the last line, field ‘y’ or ‘yy’ states the year the device was manufactured. Field ‘ww’ states the week the device was manufactured during that year. Field ‘R’ states the chip revision.

- The WKT can be used for waking up the part from any reduced power mode, including Deep power-down mode, or for general-purpose timing.

8.20 Analog comparator (ACMP)

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 24.

The analog comparator output is a movable function and is assigned to a pin through the switch matrix. The comparator inputs and the voltage reference are enabled through the switch matrix.

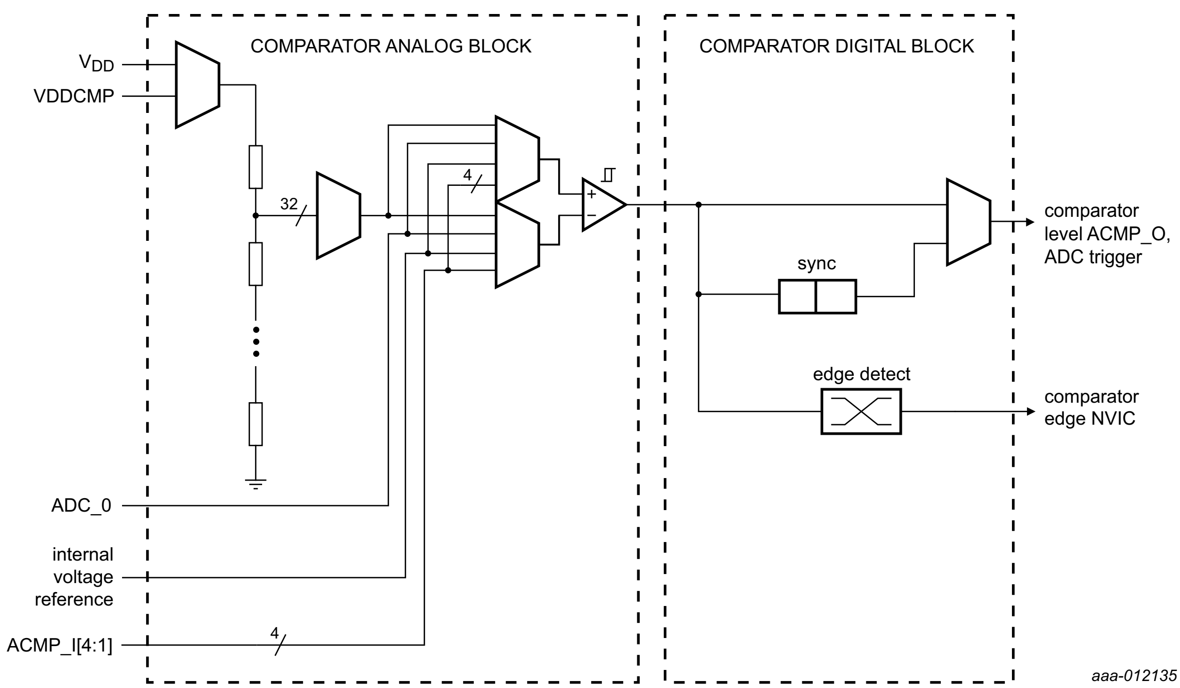


Fig 8. Comparator block diagram

8.20.1 Features

- Selectable 0 mV, 10 mV (± 5 mV), and 20 mV (± 10 mV), 40 mV (± 20 mV) input hysteresis.
- Two selectable external voltages (V_{DD} or VDDCMP on pin PIO0_6); fully configurable on either positive or negative input channel.
- Internal voltage reference from band gap selectable on either positive or negative input channel.
- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel.

8.23.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the ISP entry pin can be disabled without enabling CRP. For details, see the *LPC82x user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using the ISP entry pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION	
⚠	If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of the ISP entry pin for valid user code can be disabled. For details, see the *LPC82x user manual*.

8.23.4 APB interface

The APB peripherals are located on one APB bus.

8.23.5 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0+ to the flash memory, the main static RAM, the CRC, the DMA, the ROM, and the APB peripherals.

8.24 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The Micro Trace Buffer is implemented on the LPC82x.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC82x is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode on pins PIO0_0 to PIO0_3 (see Table 3).

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

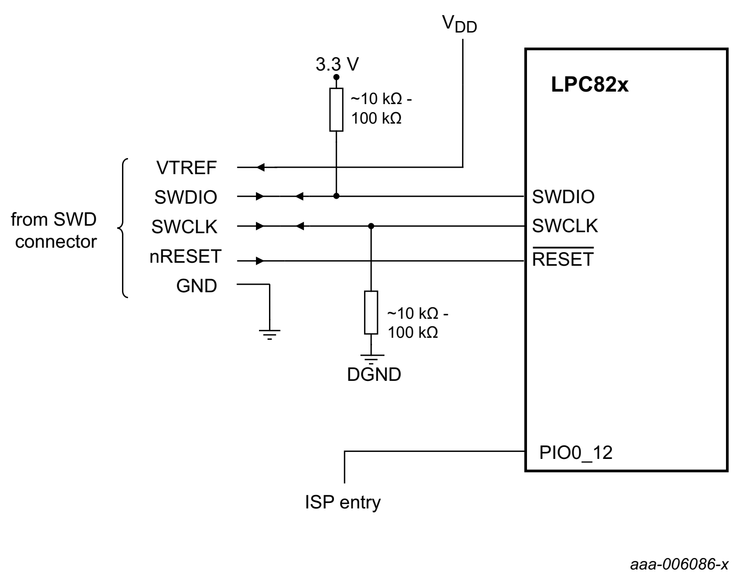


Fig 11. Connecting the SWD pins to a standard SWD connector

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)		[2]	–0.5	+4.6	V
V_{ref}	reference voltage	on pin VREFP		–0.5	V_{DD}	V
V_I	input voltage	5 V tolerant I/O pins; $V_{DD} \geq$ 1.8 V	[3][4]	–0.5	+5.5	V
		on I2C open-drain pins PIO0_10, PIO0_11	[5]	–0.5	+5.5	V
		3 V tolerant I/O pin PIO0_6	[6]	–0.5	+3.6	V
V_{IA}	analog input voltage		[7][8][9]	–0.5	+4.6	V
$V_{i(xtal)}$	crystal input voltage		[2]	–0.5	+2.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[10]	–65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model; all pins	[11]	-	3500	V
		charged device model; HVQFN33 package		-	1200	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 8) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_10 and PIO0_11 and except the 3 V tolerant pin PIO0_6.

[4] Including the voltage on outputs in 3-state mode.

[5] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[6] V_{DD} present or not present.

[7] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[8] If the comparator is configured with the common mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

[5] V_{DD} supply voltage must be present.

[6] Tri-state outputs go into tri-state mode in Deep power-down mode.

[7] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[8] Pull-up and pull-down currents are measured across the weak internal pull-up/pull-down resistors. See Figure 12.

[9] To V_{SS}.

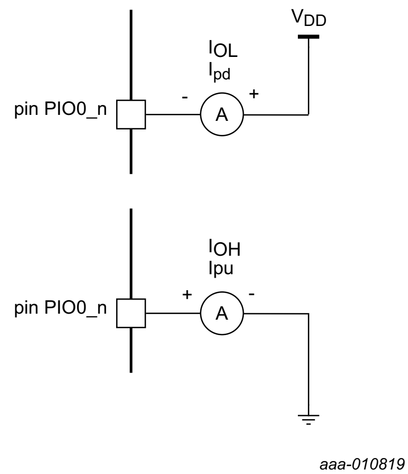
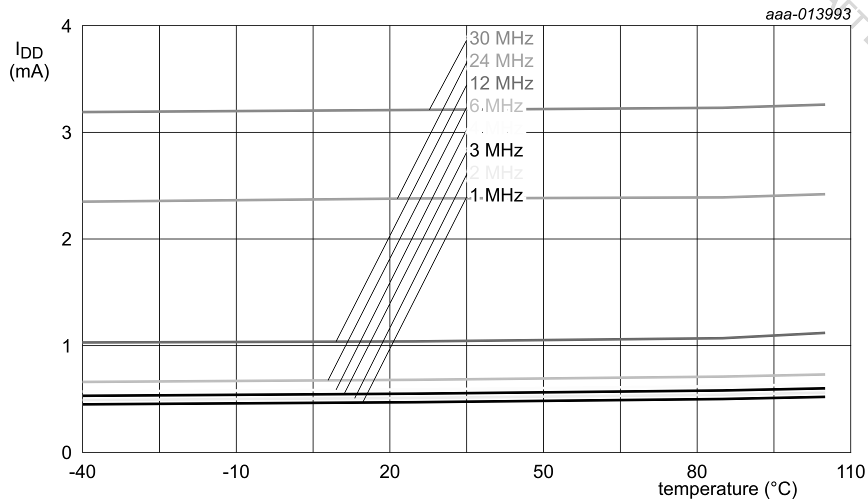


Fig 12. Pin input/output current measurement



Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL =0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

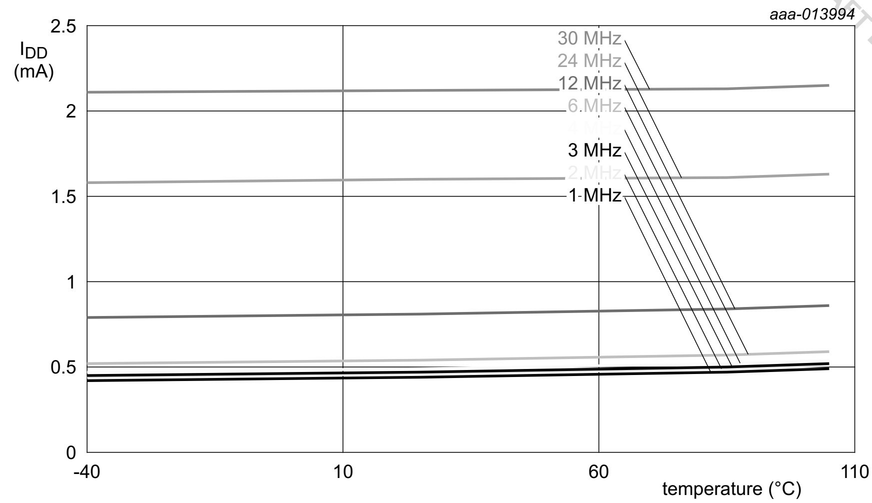
1 MHz - 6 MHz: external clock; IRC, PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz: IRC enabled; PLL enabled.

30 MHz: system oscillator enabled; PLL enabled.

Fig 14. Active mode: Typical supply current I_{DD} versus temperature



Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL =0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

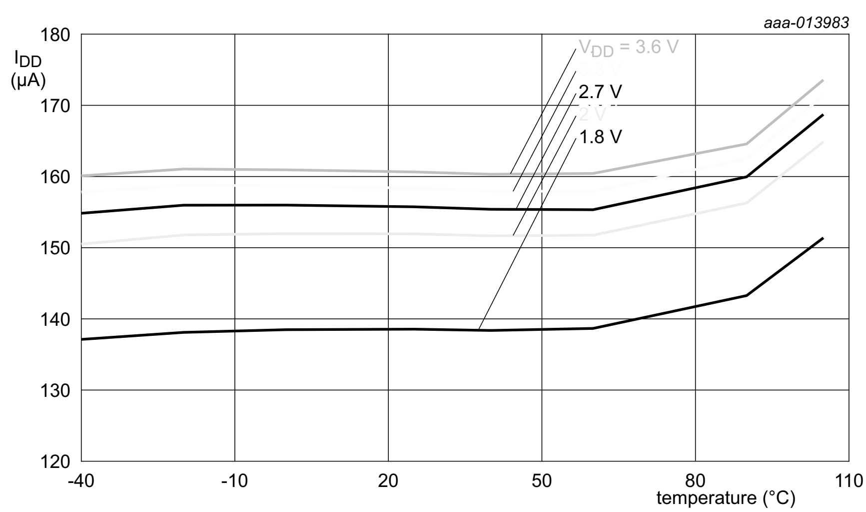
1 MHz - 6 MHz: external clock; IRC, PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz: IRC enabled; PLL enabled.

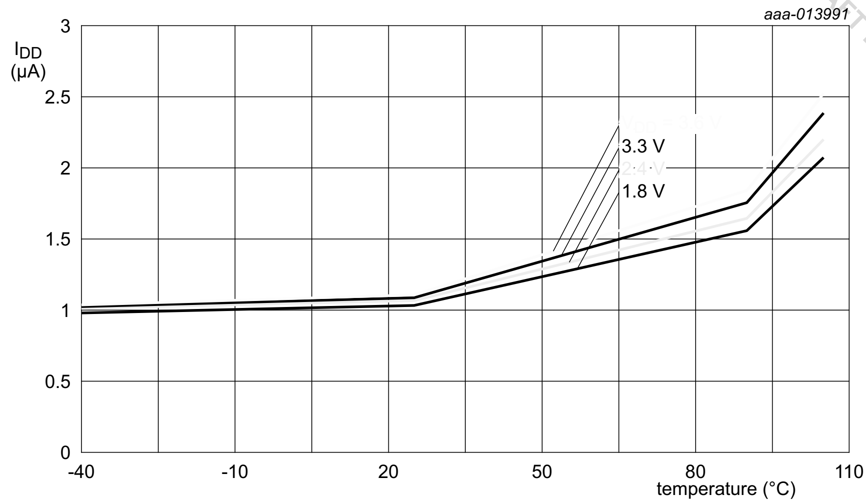
30 MHz: system oscillator enabled; PLL enabled.

Fig 15. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies



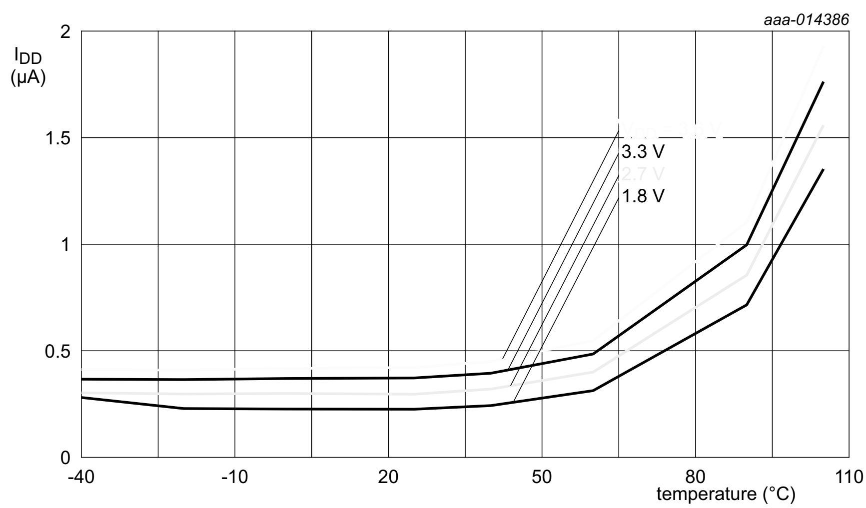
Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 16. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



WKT running with internal 10 kHz low-power oscillator.

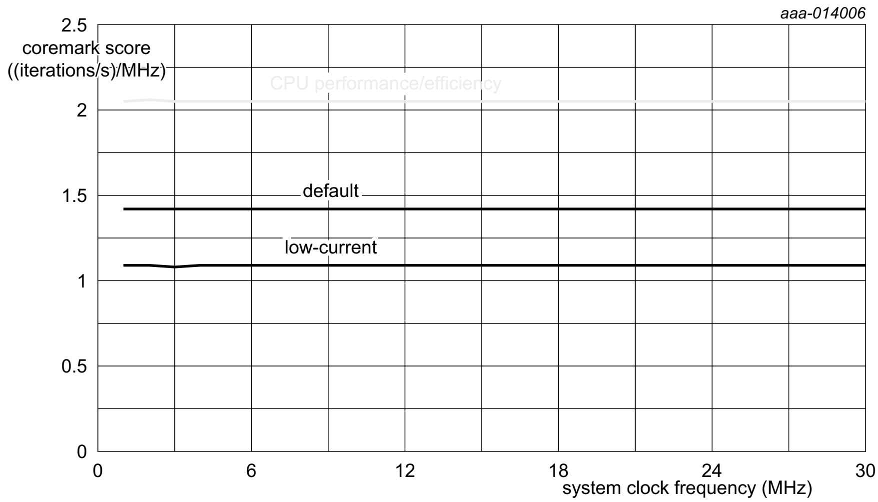
Fig 19. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (internal clock)



WKT running with external 10 kHz clock. Clock input waveform: square wave with rise time and fall time of 5 ns.

Fig 20. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (external 10 kHz input clock)

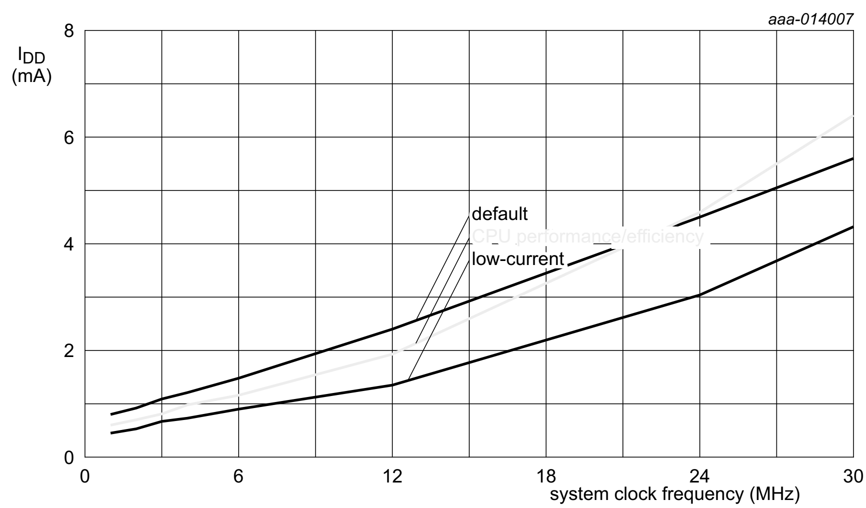
11.5 CoreMark data



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART and the SCT disabled in the SYSAHBCLKCTRL register; BOD disabled; internal pull-up resistors enabled. Measured with Keil uVision 5.10.

1 MHz - 6 MHz: external clock; IRC, PLL disabled.12 MHz: IRC enabled; PLL disabled. 24 MHz: IRC enabled; PLL enabled.30 MHz: system oscillator enabled; PLL enabled.

Fig 23. CoreMark score



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART and the SCT disabled in the SYSAHBCLKCTRL register; BOD disabled; internal pull-up resistors enabled. Measured with Keil uVision 5.10.

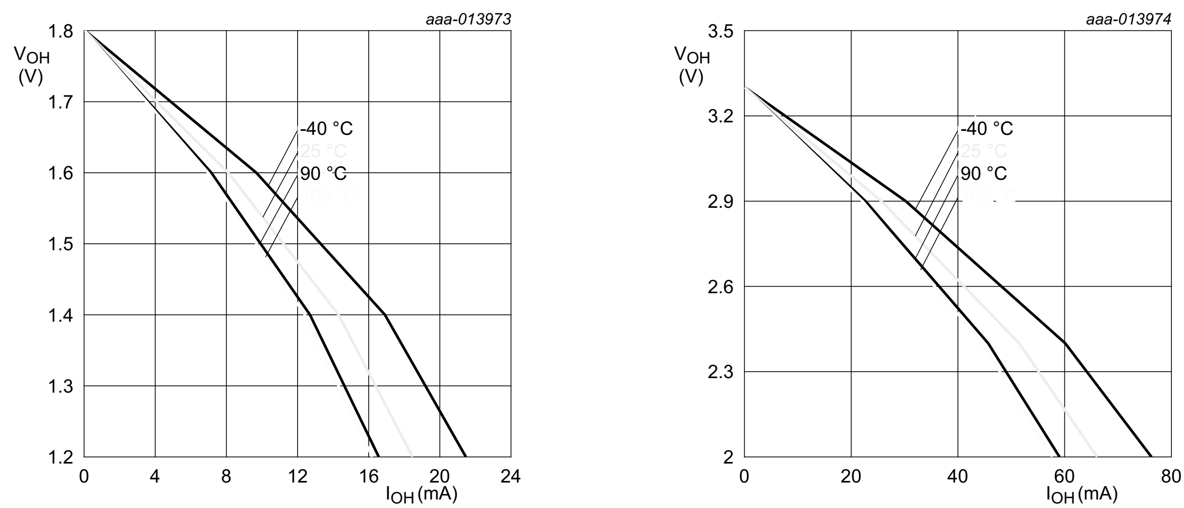
1 MHz - 6 MHz: external clock; IRC, PLL disabled.12 MHz: IRC enabled; PLL disabled.24 MHz: IRC enabled; PLL enabled.30 MHz: system oscillator enabled; PLL enabled.

Fig 24. Active mode: CoreMark power consumption I_{DD}

Table 10. Power consumption for individual analog and digital blocks *…continued*

Peripheral	Typical supply current in µA			Notes
	Main clock frequency =			
	n/a	12 MHz	30 MHz	
ADC	-	57	141	Digital controller only. Analog portion of the ADC disabled in the PDRUNCFG register.
	-	1990	2070	Combined analog and digital logic. ADC enabled in the PDRUNCFG register.
DMA	-	324	793	
CRC	-	34	85	-

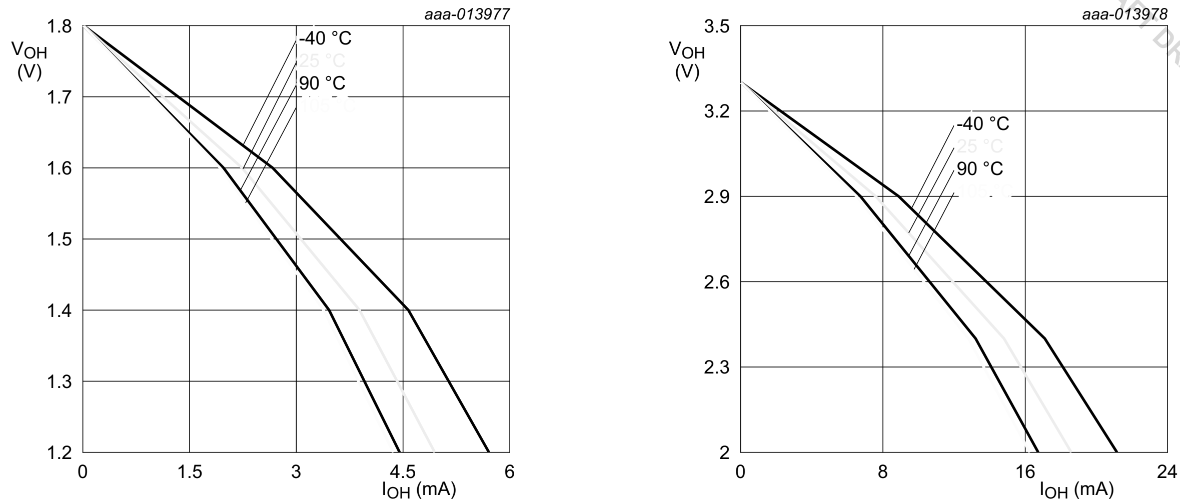
11.7 Electrical pin characteristics



Conditions: V_{DD} = 1.8 V; on pin PIO0_12.

Conditions: V_{DD} = 3.3 V; on pin PIO0_12.

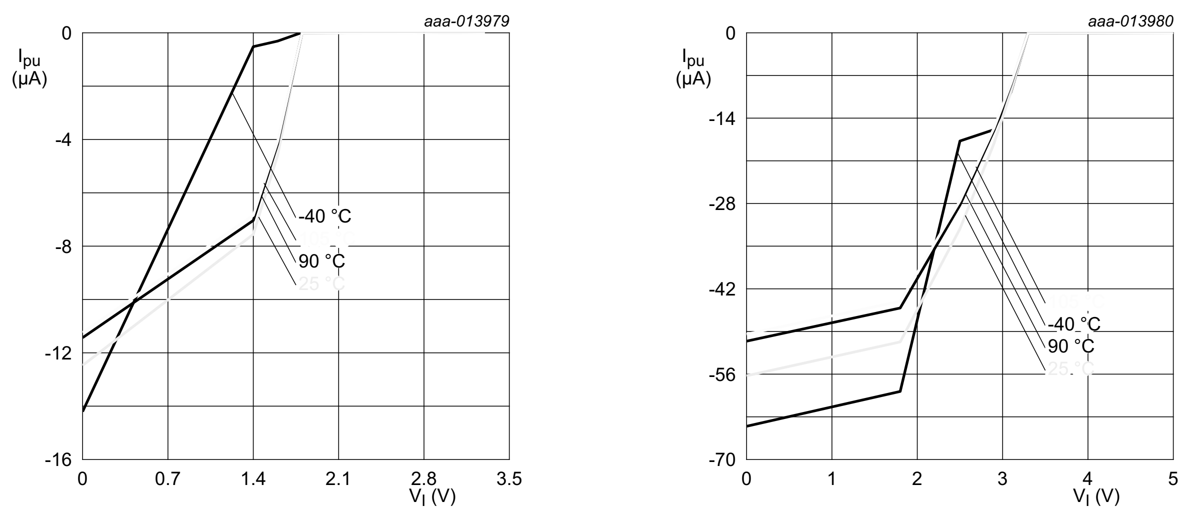
Fig 25. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}



Conditions: V_{DD} = 1.8 V; standard port pins.

Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 28. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 1.8 V; standard port pins.

Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 29. Typical pull-up current I_{PU} versus input voltage V_I

12.3.1 I/O pins

Table 15. Dynamic characteristics: I/O pins[1]

T_{amb} = –40 °C to +105 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	pin configured as output		3.0	-	5.0	ns
t_f	fall time	pin configured as output		2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

12.3.2 WKTCLKIN pin (wake-up clock input)

Table 16. Dynamic characteristics: WKTCLKIN pin

T_{amb} = –40 °C to +105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Max	Unit
f_{clk}	clock frequency	deep power-down mode and power-down mode	[1]	-	1	MHz
		deep-sleep, sleep, and active mode	[1]	-	10	MHz
t_{CHCX}	clock HIGH time	-		50	-	ns
t_{CLCX}	clock LOW time	-		50	-	ns

[1] Assuming a square-wave input clock.

12.3.3 SCTimer/PWM output timing

Table 17. SCTimer/PWM output dynamic characteristics

T_{amb} = –40 °C to 105 °C; 2.4 V <= V_{DD} <= 3.6 V; C_L = 10 pF. Simulated skew (over process, voltage, and temperature) of any two SCT output signals routed to standard I/O pins; sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(o)}$	output skew time	-	-	-	4	ns

12.3.4 I²C-bus

Table 18. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = –40 °C to +105 °C; values guaranteed by design.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	-	120	ns

13. Characteristics of analog peripherals

13.1 BOD

Table 21. BOD static characteristics[1]
T_{amb} = 25 °C.

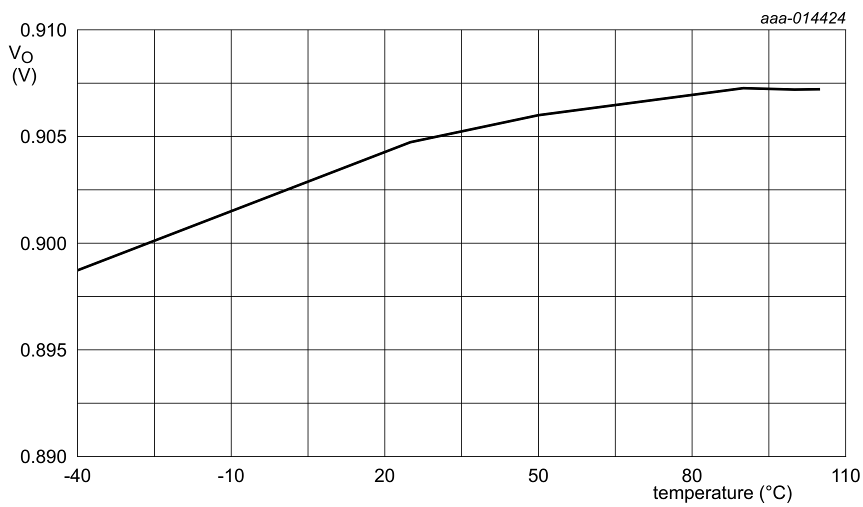
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1					
		assertion		-	2.25	-	V
		de-assertion		-	2.40	-	V
		interrupt level 2					
		assertion		-	2.54	-	V
		de-assertion		-	2.68	-	V
		interrupt level 3					
		assertion		-	2.85	-	V
		de-assertion		-	2.95	-	V
		reset level 0					
		assertion		-	1.46	-	V
		de-assertion		-	1.61	-	V
		reset level 1					
		assertion		-	2.05	-	V
		de-assertion		-	2.20	-	V
		reset level 2					
		assertion		-	2.34	-	V
		de-assertion		-	2.49	-	V
		reset level 3					
		assertion		-	2.63	-	V
		de-assertion		-	2.78	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *the* LPC82x *user manual*. Interrupt level 0 is reserved.

13.3 Comparator and internal voltage reference

Table 23. Internal voltage reference static and dynamic characteristics
T_{amb} = –40 °C to +105 °C; V_{DD} = 3.3 V; hysteresis disabled in the comparator CTRL register.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_O	output voltage	T_{amb} = 25 °C to 105°C		860	-	940	mV
		T_{amb} = 25 °C			904		mV
$t_{s(pu)}$	power-up settling time	to 99% of V_O		-	-	<tbd>	µs



V_{DD} = 3.3 V; characterized through bench measurements on typical samples.

Fig 39. Typical internal voltage reference output voltage

Table 24. Comparator characteristics
T_{amb} = –40 °C to +105 °C unless noted otherwise; V_{DD} = 1.8 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{ref(cmp)}$	comparator reference voltage	pin PIO0_6/VDDCMP configured for function VDDCMP		1.5	-	3.6	V
I_{DD}	supply current	VP > VM; T_{amb} = 25 °C; V_{DD} = 3.3 V	[2]	-	90	-	µA
		VM > VP; T_{amb} = 25 °C; V_{DD} = 3.3 V	[2]	-	60	-	µA
V_{IC}	common-mode input voltage			0	-	V_{DD}	V
DV_O	output voltage variation			0	-	V_{DD}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V; V_{DD} = 2.4 V; T_{amb} = 105 °C	[2]	-	+/- 4	-	mV
		V_{IC} = 1.5 V; V_{DD} = 2.4 V; T_{amb} = 105 °C	[2]	-	+/- 2	-	mV
		V_{IC} = 2.9 V; V_{DD} = 2.4 V; T_{amb} = 105 °C	[2]	-	+/- 4	-	mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process; V_{DD} = 3.3 V; T_{amb} = 25 °C		-	13	-	µs

Table 24. Comparator characteristics *…continued*

T_{amb} = –40 °C to +105 °C unless noted otherwise; V_{DD} = 1.8 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PD}	propagation delay	HIGH to LOW; V_{DD} = 3.0 V; T_{amb} = 105 °C					
		V_{IC} = 0.1 V; 100 mV overdrive input	[1][2][4]	-	140	-	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1][2]	-	190	-	ns
		V_{IC} = 1.5 V; 100 mV overdrive input	[1][2][4]	-	130	-	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1][2]	-	120	-	ns
		V_{IC} = 2.9 V; 100 mV overdrive input	[1][2][4]	-	220	-	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1][2]	-	80	-	ns
t_{PD}	propagation delay	LOW to HIGH; V_{DD} = 3.0 V; T_{amb} = 105 °C					
		V_{IC} = 0.1 V; 100 mV overdrive input	[1][2][4]	-	240	-	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1][2]	-	60	-	ns
		V_{IC} = 1.5 V; 100 mV overdrive input	[1][2][4]	-	160	-	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1][2]	-	150	-	ns
		V_{IC} = 2.9 V; 100 mV overdrive input	[1][2][4]	-	150	-	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1][2]	-	260	-	ns
V_{hys}	hysteresis voltage	positive hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V; T_{amb} = 105 °C; settings:	[3]	-		-	
		5 mV			6		mV
		10 mV		-	11	-	mV
		20 mV		-	23	-	mV
V_{hys}	hysteresis voltage	negative hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V; T_{amb} = 105 °C; settings:	[1][3]				
		5 mV		-	10	-	mV
		10 mV		-	15	-	mV
		20 mV		-	27	-	mV
R_{lad}	ladder resistance	-		-	1	-	MΩ

[1] C_L = 10 pF

[2] Characterized on typical samples, not tested in production.

[3] Input hysteresis is relative to the reference input channel and is software programmable.

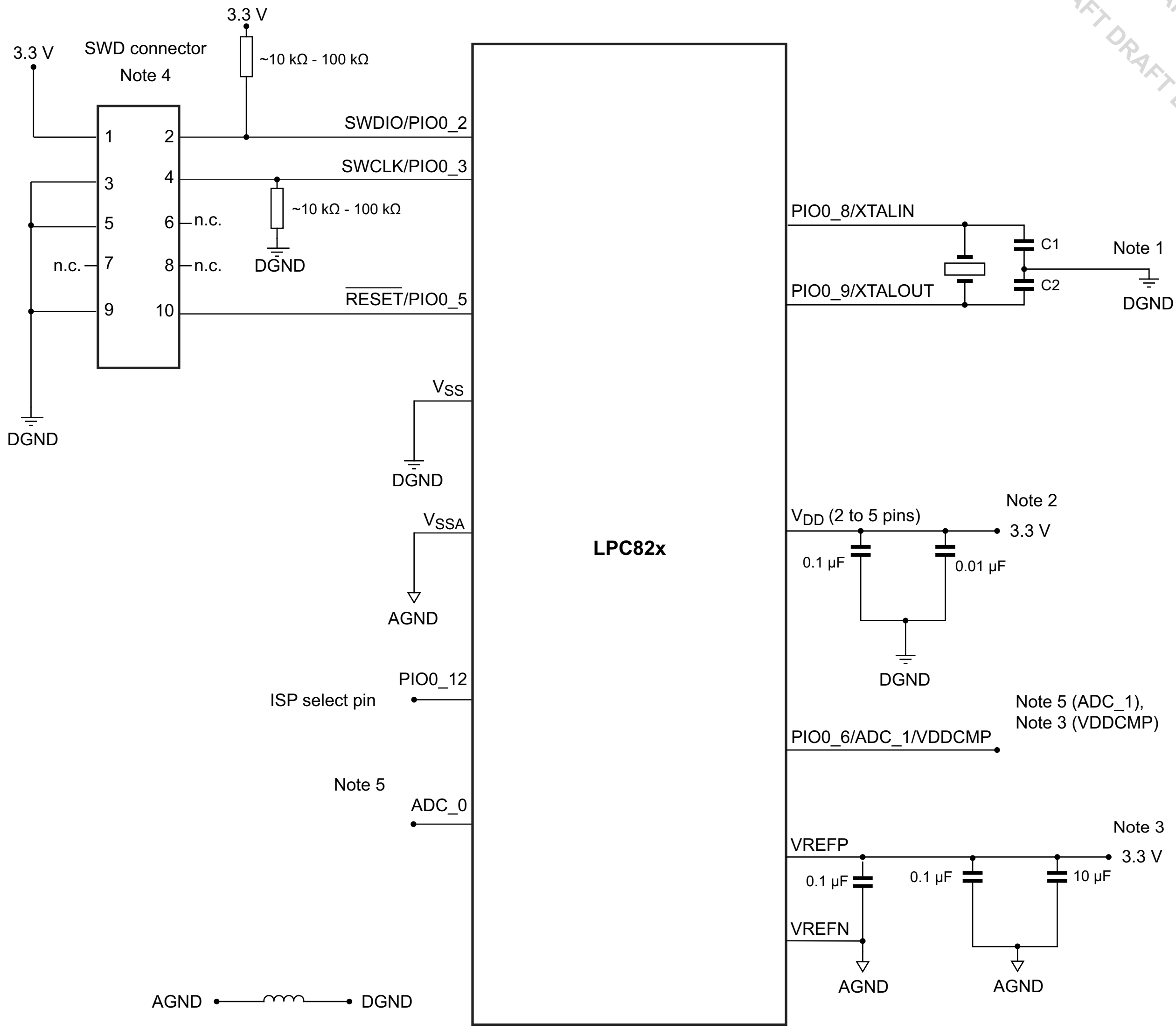
[4] 100 mV overdrive corresponds to a square wave from 50 mV below the reference (V_{IC}) to 50 mV above the reference.

Table 25. Comparator voltage ladder dynamic characteristics

T_{amb} = –40 °C to +105 °C; V_{DD} = 1.8 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	17	-	μs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1]	-	18	-	μs

[1] Characterized on typical samples, not tested in production.



(1) See Section 14.1 "XTAL input" for the values of C1 and C2.

(2) Position the decoupling capacitors of 0.1 μF and 0.01 μF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(3) Position the decoupling capacitors of 0.1 μF as close as possible to the VREFN and V_{DD} pins. The 10 μF bypass capacitor filters the power line. Tie VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(4) Uses the ARM 10-pin interface for SWD.

(5) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 4.

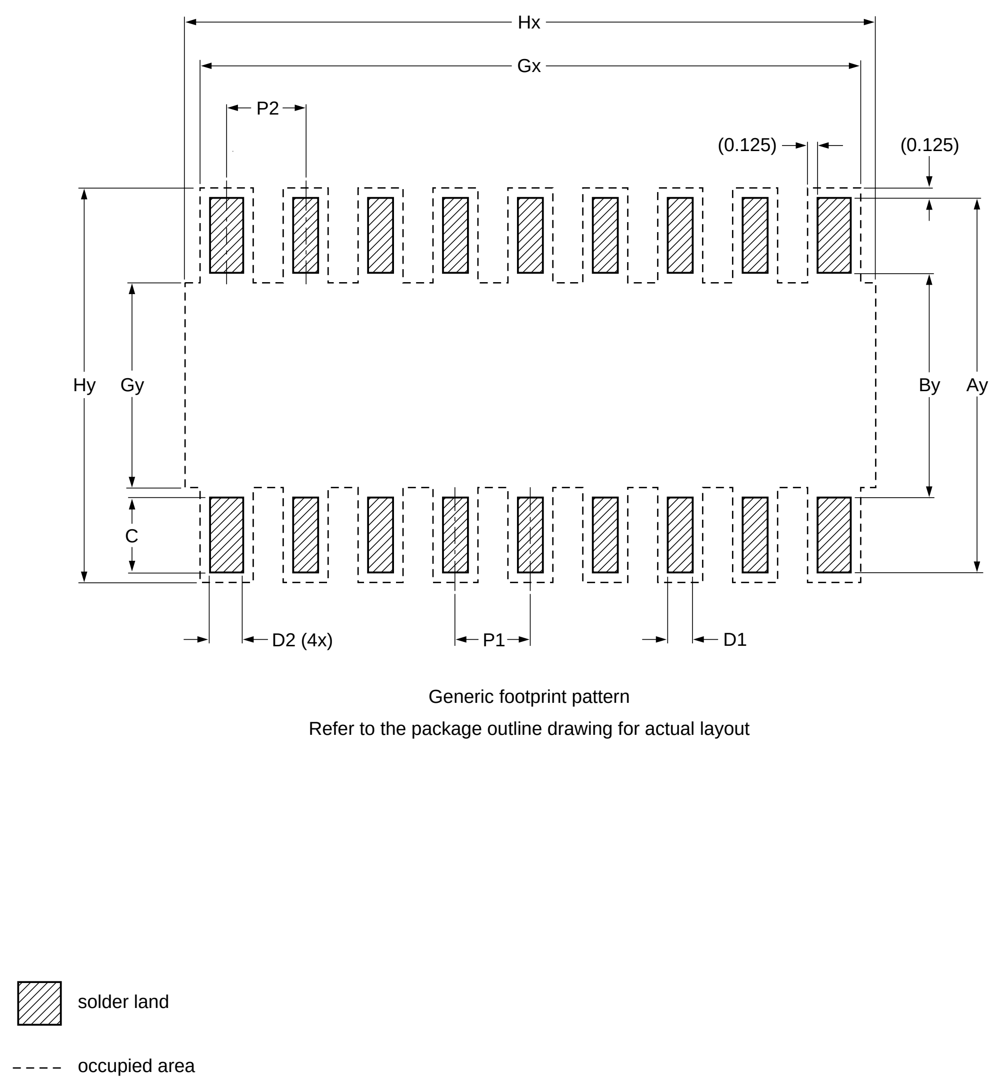
Fig 42. Power, clock, and debug connections

14.4 Termination of unused pins

Table 29 shows how to terminate pins that are **not** used in the application. In many cases, unused pins may should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

16. Soldering

Footprint information for reflow soldering of TSSOP20 package **SOT360-1**



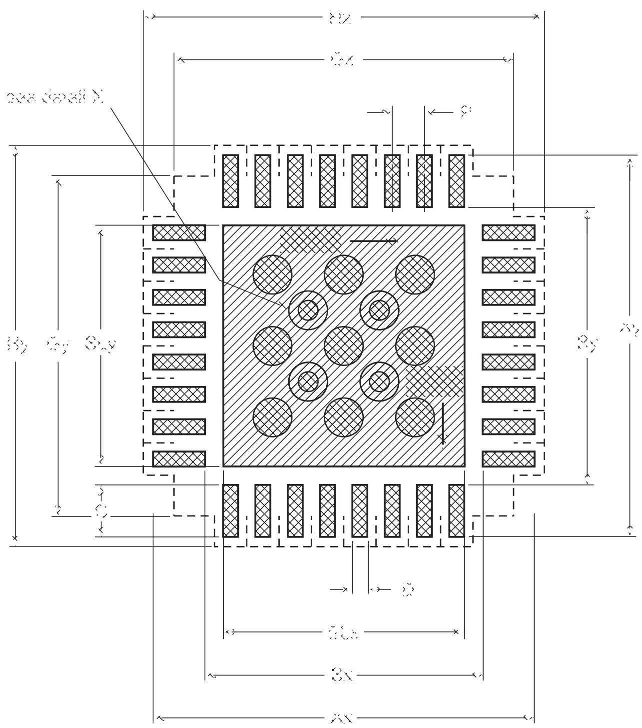
DIMENSIONS in mm

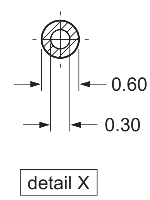
P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	6.900	5.300	7.300	7.450

sot360-1_fr

Fig 45. Reflow soldering of the TSSOP20 package

Footprint information for reflow soldering of HVQFN33 package





solder land

solder paste

---- occupied area

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

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Fig 46. Reflow soldering of the HVQFN33 package (5x5)

17. Abbreviations

Table 31. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General-Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SMBus	System Management Bus
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

18. References

[1] User manual UM10800.

[2] Errata sheet ES_LPC82XM.

[3] I2C-bus specification *UM10204*.

[4] Technical note ADC design guidelines: http://www.nxp.com/documents/technical_note/TN00009.pdf