Renesas Electronics America Inc - R5F21368SNFP#50 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21368snfp-50

1.1.2 Specifications

Tables 1.1 and 1.2 outline Specifications.

Table 1.1 Specifications (1)

Item	Function	Description
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (CPU clock = 20 MHz, VCC = 2.7 V to 5.5 V) 200 ns (CPU clock = 5 MHz, VCC = 1.8 V to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, data flash	Refer to **Table 1.3 Product List**.
Voltage detection	Voltage detection circuit	• Power-on reset • Voltage detection with three check points (the detection levels for voltage detection 0 and voltage detection 1 can be selected.)
I/O ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 59, selectable pull-up resistor • High current drive ports: 59
Clock	Clock generation circuits	• 4 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Divided by 1, 2, 4, 8, or 16 can be selected • Low-power mode: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Number of interrupt vectors: 69 • External interrupt inputs: 9 (INT × 5, key input × 4) • Priority levels: 7
Event link controller (ELC)		• Events output from peripheral functions can be linked to events input to different peripheral functions. (30 sources × 10 types of event link operations) • Events can be handled independently from interrupt requests.
Watchdog timer		• 14 bits × 1 • Selectable reset start function • Selectable low-speed on-chip oscillator for the watchdog timer
DTC (data transfer controller)		• 1 channel • Activation sources: 27 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timers RJ_0	16 bits × 1: 1 circuit integrated on-chip Timer mode (periodic timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB2_0	16 bits × 1: 1 circuit integrated on-chip Timer mode (periodic timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timers RC_0	16 bits (with 4 capture/compare registers) × 1: 1 circuit integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)
	Timer RE2	8 bits × 1 Compare match timer mode, real-time clock mode

1.2 Product List

Table 1.3 lists product information. Figure 1.1 shows the Product Part Number Structure.

Table 1.3 Product List **Current of Dec 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F21368SNFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	N version
R5F2136ASNFP	96 Kbytes		8 Kbytes		
R5F2136CSNFP	128 Kbytes		10 Kbytes		
R5F21368SNFA	64 Kbytes		6 Kbytes	PLQP0064GA-A	
R5F2136ASNFA	96 Kbytes		8 Kbytes		
R5F2136CSNFA	128 Kbytes		10 Kbytes		
R5F21368SDFP	64 Kbytes		6 Kbytes	PLQP0064KB-A	D version
R5F2136ASDFP	96 Kbytes		8 Kbytes		
R5F2136CSDFP	128 Kbytes		10 Kbytes		
R5F21368SDFA	64 Kbytes		6 Kbytes	PLQP0064GA-A	
R5F2136ASDFA	96 Kbytes		8 Kbytes		
R5F2136CSDFA	128 Kbytes		10 Kbytes		

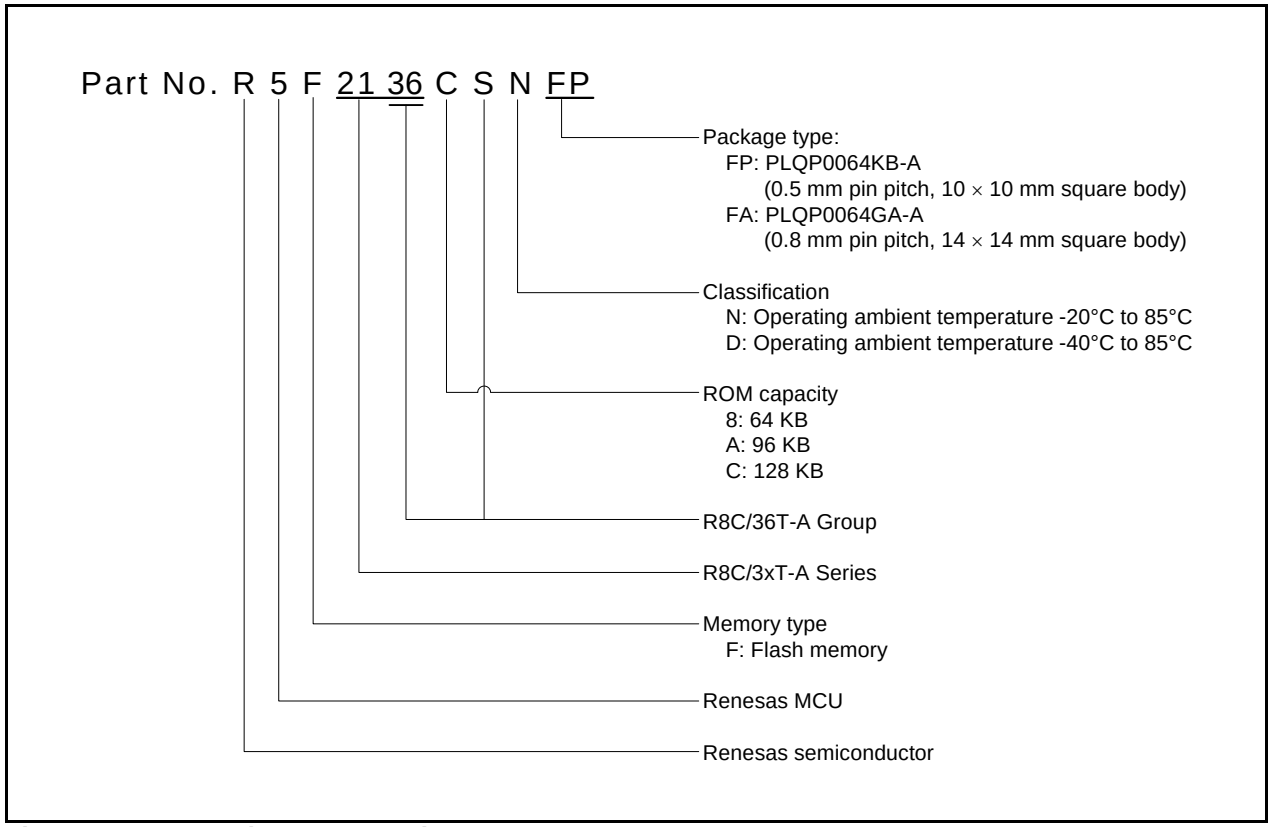


Figure 1.1 Product Part Number Structure

1.5 Pin Functions

Tables 1.7 and 1.8 list Pin Functions.

Table 1.7 Pin Functions (1)

Item	Pin Name	I/O	Description
Power supply input	VCC, VSS	—	Apply 1.8 V through 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply input for the A/D converter. Connect a capacitor between pins AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Applying a low level to this pin resets the MCU.
MODE	MODE	I	Connect this pin to the VCC pin via a resistor.
XIN clock input	XIN	I	I/O for the XIN clock generation circuit. Connect a ceramic resonator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	I/O for the XCIN clock generation circuit. Connect a crystal oscillator between pins XCIN and XCOUT. (1) To use an external clock, input it to the XCOUT pin and leave the XCIN pin open.
XCIN clock output	XCOUT	I/O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$	I	$\overline{\text{INT}}$ interrupt input.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input.
Timer RJ_0	TRJIO_0	I/O	Input/output for timer RJ.
	TRJO_0	O	Output for timer RJ.
Timer RB2_0	TRBO_0	O	Output for timer RB2.
Timer RC_0	TRCCLK_0	I	External clock input.
	TRCTRG_0	I	External trigger input.
	TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0	I/O	Input/output for timer RC.
Timer RE2	TMRE2O	O	Divided clock output.
Serial interface (UART0)	CLK_0, CLK_1	I/O	Transfer clock input/output.
	RXD_0, RXD_1	I	Serial data input.
	TXD_0, TXD_1	O	Serial data output.
Serial interface (UART2)	$\overline{\text{CTS2}}$	I	Input for transmission control.
	$\overline{\text{RTS2}}$	O	Output for reception control.
	SCL2	I/O	I^2C mode clock input/output.
	SDA2	I/O	I^2C mode data input/output.
	RXD2	I	Serial data input.
	TXD2	O	Serial data output.
	CLK2	I/O	Transfer clock input/output.
Synchronous serial communication unit (SSU_0)	SSI_0	I/O	Data input/output.
	$\overline{\text{SCS\_0}}$	I/O	Chip-select input/output.
	$\overline{\text{SSCK\_0}}$	I/O	Clock input/output.
	SSO_0	I/O	Data input/output.
I^2C bus (I^2C_0)	SCL_0	I/O	Clock input/output.
	SDA_0	I/O	Data input/output.
Reference voltage input	VREF	I	Reference voltage input for the A/D converter.

Note:
1. Contact the oscillator manufacturer for oscillation characteristics.

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 through R3. R0 can be split into high-order (R0H) and low-order (R0L) registers to be used separately as 8-bit data registers. The same applies to R1H and R1L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). Similarly, R3 and R1 can be used as a 32-bit data register.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 functions in the same manner as A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

PC is a 20-bit register that indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of the FLG register is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated in the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. It must only be set to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0. Otherwise it is set to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value. Otherwise it is set to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow. Otherwise it is set to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts. Interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction for a software interrupt numbered from 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns eight processor interrupt priority levels from 0 to 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

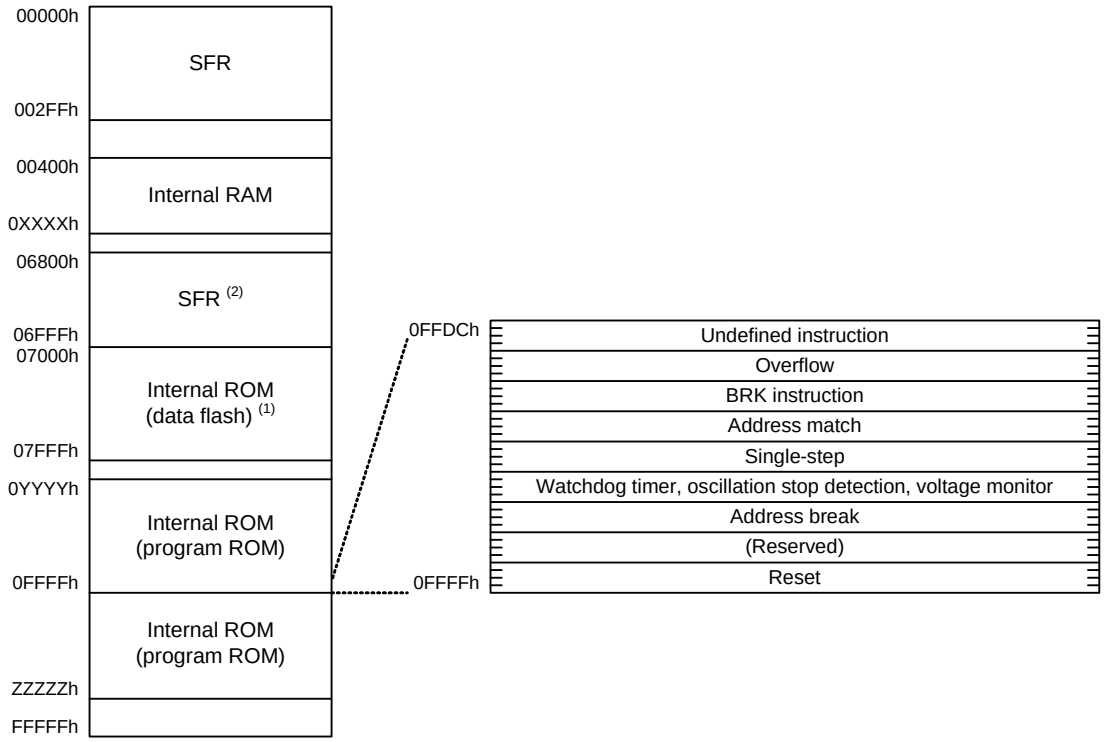
2.8.10 Reserved Bit

The write value must be 0. The read value is undefined.

3. Address Space

3.1 Memory Map

Figure 3.1 shows the Memory Map. The R8C/36T-A Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. Up to 32 Kbytes of the internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. The area in excess of 32 Kbytes is allocated at higher addresses, beginning with address 10000h. For example, a 64-Kbyte internal ROM is allocated at addresses 08000h to 17FFFh.
The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated at addresses 07000h to 07FFFh.
The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM is allocated at addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated at addresses 00000h to 02FFFh and addresses 06800h to 06FFFh. Peripheral function control registers are allocated here. All unallocated locations within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. Addresses 06800h to 06FFFh are used for the ELC, DTC, and TSCU SFR areas.
3. The blank areas are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM	
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh
R5F21368SNFP/FA, R5F21368SDFP/FA	64 Kbytes	08000h	17FFFh	6 Kbytes	01BFFh
R5F21368SNFP/FA, R5F21368SDFP/FA	96 Kbytes	08000h	1FFFFh	8 Kbytes	023FFh
R5F21368SNFP/FA, R5F21368SDFP/FA	128 Kbytes	08000h	27FFFh	10 Kbytes	02BFFh

Figure 3.1 Memory Map

3.2 Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 3.1 to 3.16 list the SFR Information. Table 3.17 lists the ID code Area, Option Function Select Area.

Table 3.1 SFR Information (1) (1)

Address	Symbol	Register Name	After Reset	Remarks
00000h				
00001h				
00002h				
00003h				
00004h	PM0	Processor Mode Register 0	00h	
00005h	PM1	Processor Mode Register 1	10000000b	
00006h				
00007h	PRCR	Protect Register	00h	
00008h	CM0	System Clock Control Register 0	00101000b	
00009h	CM1	System Clock Control Register 1	00100000b	
0000Ah	OCD	Oscillation Stop Detection Register	00h	
0000Bh	CM3	System Clock Control Register 3	00h	
0000Ch	CM4	System Clock Control Register 4	00000001b	
0000Dh				
0000Eh				
0000Fh				
00010h	CPSRF	Clock Prescaler Reset Flag	00h	
00011h				
00012h	FRA0	High-Speed On-Chip Oscillator Control Register 0	00h	
00013h				
00014h	FRA2	High-Speed On-Chip Oscillator Control Register 2	00h	
00015h				
00016h				
00017h				
00018h				
00019h				
0001Ah				
0001Bh				
0001Ch				
0001Dh				
0001Eh				
0001Fh				
00020h	RISR	Reset Interrupt Select Register	10000000b or 00000000b	(Note 2)
00021h	WDTR	Watchdog Timer Reset Register	FFh	
00022h	WDTS	Watchdog Timer Start Register	FFh	
00023h	WDTC	Watchdog Timer Control Register	01111111b	
00024h	CSPR	Count Source Protection Mode Register	10000000b or 00000000b	(Note 2)
00025h				
00026h				
00027h				
00028h	RSTFR	Reset Source Determination Register	00XXXXXXb	
00029h				
0002Ah				
0002Bh				
0002Ch	SVDC	STBY VDC Power Control Register	00h	
0002Dh				
0002Eh				
0002Fh				
00030h	CMPA	Voltage Monitor Circuit Control Register	00h	
00031h	VCAC	Voltage Monitor Circuit Edge Select Register	00h	
00032h	OCVREFCR	On-Chip Reference Voltage Control Register	00h	
00033h				
00034h	VCA2	Voltage Detection Register 2	00000000b or 00100000b	(Note 3)
00035h				
00036h	VD1LS	Voltage Detection 1 Level Select Register	00000111b	
00037h				
00038h	VW0C	Voltage Monitor 0 Circuit Control Register	1100XX10b or 1100XX11b	(Note 3)
00039h	VW1C	Voltage Monitor 1 Circuit Control Register	10001010b	

X: Undefined

Notes:

1. The blank areas are reserved. No access is allowed.
2. Depends on the CSPROINI bit in the OFS register.
3. Depends on the LVDASI bit in the OFS register.

Table 3.5 SFR Information (5) (1)

Address	Symbol	Register Name	After Reset	Remarks
000FAh				
000FBh				
000FCh				
000FDh				
000FEh				
000FFh				
00100h				
00101h				
00102h				
00103h				
00104h				
00105h				
00106h				
00107h				
00108h				
00109h				
0010Ah				
0010Bh				
0010Ch				
0010Dh				
0010Eh				
0010Fh				
00110h	TRJ_0	Timer RJ_0 Counter Register	FFFFh	
00111h				
00112h	TRJCR_0	Timer RJ_0 Control Register	00h	
00113h	TRJIOC_0	Timer RJ_0 I/O Control Register	00h	
00114h	TRJMR_0	Timer RJ_0 Mode Register	00h	
00115h	TRJISR_0	Timer RJ_0 Event Pin Select Register	00h	
00116h				
00117h				
00118h				
00119h				
0011Ah				
0011Bh				
0011Ch				
0011Dh				
0011Eh				
0011Fh				
00120h				
00121h				
00122h				
00123h				
00124h				
00125h				
00126h				
00127h				
00128h				
00129h				
0012Ah				
0012Bh				
0012Ch				
0012Dh				
0012Eh				
0012Fh				
00130h	TRBCR_0	Timer RB2_0 Control Register	00h	
00131h	TRBOCR_0	Timer RB2_0 One-Shot Control Register	00h	
00132h	TRBIOC_0	Timer RB2_0 I/O Control Register	00h	
00133h	TRBMR_0	Timer RB2_0 Mode Register	00h	
00134h	TRBPRE_0	Timer RB2_0 Prescaler Register	FFh	
00135h	TRBPR_0	Timer RB2_0 Primary Register	FFh	
00136h	TRBSC_0	Timer RB2_0 Secondary Register	FFh	
00137h	TRBIR_0	Timer RB2_0 Interrupt Request Register	00h	
00138h	TRCCNT_0	Timer RC_0 Counter	0000h	
00139h				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.7 SFR Information (7) (1)

Address	Symbol	Register Name	After Reset	Remarks
0017Ah	TREIFR	Timer RE2 Interrupt Flag Register	00h	
0017Bh	TREIER	Timer RE2 Interrupt Enable Register	00h	
0017Ch	TREAMN	Timer RE2 Alarm Minute Register	00h	
0017Dh	TREAHR	Timer RE2 Alarm Hour Register	00h	
0017Eh	TREAWK	Timer RE2 Alarm Day-of-the-Week Register	00h	
0017Fh	TREPRC	Timer RE2 Protect Register	00h	
00180h to 001FFh				
00200h	AD0	A/D Register 0	00h	
00201h			00h	
00202h	AD1	A/D Register 1	00h	
00203h			00h	
00204h	AD2	A/D Register 2	00h	
00205h			00h	
00206h	AD3	A/D Register 3	00h	
00207h			00h	
00208h	AD4	A/D Register 4	00h	
00209h			00h	
0020Ah	AD5	A/D Register 5	00h	
0020Bh			00h	
0020Ch	AD6	A/D Register 6	00h	
0020Dh			00h	
0020Eh	AD7	A/D Register 7	00h	
0020Fh			00h	
00210h				
00211h				
00212h				
00213h				
00214h	ADMOD	A/D Mode Register	00h	
00215h	ADINSEL	A/D Input Select Register	11000000b	
00216h	ADCON0	A/D Control Register 0	00h	
00217h	ADCON1	A/D Control Register 1	00h	
00218h				
00219h				
0021Ah				
0021Bh				
0021Ch				
0021Dh				
0021Eh				
0021Fh				
00220h				
00221h				
00222h				
00223h				
00224h				
00225h				
00226h				
00227h				
00228h	INTCMP	Comparator B Control Register 0	00h	
00229h				
0022Ah				
0022Bh				
0022Ch				
0022Dh				
0022Eh				
0022Fh				
00230h	INTEN	External Input Enable Register 0	00h	
00231h	INTEN1	External Input Enable Register 1	00h	
00232h	INTF	INT Input Filter Select Register 0	00h	
00233h	INTF1	INT Input Filter Select Register 1	00h	
00234h	INTPOL	INT Input Polarity Switch Register	00h	
00235h				
00236h	KIEN	Key Input Interrupt Enable Register	00h	
00237h				
00238h	MSTCR0	Module Standby Control Register 0	00h	
00239h	MSTCR1	Module Standby Control Register 1	00h	

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.14 SFR Information (14) (1)

Address	Symbol	Register Name	After Reset	Remarks
06C4Ah	DTCCT1	DTC Transfer Count Register 1	XXh	
06C4Bh	DTRLD1	DTC Transfer Count Reload Register 1	XXh	
06C4Ch	DTSAR1	DTC Source Address Register 1	XXXXh	
06C4Dh				
06C4Eh	DTDAR1	DTC Destination Address Register 1	XXXXh	
06C4Fh				
06C50h	DTCCR2	DTC Control Register 2	XXh	
06C51h	DTBLS2	DTC Block Size Register 2	XXh	
06C52h	DTCCT2	DTC Transfer Count Register 2	XXh	
06C53h	DTRLD2	DTC Transfer Count Reload Register 2	XXh	
06C54h	DTSAR2	DTC Source Address Register 2	XXXXh	
06C55h				
06C56h	DTDAR2	DTC Destination Address Register 2	XXXXh	
06C57h				
06C58h	DTCCR3	DTC Control Register 3	XXh	
06C59h	DTBLS3	DTC Block Size Register 3	XXh	
06C5Ah	DTCCT3	DTC Transfer Count Register 3	XXh	
06C5Bh	DTRLD3	DTC Transfer Count Reload Register 3	XXh	
06C5Ch	DTSAR3	DTC Source Address Register 3	XXXXh	
06C5Dh				
06C5Eh	DTDAR3	DTC Destination Address Register 3	XXXXh	
06C5Fh				
06C60h	DTCCR4	DTC Control Register 4	XXh	
06C61h	DTBLS4	DTC Block Size Register 4	XXh	
06C62h	DTCCT4	DTC Transfer Count Register 4	XXh	
06C63h	DTRLD4	DTC Transfer Count Reload Register 4	XXh	
06C64h	DTSAR4	DTC Source Address Register 4	XXXXh	
06C65h				
06C66h	DTDAR4	DTC Destination Address Register 4	XXXXh	
06C67h				
06C68h	DTCCR5	DTC Control Register 5	XXh	
06C69h	DTBLS5	DTC Block Size Register 5	XXh	
06C6Ah	DTCCT5	DTC Transfer Count Register 5	XXh	
06C6Bh	DTRLD5	DTC Transfer Count Reload Register 5	XXh	
06C6Ch	DTSAR5	DTC Source Address Register 5	XXXXh	
06C6Dh				
06C6Eh	DTDAR5	DTC Destination Address Register 5	XXXXh	
06C6Fh				
06C70h	DTCCR6	DTC Control Register 6	XXh	
06C71h	DTBLS6	DTC Block Size Register 6	XXh	
06C72h	DTCCT6	DTC Transfer Count Register 6	XXh	
06C73h	DTRLD6	DTC Transfer Count Reload Register 6	XXh	
06C74h	DTSAR6	DTC Source Address Register 6	XXXXh	
06C75h				
06C76h	DTDAR6	DTC Destination Address Register 6	XXXXh	
06C77h				
06C78h	DTCCR7	DTC Control Register 7	XXh	
06C79h	DTBLS7	DTC Block Size Register 7	XXh	
06C7Ah	DTCCT7	DTC Transfer Count Register 7	XXh	
06C7Bh	DTRLD7	DTC Transfer Count Reload Register 7	XXh	
06C7Ch	DTSAR7	DTC Source Address Register 7	XXXXh	
06C7Dh				
06C7Eh	DTDAR7	DTC Destination Address Register 7	XXXXh	
06C7Fh				
06C80h	DTCCR8	DTC Control Register 8	XXh	
06C81h	DTBLS8	DTC Block Size Register 8	XXh	
06C82h	DTCCT8	DTC Transfer Count Register 8	XXh	
06C83h	DTRLD8	DTC Transfer Count Reload Register 8	XXh	
06C84h	DTSAR8	DTC Source Address Register 8	XXXXh	
06C85h				
06C86h	DTDAR8	DTC Destination Address Register 8	XXXXh	
06C87h				
06C88h	DTCCR9	DTC Control Register 9	XXh	
06C89h	DTBLS9	DTC Block Size Register 9	XXh	
06C8Ah	DTCCT9	DTC Transfer Count Register 9	XXh	
06C8Bh	DTRLD9	DTC Transfer Count Reload Register 9	XXh	
06C8Ch	DTSAR9	DTC Source Address Register 9	XXXXh	
06C8Dh				
06C8Eh	DTDAR9	DTC Destination Address Register 9	XXXXh	
06C8Fh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.15 SFR Information (15) (1)

Address	Symbol	Register Name	After Reset	Remarks
06C90h	DTCCR10	DTC Control Register 10	XXh	
06C91h	DTBLS10	DTC Block Size Register 10	XXh	
06C92h	DTCCT10	DTC Transfer Count Register 10	XXh	
06C93h	DTRLD10	DTC Transfer Count Reload Register 10	XXh	
06C94h	DTSAR10	DTC Source Address Register 10	XXXXh	
06C95h				
06C96h	DTDAR10	DTC Destination Address Register 10	XXXXh	
06C97h				
06C98h	DTCCR11	DTC Control Register 11	XXh	
06C99h	DTBLS11	DTC Block Size Register 11	XXh	
06C9Ah	DTCCT11	DTC Transfer Count Register 11	XXh	
06C9Bh	DTRLD11	DTC Transfer Count Reload Register 11	XXh	
06C9Ch	DTSAR11	DTC Source Address Register 11	XXXXh	
06C9Dh				
06C9Eh	DTDAR11	DTC Destination Address Register 11	XXXXh	
06C9Fh				
06CA0h	DTCCR12	DTC Control Register 12	XXh	
06CA1h	DTBLS12	DTC Block Size Register 12	XXh	
06CA2h	DTCCT12	DTC Transfer Count Register 12	XXh	
06CA3h	DTRLD12	DTC Transfer Count Reload Register 12	XXh	
06CA4h	DTSAR12	DTC Source Address Register 12	XXXXh	
06CA5h				
06CA6h	DTDAR12	DTC Destination Address Register 12	XXXXh	
06CA7h				
06CA8h	DTCCR13	DTC Control Register 13	XXh	
06CA9h	DTBLS13	DTC Block Size Register 13	XXh	
06CAAh	DTCCT13	DTC Transfer Count Register 13	XXh	
06CABh	DTRLD13	DTC Transfer Count Reload Register 13	XXh	
06CACh	DTSAR13	DTC Source Address Register 13	XXXXh	
06CADh				
06CAEh	DTDAR13	DTC Destination Address Register 13	XXXXh	
06CAFh				
06CB0h	DTCCR14	DTC Control Register 14	XXh	
06CB1h	DTBLS14	DTC Block Size Register 14	XXh	
06CB2h	DTCCT14	DTC Transfer Count Register 14	XXh	
06CB3h	DTRLD14	DTC Transfer Count Reload Register 14	XXh	
06CB4h	DTSAR14	DTC Source Address Register 14	XXXXh	
06CB5h				
06CB6h	DTDAR14	DTC Destination Address Register 14	XXXXh	
06CB7h				
06CB8h	DTCCR15	DTC Control Register 15	XXh	
06CB9h	DTBLS15	DTC Block Size Register 15	XXh	
06CBAh	DTCCT15	DTC Transfer Count Register 15	XXh	
06CBBh	DTRLD15	DTC Transfer Count Reload Register 15	XXh	
06CBCh	DTSAR15	DTC Source Address Register 15	XXXXh	
06CBDh				
06CBEh	DTDAR15	DTC Destination Address Register 15	XXXXh	
06CBFh				
06CC0h	DTCCR16	DTC Control Register 16	XXh	
06CC1h	DTBLS16	DTC Block Size Register 16	XXh	
06CC2h	DTCCT16	DTC Transfer Count Register 16	XXh	
06CC3h	DTRLD16	DTC Transfer Count Reload Register 16	XXh	
06CC4h	DTSAR16	DTC Source Address Register 16	XXXXh	
06CC5h				
06CC6h	DTDAR16	DTC Destination Address Register 16	XXXXh	
06CC7h				
06CC8h	DTCCR17	DTC Control Register 17	XXh	
06CC9h	DTBLS17	DTC Block Size Register 17	XXh	
06CCAh	DTCCT17	DTC Transfer Count Register 17	XXh	
06CCBh	DTRLD17	DTC Transfer Count Reload Register 17	XXh	
06CCCh	DTSAR17	DTC Source Address Register 17	XXXXh	
06CCDh				
06CCEh	DTDAR17	DTC Destination Address Register 17	XXXXh	
06CCFh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.6 Flash Memory (Data flash Block A to Block D) Characteristics (Vcc = 2.7 V to 5.5 V, Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (1)		10,000 (2)	—	—	times
—	Byte program time (Program and erase endurance ≤ 1,000 times)		—	160	950	µs
—	Byte program time (Program and erase endurance > 1,000 times)		—	300	950	µs
—	Block erase time (Program and erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (Program and erase endurance > 1,000 times)		—	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	3 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		–20 (N ver.) –40 (D ver.)	—	85	°C
—	Data hold time (6)	Ambient temperature = 55°C (7)	20	—	—	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100, 1,000 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. The data hold time includes 7,000 hours under an environment of ambient temperature 85°C.

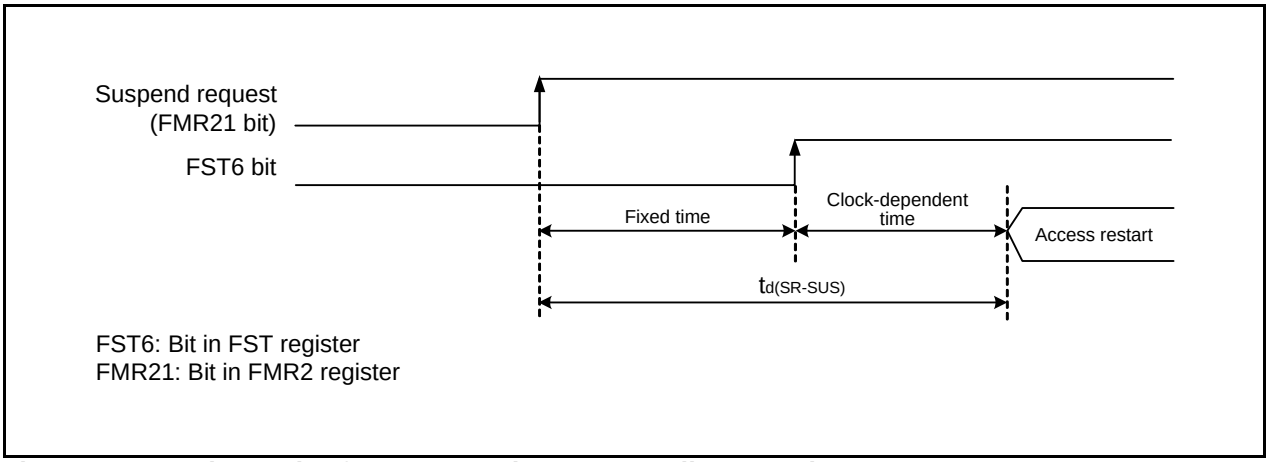


Figure 4.2 Time Delay from Suspend Request until Suspend

Table 4.7 Voltage Detection 0 Circuit Characteristics (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (1)	When Vcc falls	1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (1)	When Vcc falls	2.15	2.35	2.55	V
	Voltage detection level Vdet0_2 (1)	When Vcc falls	2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (1)	When Vcc falls	3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (2)	At the falling of Vcc from 5 V to (Vdet0 – 0.1) V	—	6	150	µs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. The voltage detection level must be selected with bits VDSEL0 and VDSEL1 in the OFS register.
2. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 4.16 DC Characteristics (3) [2.7 V ≤ Vcc < 4.2 V]
(Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	Other than XOUT	Drive capacity is high	I_{OH} = –5 mA	Vcc – 0.5	—	Vcc	V
			Drive capacity is low	I_{OH} = –1 mA	Vcc – 0.5	—	Vcc	V
		XOUT		I_{OH} = –200 µA	1.0	—	Vcc	V
V_{OL}	Output low voltage	Other than XOUT	Drive capacity is high	I_{OL} = 5 mA	—	—	0.5	V
			Drive capacity is low	I_{OL} = 1 mA	—	—	0.5	V
		XOUT		I_{OL} = 200 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRJIO_0, TRCCLK_0, TRCTRG_0, TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0, CLK_0, CLK_1, RXD_0, RXD_1, $\overline{CTS2}$, SCL2, SDA2, CLK2, RXD2, $\underline{SCL\_0}$, SDA_0, SSI_0, $\overline{SCS\_0}$, SSCK_0, SSO_0			0.1	0.4	—	V
		$\overline{RESET}$	Vcc = 3.0 V		0.1	0.5	—	V
I_{IH}	Input high current		V_I = 3.0 V		—	—	1.0	µA
I_{IL}	Input low current		V_I = 0 V		—	—	–1.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Table 4.19 DC Characteristics (6) [1.8 V ≤ Vcc < 2.7 V] (Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter	Conditions								Standard (4)			Unit
			Oscillation		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ.	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	5 MHz	Off	Off	125 kHz	No division	—		—	2.2	—	mA
			5 MHz	Off	Off	125 kHz	Divide-by-8	—		—	0.8	—	mA
		High-speed on-chip oscillator mode	Off	Off	5 MHz (3)	125 kHz	No division	—		—	2.5	10	mA
			Off	Off	5 MHz (3)	125 kHz	Divide-by-8	—		—	1.7	—	mA
			Off	Off	4 MHz (3)	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRC = 1		—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 SVC0 = 0		—	90	300	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 SVC0 = 0		—	80	350	µA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	90	µA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	4	80	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	—	2.2	6	µA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	—	30	—	µA

Notes:
1. Vcc = 1.8 V to 2.7 V, single-chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

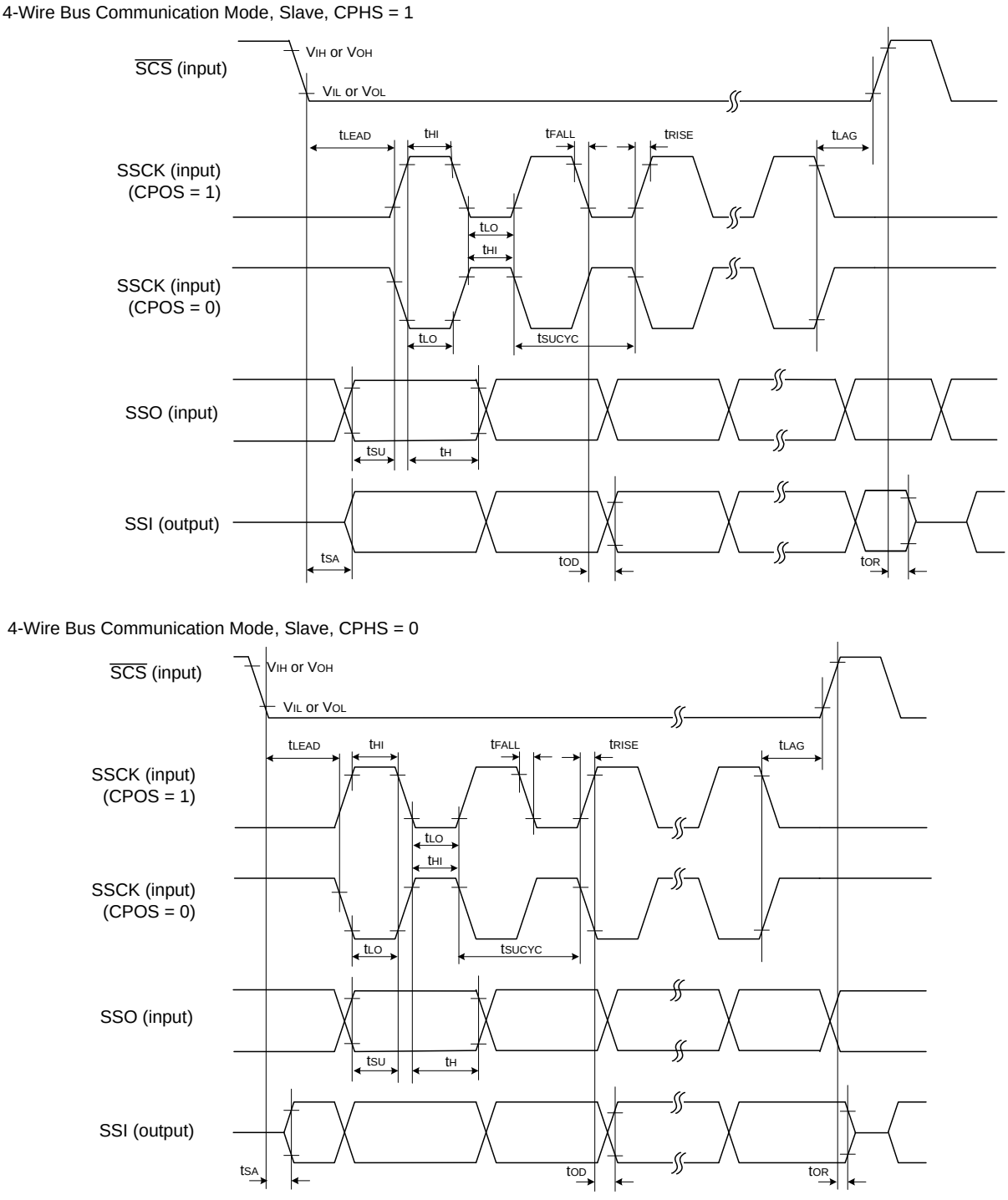


Figure 4.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

Table 4.26 Timing Requirements of External Interrupt $\overline{INTi}$ (i = 0 to 4) and Key Input Interrupt $\overline{KIj}$ (j = 0 to 3)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIj}$ input high width	1000 (1)	—	380 (1)	—	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIj}$ input low width	1000 (2)	—	380 (2)	—	250 (2)	—	ns

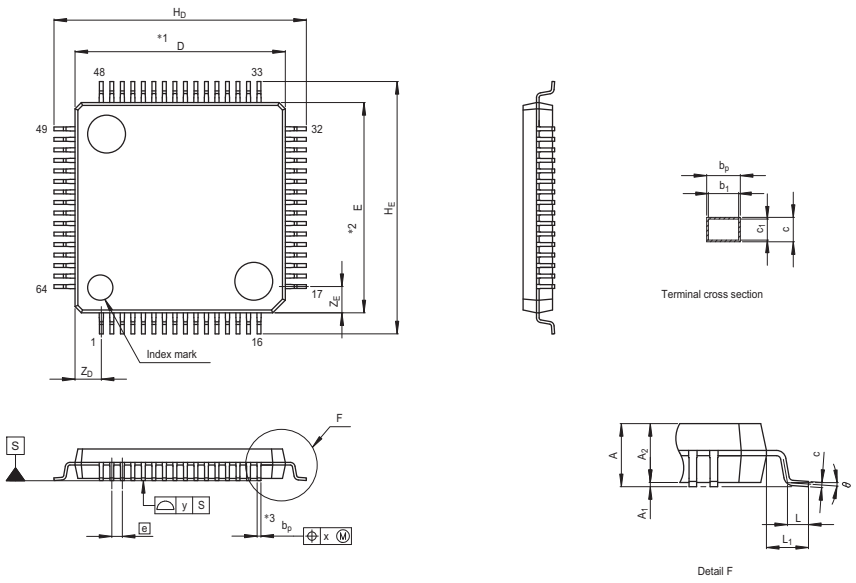
Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input high pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input low pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.

Figure 4.10 Input Timing of External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIj}$ (i = 0 to 4; j = 0 to 3)

Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

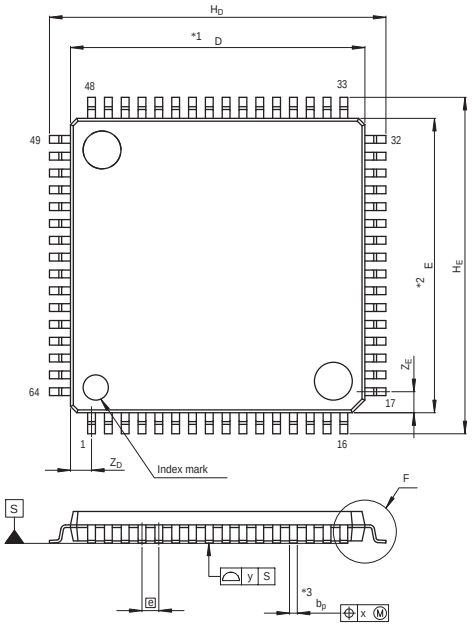
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g

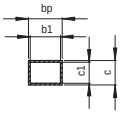


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

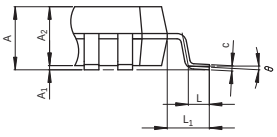
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.