Renesas Electronics America Inc - R5F21368SYFA#V0 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21368syfa-v0

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Tables 1.4 to 1.6 list the Pin Name Information by Pin Number.

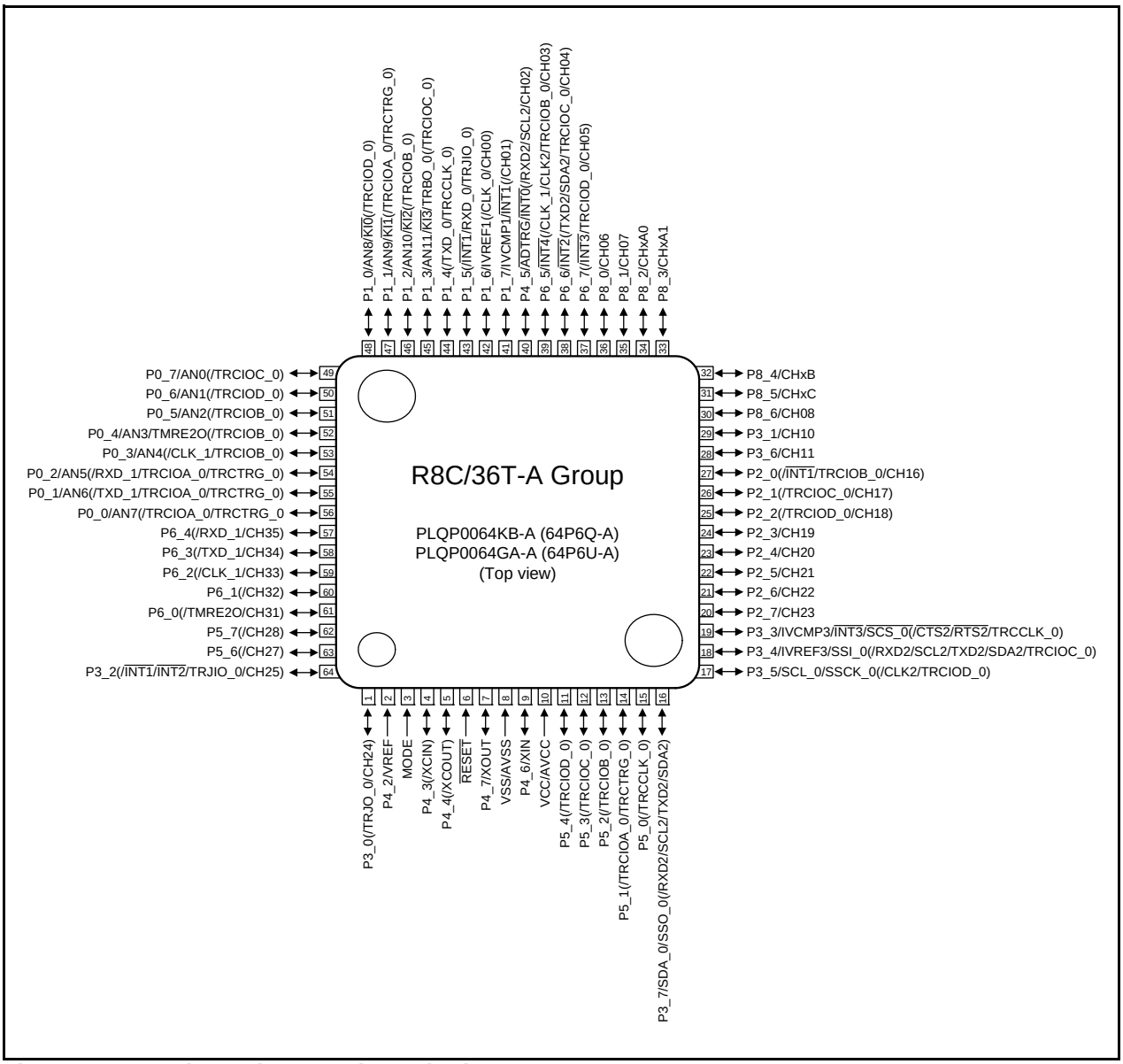


Figure 1.3 Pin Assignment (Top View)

Table 1.4 Pin Name Information by Pin Number (INT, URAT0, and UART2)

Port	Pin No.	INT					UART0						UART2						
		$\overline{INT0}$	$\overline{INT1}$	$\overline{INT2}$	$\overline{INT3}$	$\overline{INT4}$	TXD_0	TXD_1	RXD_0	RXD_1	CLK_0	CLK_1	TXD2	RXD2	$\overline{CTS2}$	$\overline{RTS2}$	SDA2	SCL2	CLK2
P0_0	56																		
P0_1	55							TXD_1											
P0_2	54									RXD_1									
P0_3	53											CLK_1							
P0_4	52																		
P0_5	51																		
P0_6	50																		
P0_7	49																		
P1_0	48																		
P1_1	47																		
P1_2	46																		
P1_3	45																		
P1_4	44						TXD_0												
P1_5	43		$\overline{INT1}$						RXD_0										
P1_6	42										CLK_0								
P1_7	41		$\overline{INT1}$																
P2_0	27		$\overline{INT1}$																
P2_1	26																		
P2_2	25																		
P2_3	24																		
P2_4	23																		
P2_5	22																		
P2_6	21																		
P2_7	20																		
P3_0	1																		
P3_1	29																		
P3_2	64		$\overline{INT1}$	$\overline{INT2}$															
P3_3	19				$\overline{INT3}$										$\overline{CTS2}$	$\overline{RTS2}$			
P3_4	18												TXD2	RXD2			SDA2	SCL2	
P3_5	17																		CLK2
P3_6	28																		
P3_7	16												TXD2	RXD2			SDA2	SCL2	
P4_2	2																		
P4_3	4																		
P4_4	5																		
P4_5	40	$\overline{INT0}$												RXD2				SCL2	
P4_6	9																		
P4_7	7																		
P5_0	15																		
P5_1	14																		
P5_2	13																		
P5_3	12																		
P5_4	11																		
P5_6	63																		
P5_7	62																		
P6_0	61																		
P6_1	60																		
P6_2	59											CLK_1							
P6_3	58							TXD_1											
P6_4	57									RXD_1									
P6_5	39					$\overline{INT4}$						CLK_1							CLK2
P6_6	38			$\overline{INT2}$									TXD2				SDA2		
P6_7	37				$\overline{INT3}$														
P8_0	36																		
P8_1	35																		
P8_2	34																		
P8_3	33																		
P8_4	32																		
P8_5	31																		
P8_6	30																		

Table 1.6 Pin Name Information by Pin Number (Timer RC, Timer RE2, and Others)

Port	Pin No.	Timer RC						Timer RE2	Others		
		TRCCLK_0	TRCIOA_0	TRCIOB_0	TRCIOC_0	TRCIOD_0	TRCTRG_0	TMRE2O			
P0_0	56		TRCIOA_0				TRCTRG_0		AN7		
P0_1	55		TRCIOA_0				TRCTRG_0		AN6		
P0_2	54		TRCIOA_0				TRCTRG_0		AN5		
P0_3	53			TRCIOB_0					AN4		
P0_4	52			TRCIOB_0				TMRE2O	AN3		
P0_5	51			TRCIOB_0					AN2		
P0_6	50					TRCIOD_0			AN1		
P0_7	49				TRCIOC_0				AN0		
P1_0	48					TRCIOD_0			AN8	$\overline{KI0}$	
P1_1	47		TRCIOA_0				TRCTRG_0		AN9	$\overline{KI1}$	
P1_2	46			TRCIOB_0					AN10	$\overline{KI2}$	
P1_3	45				TRCIOC_0				AN11	$\overline{KI3}$	
P1_4	44	TRCCLK_0									
P1_5	43										
P1_6	42								IVREF1		CH00
P1_7	41								IVCMP1		CH01
P2_0	27			TRCIOB_0							CH16
P2_1	26				TRCIOC_0						CH17
P2_2	25					TRCIOD_0					CH18
P2_3	24										CH19
P2_4	23										CH20
P2_5	22										CH21
P2_6	21										CH22
P2_7	20										CH23
P3_0	1										CH24
P3_1	29										CH10
P3_2	64										CH25
P3_3	19	TRCCLK_0							IVCMP3		
P3_4	18				TRCIOC_0				IVREF3		
P3_5	17					TRCIOD_0					
P3_6	28										CH11
P3_7	16										
P4_2	2								VREF		
P4_3	4								XCIN		
P4_4	5								XCOUT		
P4_5	40								$\overline{ADTRG}$		CH02
P4_6	9								XIN		
P4_7	7								XOUT		
P5_0	15	TRCCLK_0									
P5_1	14		TRCIOA_0				TRCTRG_0				
P5_2	13			TRCIOB_0							
P5_3	12				TRCIOC_0						
P5_4	11					TRCIOD_0					
P5_6	63										CH27
P5_7	62										CH28
P6_0	61							TMRE2O			CH31
P6_1	60										CH32
P6_2	59										CH33
P6_3	58										CH34
P6_4	57										CH35
P6_5	39			TRCIOB_0							CH03
P6_6	38				TRCIOC_0						CH04
P6_7	37					TRCIOD_0					CH05
P8_0	36										CH06
P8_1	35										CH07
P8_2	34										CHxA0
P8_3	33										CHxA1
P8_4	32										CHxB
P8_5	31										CHxC
P8_6	30										CH08

1.5 Pin Functions

Tables 1.7 and 1.8 list Pin Functions.

Table 1.7 Pin Functions (1)

Item	Pin Name	I/O	Description
Power supply input	VCC, VSS	—	Apply 1.8 V through 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply input for the A/D converter. Connect a capacitor between pins AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Applying a low level to this pin resets the MCU.
MODE	MODE	I	Connect this pin to the VCC pin via a resistor.
XIN clock input	XIN	I	I/O for the XIN clock generation circuit. Connect a ceramic resonator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	I/O for the XCIN clock generation circuit. Connect a crystal oscillator between pins XCIN and XCOUT. (1) To use an external clock, input it to the XCOUT pin and leave the XCIN pin open.
XCIN clock output	XCOUT	I/O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$	I	$\overline{\text{INT}}$ interrupt input.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input.
Timer RJ_0	TRJIO_0	I/O	Input/output for timer RJ.
	TRJO_0	O	Output for timer RJ.
Timer RB2_0	TRBO_0	O	Output for timer RB2.
Timer RC_0	TRCCLK_0	I	External clock input.
	TRCTRG_0	I	External trigger input.
	TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0	I/O	Input/output for timer RC.
Timer RE2	TMRE2O	O	Divided clock output.
Serial interface (UART0)	CLK_0, CLK_1	I/O	Transfer clock input/output.
	RXD_0, RXD_1	I	Serial data input.
	TXD_0, TXD_1	O	Serial data output.
Serial interface (UART2)	$\overline{\text{CTS2}}$	I	Input for transmission control.
	$\overline{\text{RTS2}}$	O	Output for reception control.
	SCL2	I/O	I^2C mode clock input/output.
	SDA2	I/O	I^2C mode data input/output.
	RXD2	I	Serial data input.
	TXD2	O	Serial data output.
	CLK2	I/O	Transfer clock input/output.
Synchronous serial communication unit (SSU_0)	SSI_0	I/O	Data input/output.
	$\overline{\text{SCS\_0}}$	I/O	Chip-select input/output.
	$\overline{\text{SSCK\_0}}$	I/O	Clock input/output.
	SSO_0	I/O	Data input/output.
I^2C bus (I^2C_0)	SCL_0	I/O	Clock input/output.
	SDA_0	I/O	Data input/output.
Reference voltage input	VREF	I	Reference voltage input for the A/D converter.

Note:
1. Contact the oscillator manufacturer for oscillation characteristics.

Table 1.8 Pin Functions (2)

Item	Pin Name	I/O	Description
A/D converter	AN0 to AN11	I	Analog input for the A/D converter.
	$\overline{\text{ADTRG}}$	I	External trigger input for the A/D converter.
Comparator B	IVCMP1, IVCMP3	I	Analog voltage input for comparator B.
	IVREF1, IVREF3	I	Reference voltage input for comparator B.
Touch sensor control unit	CHxA0, CHxA1, CHxB, CHxC	I/O	Control pins for electrostatic capacitive touch detection.
	CH00 to CH08, CH10, CH11, CH16 to CH25, CH27, CH28, CH31 to CH35	I	Electrostatic capacitive touch detection pins.
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6_0 to P6_7, P8_0 to P8_6	I/O	8-bit CMOS input/output ports. Each port has an I/O select direction register, enabling switching input and output for each pin. For input ports, the presence or absence of a pull-up resistor can be selected by a program. All ports can be used as LED drive (high drive) ports.
Input port	P4_2	I	Input-only port.

Table 3.3 SFR Information (3) (1)

Address	Symbol	Register Name	After Reset	Remarks
0007Ah				
0007Bh				
0007Ch				
0007Dh				
0007Eh				
0007Fh				
00080h	U0MR_0	UART0_0 Transmit/Receive Mode Register	00h	
00081h	U0BRG_0	UART0_0 Bit Rate Register	XXh	
00082h	U0TB_0	UART0_0 Transmit Buffer Register	XXh	
00083h			XXh	
00084h	U0C0_0	UART0_0 Transmit/Receive Control Register 0	00001000b	
00085h	U0C1_0	UART0_0 Transmit/Receive Control Register 1	00000010b	
00086h	U0RB_0	UART0_0 Receive Buffer Register	XXXXh	
00087h				
00088h	U0IR_0	UART0_0 Interrupt Flag and Enable Register	00h	
00089h				
0008Ah				
0008Bh				
0008Ch	LINCR2_0	LIN_0 Special Function Register	00h	
0008Dh				
0008Eh	LINCT_0	LIN_0 Control Register	00h	
0008Fh	LINST_0	LIN_0 Status Register	00h	
00090h	U0MR_1	UART0_1 Transmit/Receive Mode Register	00h	
00091h	U0BRG_1	UART0_1 Bit Rate Register	XXh	
00092h	U0TB_1	UART0_1 Transmit Buffer Register	XXh	
00093h			XXh	
00094h	U0C0_1	UART0_1 Transmit/Receive Control Register 0	00001000b	
00095h	U0C1_1	UART0_1 Transmit/Receive Control Register 1	00000010b	
00096h	U0RB_1	UART0_1 Receive Buffer Register	XXXXh	
00097h				
00098h	U0IR_1	UART0_1 Interrupt Flag and Enable Register	00h	
00099h				
0009Ah				
0009Bh				
0009Ch				
0009Dh				
0009Eh				
0009Fh				
000A0h				
000A1h				
000A2h				
000A3h				
000A4h				
000A5h				
000A8h				
000A9h				
000AAh				
000ABh				
000ACh				
000ADh				
000AEh				
000AFh				
000B0h				
000B1h				
000B4h				
000B5h				
000B8h				
000B9h				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.4 SFR Information (4) (1)

Address	Symbol	Register Name	After Reset	Remarks
000BAh				
000BBh				
000BCh				
000BDh				
000BEh				
000BFh				
000C0h	U2MR	UART2 Transmit/Receive Mode Register	00h	
000C1h	U2BRG	UART2 Bit Rate Register	00h	
000C2h	U2TB	UART2 Transmit Buffer Register	00h	
000C3h			00h	
000C4h	U2C0	UART2 Transmit/Receive Control Register 0	00001000b	
000C5h	U2C1	UART2 Transmit/Receive Control Register 1	00000010b	
000C6h	U2RB	UART2 Receive Buffer Register	0000h	
000C7h				
000C8h	U2RXDF	UART2 Digital Filter Function Select Register	00h	
000C9h				
000CAh				
000CBh				
000CCh				
000CDh				
000CEh				
000CFh				
000D0h	U2SMR5	UART2 Special Mode Register 5	00h	
000D1h				
000D2h				
000D3h				
000D4h	U2SMR4	UART2 Special Mode Register 4	00h	
000D5h	U2SMR3	UART2 Special Mode Register 3	00h	
000D6h	U2SMR2	UART2 Special Mode Register 2	00h	
000D7h	U2SMR	UART2 Special Mode Register	00h	
000D8h				
000D9h				
000DAh				
000DBh				
000DCh				
000DDh				
000DEh				
000DFh				
000E0h	IICCR_0	I²C_0 Control Register	00001110b	
000E1h	SSBR_0	SS_0 Bit Counter Register	11111000b	
000E2h	SITDR_0	SI_0 Transmit Data Register	FFh	
000E3h			FFh	
000E4h	SIRDR_0	SI_0 Receive Data Register	FFh	
000E5h			FFh	
000E6h	SICR1_0	SI_0 Control Register 1	00h	
000E7h	SICR2_0	SI_0 Control Register 2	01111101b	
000E8h	SIMR1_0	SI_0 Mode Register 1	00010000b	
000E9h	SIER_0	SI_0 Interrupt Enable Register	00h	
000EAh	SISR_0	SI_0 Status Register	00h	
000EBh	SIMR2_0	SI_0 Mode Register 2	00h	
000ECh				
000EDh				
000EEh				
000EFh				
000F0h				
000F1h				
000F2h				
000F3h				
000F4h				
000F5h				
000F6h				
000F7h				
000F8h				
000F9h				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.6 SFR Information (6) (1)

Address	Symbol	Register Name	After Reset	Remarks
0013Ah	TRCGRA_0	Timer RC_0 General Register A	FFFFh	
0013Bh				
0013Ch	TRCGRB_0	Timer RC_0 General Register B	FFFFh	
0013Dh				
0013Eh	TRCGRC_0	Timer RC_0 General Register C	FFFFh	
0013Fh				
00140h	TRCGRD_0	Timer RC_0 General Register D	FFFFh	
00141h				
00142h	TRCMR_0	Timer RC_0 Mode Register	01001000b	
00143h	TRCCR1_0	Timer RC_0 Control Register 1	00h	
00144h	TRCIER_0	Timer RC_0 Interrupt Enable Register	01110000b	
00145h	TRCSR_0	Timer RC_0 Status Register	01110000b	
00146h	TRCIOR0_0	Timer RC_0 I/O Control Register 0	10001000b	
00147h	TRCIOR1_0	Timer RC_0 I/O Control Register 1	10001000b	
00148h	TRCCR2_0	Timer RC_0 Control Register 2	00011000b	
00149h	TRCDF_0	Timer RC_0 Digital Filter Function Select Register	00h	
0014Ah	TRCOER_0	Timer RC_0 Output Enable Register	01111111b	
0014Bh	TRCADCR_0	Timer RC_0 A/D Conversion Trigger Control Register	11110000b	
0014Ch	TRCOPR_0	Timer RC_0 Output Waveform Manipulation Register	00h	
0014Dh	TRCELCCR_0	Timer RC_0 ELC Cooperation Control Register	00h	
0014Eh				
0014Fh				
00150h				
00151h				
00152h				
00153h				
00154h				
00155h				
00156h				
00157h				
00158h				
00159h				
0015Ah				
0015Bh				
0015Ch				
0015Dh				
0015Eh				
0015Fh				
00160h				
00161h				
00162h				
00163h				
00164h				
00165h				
00166h				
00167h				
00168h				
00169h				
0016Ah				
0016Bh				
0016Ch				
0016Dh				
0016Eh				
0016Fh				
00170h	TRESEC	Timer RE2 Counter Data Register Timer RE2 Second Data Register	00h	
00171h	TREMIN	Timer RE2 Compare Data Register Timer RE2 Minute Data Register	00h	
00172h	TREHR	Timer RE2 Hour Data Register	00h	
00173h	TREWK	Timer RE2 Day-of-the-Week Data Register	00h	
00174h	TREDY	Timer RE2 Day Data Register	00000001b	
00175h	TREMON	Timer RE2 Month Data Register	00000001b	
00176h	TREYR	Timer RE2 Year Data Register	00h	
00177h	TRECR	Timer RE2 Control Register	00000100b	
00178h	TRECSR	Timer RE2 Count Source Select Register	00001000b	
00179h	TREADJ	Timer RE2 Clock Error Correction Register	00h	

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.10 SFR Information (10) (1)

Address	Symbol	Register Name	After Reset	Remarks
002C0h	PUR0	Pull-Up Control Register 0	00h	
002C1h	PUR1	Pull-Up Control Register 1	00h	
002C2h	PUR2	Pull-Up Control Register 2	00h	
002C3h				
002C4h				
002C5h				
002C6h				
002C7h				
002C8h	P1DRR	Port P1 Drive Capacity Control Register	00h	
002C9h	P2DRR	Port P2 Drive Capacity Control Register	00h	
002CAh				
002CBh				
002CCh	DRR0	Drive Capacity Control Register 0	00h	
002CDh	DRR1	Drive Capacity Control Register 1	00h	
002CEh	DRR2	Drive Capacity Control Register 2	00h	
002CFh				
002D0h	VLT0	Input Threshold Control Register 0	00h	
002D1h	VLT1	Input Threshold Control Register 1	00h	
002D2h	VLT2	Input Threshold Control Register 2	00h	
002D3h				
002D4h				
002D5h				
002D6h				
002D7h				
002D8h				
002D9h				
002DAh				
002DBh				
002DCh				
002DDh				
002DEh				
002DFh				
002E0h	PORT0	Port P0 Register	XXh	
002E1h	PORT1	Port P1 Register	XXh	
002E2h	PD0	Port P0 Direction Register	00h	
002E3h	PD1	Port P1 Direction Register	00h	
002E4h	PORT2	Port P2 Register	XXh	
002E5h	PORT3	Port P3 Register	XXh	
002E6h	PD2	Port P2 Direction Register	00h	
002E7h	PD3	Port P3 Direction Register	00h	
002E8h	PORT4	Port P4 Register	XXh	
002E9h	PORT5	Port P5 Register	XXh	
002EAh	PD4	Port P4 Direction Register	00h	
002EBh	PD5	Port P5 Direction Register	00h	
002ECh	PORT6	Port P6 Register	XXh	
002EDh				
002EEh	PD6	Port P6 Direction Register	00h	
002EFh				
002F0h	PORT8	Port P8 Register	XXh	
002F1h				
002F2h	PD8	Port P8 Direction Register	00h	
002F3h				
002F4h				
002F5h				
002F6h				
002F7h				
002F8h				
002F9h				
002FAh				
002FBh				
002FCh				
002FDh				
002FEh				
002FFh				
00300h to 003FFh				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.11 SFR Information (11) (1)

Address	Symbol	Register Name	After Reset	Remarks
00400h to 053FFh	On-chip RAM	On-chip RAM		
05400h to 069FFh				
06A00h	ELSELR0	Event Output Destination Select Register 0	00h	
06A01h	ELSELR1	Event Output Destination Select Register 1	00h	
06A02h	ELSELR2	Event Output Destination Select Register 2	00h	
06A03h	ELSELR3	Event Output Destination Select Register 3	00h	
06A04h	ELSELR4	Event Output Destination Select Register 4	00h	
06A05h				
06A06h				
06A07h				
06A08h	ELSELR8	Event Output Destination Select Register 8	00h	
06A09h	ELSELR9	Event Output Destination Select Register 9	00h	
06A0Ah				
06A0Bh	ELSELR11	Event Output Destination Select Register 11	00h	
06A0Ch	ELSELR12	Event Output Destination Select Register 12	00h	
06A0Dh	ELSELR13	Event Output Destination Select Register 13	00h	
06A0Eh	ELSELR14	Event Output Destination Select Register 14	00h	
06A0Fh	ELSELR15	Event Output Destination Select Register 15	00h	
06A10h	ELSELR16	Event Output Destination Select Register 16	00h	
06A11h				
06A12h				
06A13h				
06A14h				
06A15h				
06A16h				
06A17h				
06A18h				
06A19h				
06A1Ah				
06A1Bh				
06A1Ch				
06A1Dh				
06A1Eh				
06A1Fh				
06A20h				
06A21h				
06A22h				
06A23h				
06A24h				
06A25h				
06A26h				
06A27h				
06A28h				
06A29h				
06A2Ah				
06A2Bh				
06A2Ch				
06A2Dh				
06A2Eh				
06A2Fh				
06A30h				
06A31h to 06AFFh				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.13 SFR Information (13) (1)

Address	Symbol	Register Name	After Reset	Remarks
06C0Ah		Area for storing DTC transfer vector 10	XXh	
06C0Bh		Area for storing DTC transfer vector 11	XXh	
06C0Ch		Area for storing DTC transfer vector 12	XXh	
06C0Dh		Area for storing DTC transfer vector 13	XXh	
06C0Eh		Area for storing DTC transfer vector 14	XXh	
06C0Fh		Area for storing DTC transfer vector 15	XXh	
06C10h		Area for storing DTC transfer vector 16	XXh	
06C11h		Area for storing DTC transfer vector 17	XXh	
06C12h		Area for storing DTC transfer vector 18	XXh	
06C13h		Area for storing DTC transfer vector 19	XXh	
06C14h				
06C15h				
06C16h		Area for storing DTC transfer vector 22	XXh	
06C17h		Area for storing DTC transfer vector 23	XXh	
06C18h		Area for storing DTC transfer vector 24	XXh	
06C19h		Area for storing DTC transfer vector 25	XXh	
06C1Ah				
06C1Bh				
06C1Ch				
06C1Dh				
06C1Eh				
06C1Fh				
06C20h				
06C21h				
06C22h				
06C23h				
06C24h				
06C25h				
06C26h				
06C27h				
06C28h				
06C29h				
06C2Ah		Area for storing DTC transfer vector 42	XXh	
06C2Bh				
06C2Ch				
06C2Dh				
06C2Eh				
06C2Fh				
06C30h				
06C31h		Area for storing DTC transfer vector 49	XXh	
06C32h				
06C33h		Area for storing DTC transfer vector 51	XXh	
06C34h		Area for storing DTC transfer vector 52	XXh	
06C35h		Area for storing DTC transfer vector 53	XXh	
06C36h		Area for storing DTC transfer vector 54	XXh	
06C37h				
06C38h				
06C39h				
06C3Ah				
06C3Bh				
06C3Ch				
06C3Dh				
06C3Eh				
06C3Fh				
06C40h	DTCCR0	DTC Control Register 0	XXh	
06C41h	DTBLS0	DTC Block Size Register 0	XXh	
06C42h	DTCCT0	DTC Transfer Count Register 0	XXh	
06C43h	DTRLD0	DTC Transfer Count Reload Register 0	XXh	
06C44h	DTSAR0	DTC Source Address Register 0	XXXXh	
06C45h				
06C46h	DTDAR0	DTC Destination Address Register 0	XXXXh	
06C47h				
06C48h	DTCCR1	DTC Control Register 1	XXh	
06C49h	DTBLS1	DTC Block Size Register 1	XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

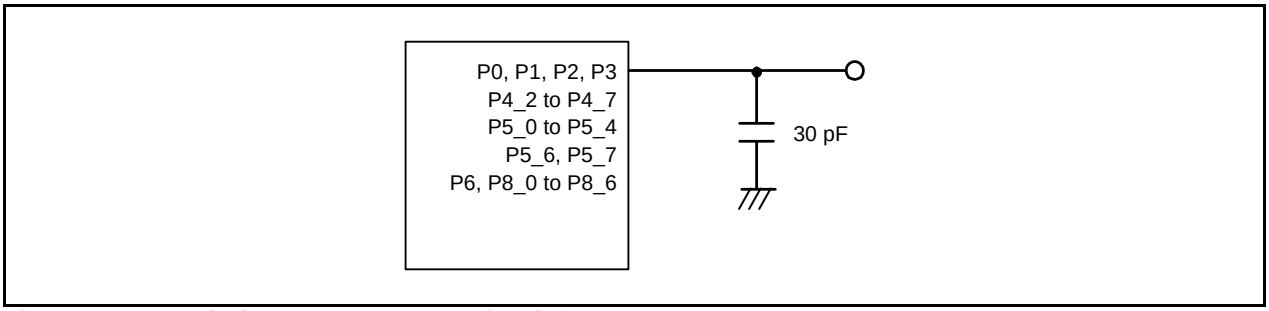


Figure 4.1 Timing Measurement Circuit for Ports P0, P1, P2, P3, P4_2 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6, and P8_0 to P8_6

4.3 Peripheral Function Characteristics

Table 4.3 A/D Converter Characteristics (Vcc/AVcc = Vref = 2.2 V to 5.5 V, Vss = 0 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		V_{ref} = AVcc		—	—	10	Bit
—	Absolute accuracy	10-bit mode	V_{ref} = AVcc = 5.0 V	AN0 to AN11 input	—	—	±3	LSB
			V_{ref} = AVcc = 3.3 V	AN0 to AN11 input	—	—	±5	LSB
			V_{ref} = AVcc = 3.0 V	AN0 to AN11 input	—	—	±5	LSB
			V_{ref} = AVcc = 2.2 V	AN0 to AN11 input	—	—	±5	LSB
		8-bit mode	V_{ref} = AVcc = 5.0 V	AN0 to AN11 input	—	—	±2	LSB
			V_{ref} = AVcc = 3.3 V	AN0 to AN11 input	—	—	±2	LSB
			V_{ref} = AVcc = 3.0 V	AN0 to AN11 input	—	—	±2	LSB
			V_{ref} = AVcc = 2.2 V	AN0 to AN11 input	—	—	±2	LSB
ϕAD	A/D conversion clock		4.0 V ≤ V_{ref} = AVcc ≤ 5.5 V (1)		2	—	20	MHz
			3.2 V ≤ V_{ref} = AVcc ≤ 5.5 V (1)		2	—	16	MHz
			2.7 V ≤ V_{ref} = AVcc ≤ 5.5 V (1)		2	—	10	MHz
			2.2 V ≤ V_{ref} = AVcc ≤ 5.5 V (1)		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
I_{vref}	Vref current		Vcc = 5 V, XIN = f1 = fAD = 20 MHz		—	45	—	µA
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	—	—	µs
		8-bit mode	V_{ref} = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	—	—	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	—	—	µs
V_{ref}	Reference voltage				2.2	—	AVcc	V
V_{IA}	Analog input voltage (2)				0	—	V_{ref}	V
OCVREF	On-chip reference voltage		2MHz ≤ ϕAD ≤ 4MHz		1.19	1.34	1.49	V

Notes:
1. If the CPU and the flash memory stop, the A/D conversion result will be undefined.
2. When the analog input voltage exceeds the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 4.4 Comparator B Characteristics (Vcc/AVcc = 2.2 V to 5.5 V, Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	Vcc – 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		–0.3	—	Vcc + 0.3	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time (1)	V_I = V_{ref} ±100 mV	—	0.1	—	µs
I_{CMP}	Comparator operating current	Vcc = 5.0 V	—	17.5	—	µA

Note:
1. When the digital filter is not selected.

4.4 DC Characteristics

Table 4.14 DC Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V] (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	Other than XOUT	Drive capacity is high	I_{OH} = –20 mA	Vcc – 2.0	—	Vcc	V
			Drive capacity is low	I_{OH} = –5 mA	Vcc – 2.0	—	Vcc	V
				I_{OH} = –200 µA	Vcc – 0.3	—	Vcc	V
		XOUT		I_{OH} = –200 µA	1.0	—	Vcc	V
V_{OL}	Output low voltage	Other than XOUT	Drive capacity is high	I_{OL}= 20 mA	—	—	2.0	V
			Drive capacity is low	I_{OL} = 5 mA	—	—	2.0	V
				I_{OL} = 200 µA	—	—	0.45	V
		XOUT		I_{OL} = 200 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRJIO_0, TRCCLK_0, TRCTRG_0, TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0, CLK_0, CLK_1, $\overline{RXD\_0}$, RXD_1, $\overline{CTS2}$, SCL2, SDA2, CLK2, RXD2, $\underline{SCL\_0}$, SDA_0, SSI_0, $\overline{SCS\_0}$, SSCK_0, SSO_0			0.1	1.2	—	V
		$\overline{RESET}$	Vcc = 5.0 V		0.1	1.2	—	V
I_{IH}	Input high current		V_I = 5.0 V		—	—	1.0	µA
I_{IL}	Input low current		V_I = 0 V		—	—	–1.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

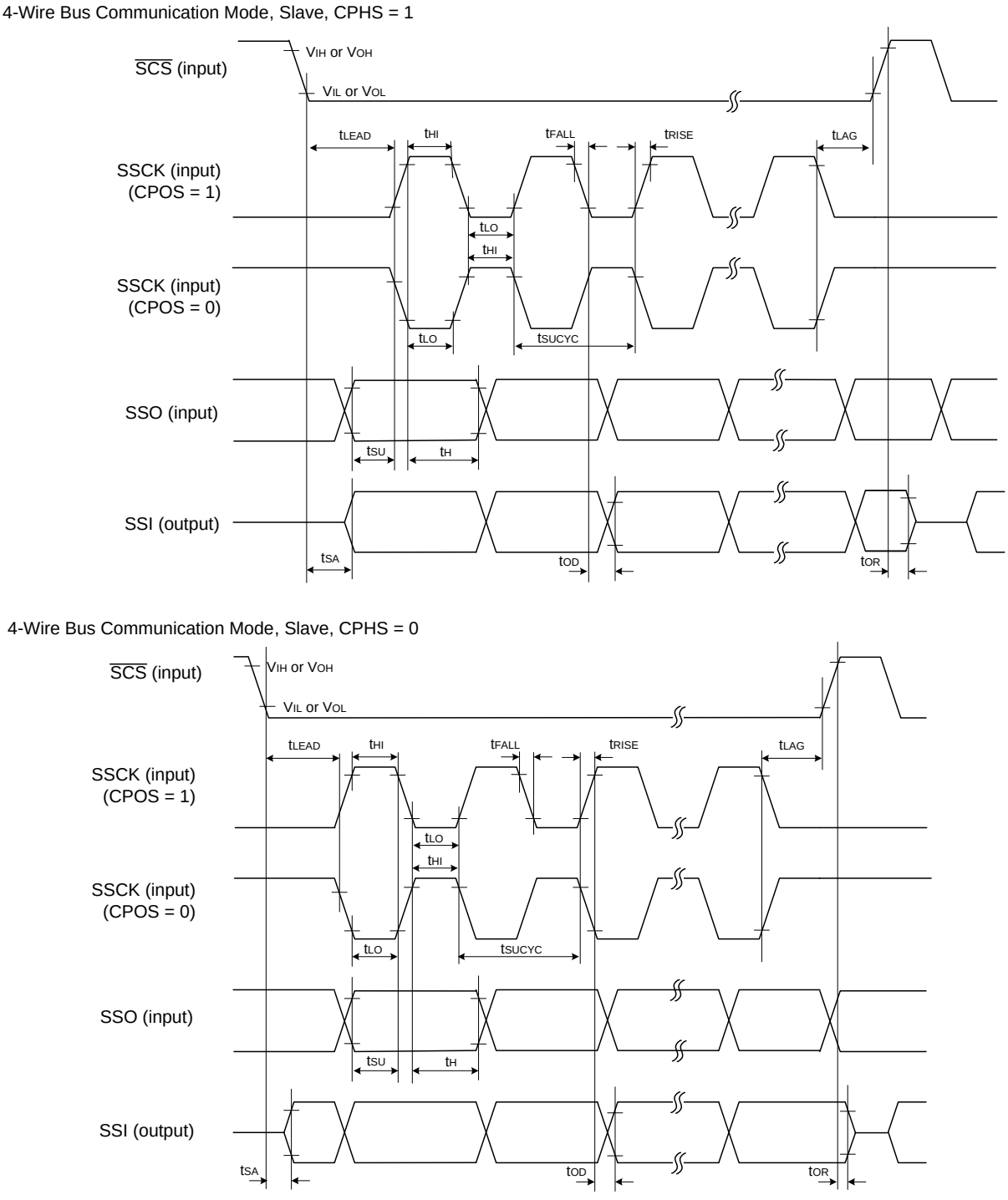


Figure 4.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

Table 4.22 External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	200	—	50	—	50	—	ns
$t_{WH(XOUT)}$	XOUT input high width	90	—	24	—	24	—	ns
$t_{WL(XOUT)}$	XOUT input low width	90	—	24	—	24	—	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	—	14	—	14	—	µs
$t_{WH(XCIN)}$	XCIN input high width	7	—	7	—	7	—	µs
$t_{WL(XCIN)}$	XCIN input low width	7	—	7	—	7	—	µs

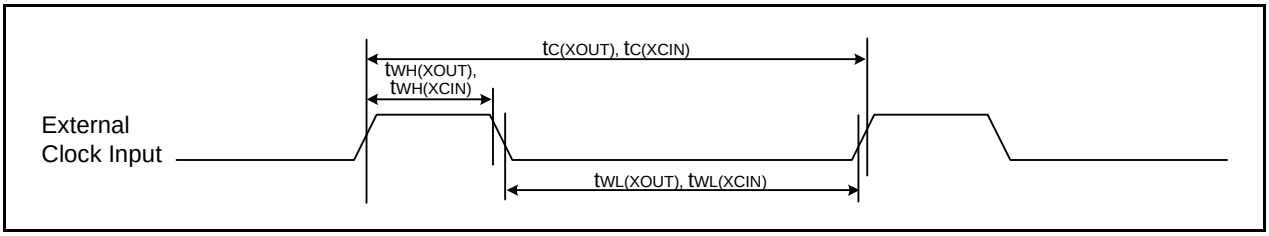


Figure 4.7 External Clock Input Timing Diagram

Table 4.23 Timing Requirements of TRJIO

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	500	—	300	—	100	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	200	—	120	—	40	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	200	—	120	—	40	—	ns

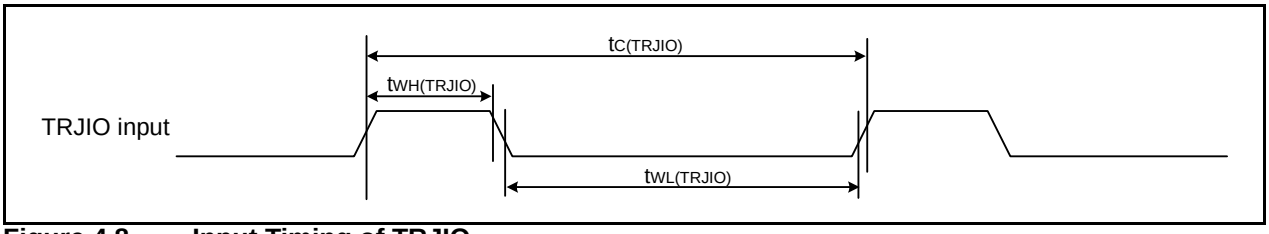


Figure 4.8 Input Timing of TRJIO

Table 4.26 Timing Requirements of External Interrupt $\overline{INTi}$ (i = 0 to 4) and Key Input Interrupt $\overline{KIj}$ (j = 0 to 3)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIj}$ input high width	1000 (1)	—	380 (1)	—	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIj}$ input low width	1000 (2)	—	380 (2)	—	250 (2)	—	ns

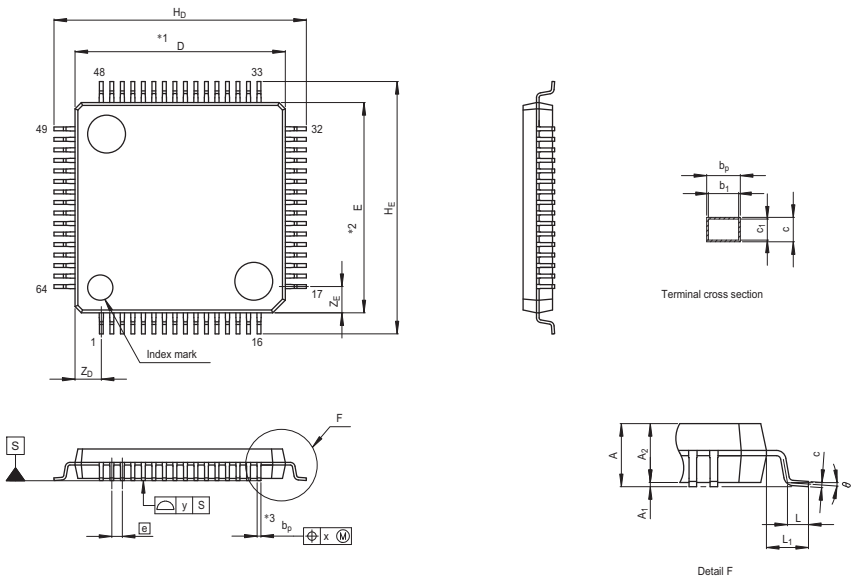
Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input high pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input low pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.

Figure 4.10 Input Timing of External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIj}$ (i = 0 to 4; j = 0 to 3)

Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

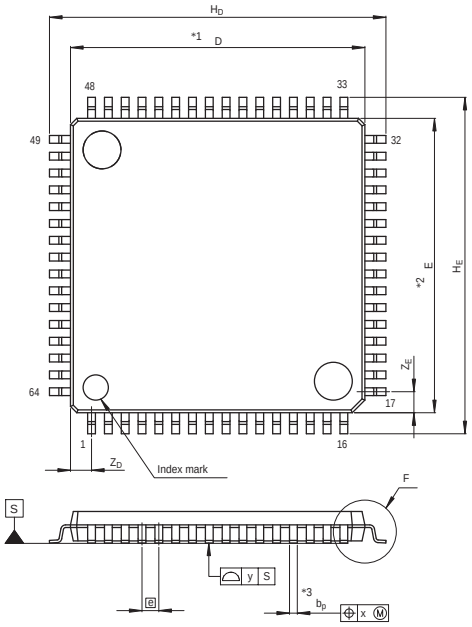
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g

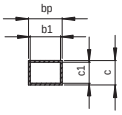


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

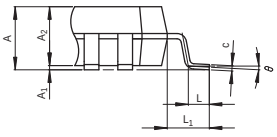
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

REVISION HISTORY	R8C/36T-A Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Feb 23, 2011	—	First Edition issued
1.00	Dec 09, 2011	All pages	“Preliminary”, “Under development” deleted, “sensor control unit” → “touch sensor control unit”
		2, 3	Tables 1.1 and 1.2 revised
		6	Figure 1.3 “P3_10/CH10” → “P3_1/CH10”
		11	Table 1.8 “Touch sensor control unit” added
		13	2.1 revised
		16, 17, 19 to 22, 24 to 28	Tables 3.1, 3.2, 3.4 to 3.7, 3.9 to 3.13
		32	Table 3.17 revised, Note 2 added
		33 to 56	“4. Electrical Characteristics” added