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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2136asnfa-30

1.1.2 Specifications

Tables 1.1 and 1.2 outline Specifications.

Table 1.1 Specifications (1)

Item	Function	Description
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (CPU clock = 20 MHz, VCC = 2.7 V to 5.5 V) 200 ns (CPU clock = 5 MHz, VCC = 1.8 V to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, data flash	Refer to Table 1.3 Product List .
Voltage detection	Voltage detection circuit	• Power-on reset • Voltage detection with three check points (the detection levels for voltage detection 0 and voltage detection 1 can be selected.)
I/O ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 59, selectable pull-up resistor • High current drive ports: 59
Clock	Clock generation circuits	• 4 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Divided by 1, 2, 4, 8, or 16 can be selected • Low-power mode: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Number of interrupt vectors: 69 • External interrupt inputs: 9 (INT × 5, key input × 4) • Priority levels: 7
Event link controller (ELC)		• Events output from peripheral functions can be linked to events input to different peripheral functions. (30 sources × 10 types of event link operations) • Events can be handled independently from interrupt requests.
Watchdog timer		• 14 bits × 1 • Selectable reset start function • Selectable low-speed on-chip oscillator for the watchdog timer
DTC (data transfer controller)		• 1 channel • Activation sources: 27 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timers RJ_0	16 bits × 1: 1 circuit integrated on-chip Timer mode (periodic timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB2_0	16 bits × 1: 1 circuit integrated on-chip Timer mode (periodic timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timers RC_0	16 bits (with 4 capture/compare registers) × 1: 1 circuit integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)
	Timer RE2	8 bits × 1 Compare match timer mode, real-time clock mode

Table 1.2 Specifications (2)

Item	Function	Description
Serial interface	UART0_0 and UART0_1	2 channels Clock synchronous serial I/O mode, clock asynchronous serial I/O mode
	UART2	1 channel Clock synchronous serial I/O mode, clock asynchronous serial I/O mode, I ² C mode (I ² C-bus), multiprocessor communication mode
Clock Synchronous serial interface	(SSU) SSU_0	1 channel (also used for the I ² C bus)
	(I ² C bus) I ² C_0	1 channel (also used for the SSU)
LIN module	HW-LIN_0	Hardware LIN 1 channel (timer RJ_0, UART0_0, or UART0_1 used)
A/D converter		Resolution: 10 bits × 12 channels, sample and hold function, sweep mode
Comparator B		2 circuits
Touch Sensor control unit (TSCU)		System CH × 4, electrostatic capacitive touch detection × 28
CRC calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash memory		• Program/erase voltage: VCC = 2.7 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • BGO (background operation) function (data flash)
Operating frequency/ Power supply voltage		CPU clock = 20 MHz (VCC = 2.7 V to 5.5 V) CPU clock = 5 MHz (VCC = 1.8 V to 5.5 V)
Current consumption		Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 4.0 μA (VCC = 3.0 V, wait mode f(XCIN) = 32 kHz) Typ. 2.2 μA (VCC = 3.0 V, stop mode)
Operating ambient temperature		-20°C to 85°C (N version) -40°C to 85°C (D version) ⁽¹⁾
Package		64-pin LQFP Package code: PLQP0064KB-A (previous code: 64P6Q-A) Package code: PLQP0064GA-A (previous code: 64P6U-A)

Note:

1. Specify the D version if it is to be used.

Table 1.4 Pin Name Information by Pin Number (INT, URAT0, and UART2)

Port	Pin No.	INT					UART0						UART2						
		INT0	INT1	INT2	INT3	INT4	TXD_0	TXD_1	RXD_0	RXD_1	CLK_0	CLK_1	TXD2	RXD2	CTS2	RTS2	SDA2	SCL2	CLK2
P0_0	56																		
P0_1	55							TXD_1											
P0_2	54									RXD_1									
P0_3	53										CLK_1								
P0_4	52																		
P0_5	51																		
P0_6	50																		
P0_7	49																		
P1_0	48																		
P1_1	47																		
P1_2	46																		
P1_3	45																		
P1_4	44						TXD_0												
P1_5	43		INT1						RXD_0										
P1_6	42										CLK_0								
P1_7	41		INT1																
P2_0	27		INT1																
P2_1	26																		
P2_2	25																		
P2_3	24																		
P2_4	23																		
P2_5	22																		
P2_6	21																		
P2_7	20																		
P3_0	1																		
P3_1	29																		
P3_2	64		INT1	INT2															
P3_3	19				INT3										CTS2	RTS2			
P3_4	18												TXD2	RXD2			SDA2	SCL2	
P3_5	17																		CLK2
P3_6	28																		
P3_7	16												TXD2	RXD2			SDA2	SCL2	
P4_2	2																		
P4_3	4																		
P4_4	5																		
P4_5	40	INT0												RXD2				SCL2	
P4_6	9																		
P4_7	7																		
P5_0	15																		
P5_1	14																		
P5_2	13																		
P5_3	12																		
P5_4	11																		
P5_6	63																		
P5_7	62																		
P6_0	61																		
P6_1	60																		
P6_2	59										CLK_1								
P6_3	58							TXD_1											
P6_4	57									RXD_1									
P6_5	39					INT4						CLK_1							CLK2
P6_6	38			INT2									TXD2				SDA2		
P6_7	37				INT3														
P8_0	36																		
P8_1	35																		
P8_2	34																		
P8_3	33																		
P8_4	32																		
P8_5	31																		
P8_6	30																		

Table 1.5 Pin Name Information by Pin Number (SSU/I²C, Timer RJ, and Timer RB2)

Port	Pin No.	SSU/I ² C						Timer RJ		Timer RB2
		SCL_0	SDA_0	SSI_0	SCS_0	SSCK_0	SSO_0	TRJO_0	TRJIO_0	TRBO_0
P0_0	56									
P0_1	55									
P0_2	54									
P0_3	53									
P0_4	52									
P0_5	51									
P0_6	50									
P0_7	49									
P1_0	48									
P1_1	47									
P1_2	46									
P1_3	45									TRBO_0
P1_4	44									
P1_5	43								TRJIO_0	
P1_6	42									
P1_7	41									
P2_0	27									
P2_1	26									
P2_2	25									
P2_3	24									
P2_4	23									
P2_5	22									
P2_6	21									
P2_7	20									
P3_0	1							TRJO_0		
P3_1	29									
P3_2	64								TRJIO_0	
P3_3	19				SCS_0					
P3_4	18			SSI_0						
P3_5	17	SCL_0				SSCK_0				
P3_6	28									
P3_7	16		SDA_0				SSO_0			
P4_2	2									
P4_3	4									
P4_4	5									
P4_5	40									
P4_6	9									
P4_7	7									
P5_0	15									
P5_1	14									
P5_2	13									
P5_3	12									
P5_4	11									
P5_6	63									
P5_7	62									
P6_0	61									
P6_1	60									
P6_2	59									
P6_3	58									
P6_4	57									
P6_5	39									
P6_6	38									
P6_7	37									
P8_0	36									
P8_1	35									
P8_2	34									
P8_3	33									
P8_4	32									
P8_5	31									
P8_6	30									

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 through R3.

R0 can be split into high-order (R0H) and low-order (R0L) registers to be used separately as 8-bit data registers. The same applies to R1H and R1L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). Similarly, R3 and R1 can be used as a 32-bit data register.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 functions in the same manner as A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

PC is a 20-bit register that indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of the FLG register is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated in the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. It must only be set to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0. Otherwise it is set to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value. Otherwise it is set to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow. Otherwise it is set to 0.

3.2 Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 3.1 to 3.16 list the SFR Information. Table 3.17 lists the ID code Area, Option Function Select Area.

Table 3.1 SFR Information (1) (1)

Address	Symbol	Register Name	After Reset	Remarks
00000h				
00001h				
00002h				
00003h				
00004h	PM0	Processor Mode Register 0	00h	
00005h	PM1	Processor Mode Register 1	10000000b	
00006h				
00007h	PRCR	Protect Register	00h	
00008h	CM0	System Clock Control Register 0	00101000b	
00009h	CM1	System Clock Control Register 1	00100000b	
0000Ah	OCD	Oscillation Stop Detection Register	00h	
0000Bh	CM3	System Clock Control Register 3	00h	
0000Ch	CM4	System Clock Control Register 4	00000001b	
0000Dh				
0000Eh				
0000Fh				
00010h	CPSRF	Clock Prescaler Reset Flag	00h	
00011h				
00012h	FRA0	High-Speed On-Chip Oscillator Control Register 0	00h	
00013h				
00014h	FRA2	High-Speed On-Chip Oscillator Control Register 2	00h	
00015h				
00016h				
00017h				
00018h				
00019h				
0001Ah				
0001Bh				
0001Ch				
0001Dh				
0001Eh				
0001Fh				
00020h	RISR	Reset Interrupt Select Register	10000000b or 00000000b	(Note 2)
00021h	WDTR	Watchdog Timer Reset Register	FFh	
00022h	WDTs	Watchdog Timer Start Register	FFh	
00023h	WDTC	Watchdog Timer Control Register	01111111b	
00024h	CSPR	Count Source Protection Mode Register	10000000b or 00000000b	(Note 2)
00025h				
00026h				
00027h				
00028h	RSTFR	Reset Source Determination Register	00XXXXXXb	
00029h				
0002Ah				
0002Bh				
0002Ch	SVDC	STBY VDC Power Control Register	00h	
0002Dh				
0002Eh				
0002Fh				
00030h	CMPA	Voltage Monitor Circuit Control Register	00h	
00031h	VCAC	Voltage Monitor Circuit Edge Select Register	00h	
00032h	OCVREFCR	On-Chip Reference Voltage Control Register	00h	
00033h				
00034h	VCA2	Voltage Detection Register 2	00000000b or 00100000b	(Note 3)
00035h				
00036h	VD1LS	Voltage Detection 1 Level Select Register	00000111b	
00037h				
00038h	VW0C	Voltage Monitor 0 Circuit Control Register	1100XX10b or 1100XX11b	(Note 3)
00039h	VW1C	Voltage Monitor 1 Circuit Control Register	10001010b	

X: Undefined

Notes:

1. The blank areas are reserved. No access is allowed.
2. Depends on the CSPROINI bit in the OFS register.
3. Depends on the LVDASI bit in the OFS register.

Table 3.2 SFR Information (2) ⁽¹⁾

Address	Symbol	Register Name	After Reset	Remarks
0003Ah	VW2C	Voltage Monitor 2 Circuit Control Register	10001010b	
0003Bh				
0003Ch				
0003Dh				
0003Eh				
0003Fh				
00040h				
00041h	FMRDYIC	Interrupt Control Register	00h	
00042h				
00043h				
00044h				
00045h				
00046h	INT4IC	Interrupt Control Register	00h	
00047h	TRCIC_0	Interrupt Control Register	00h	
00048h				
00049h				
0004Ah	TRE2IC	Interrupt Control Register	00h	
0004Bh	U2TIC	Interrupt Control Register	00h	
0004Ch	U2RIC	Interrupt Control Register	00h	
0004Dh	KUPIC	Interrupt Control Register	00h	
0004Eh	ADIC	Interrupt Control Register	00h	
0004Fh	SSUIC_0/IICIC_0	Interrupt Control Register	00h	
00050h				
00051h	U0TIC_0	Interrupt Control Register	00h	
00052h	U0RIC_0	Interrupt Control Register	00h	
00053h	U0TIC_1	Interrupt Control Register	00h	
00054h	U0RIC_1	Interrupt Control Register	00h	
00055h	INT2IC	Interrupt Control Register	00h	
00056h	TRJIC_0	Interrupt Control Register	00h	
00057h				
00058h	TRB2IC_0	Interrupt Control Register	00h	
00059h	INT1IC	Interrupt Control Register	00h	
0005Ah	INT3IC	Interrupt Control Register	00h	
0005Bh				
0005Ch				
0005Dh	INT0IC	Interrupt Control Register	00h	
0005Eh	U2BCNIC	Interrupt Control Register	00h	
0005Fh				
00060h				
00061h				
00062h				
00063h				
00064h				
00065h				
00066h				
00067h				
00068h				
00069h				
0006Ah				
0006Bh				
0006Ch				
0006Dh				
0006Eh				
0006Fh				
00070h				
00071h				
00072h	VCMP1IC	Interrupt Control Register	00h	
00073h	VCMP2IC	Interrupt Control Register	00h	
00074h				
00075h	TSCUIC	Interrupt Control Register	00h	
00076h				
00077h				
00078h				
00079h				

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.5 SFR Information (5) (1)

Address	Symbol	Register Name	After Reset	Remarks
000FAh				
000FBh				
000FCh				
000FDh				
000FEh				
000FFh				
00100h				
00101h				
00102h				
00103h				
00104h				
00105h				
00106h				
00107h				
00108h				
00109h				
0010Ah				
0010Bh				
0010Ch				
0010Dh				
0010Eh				
0010Fh				
00110h	TRJ_0	Timer RJ_0 Counter Register	FFFFh	
00111h				
00112h	TRJCR_0	Timer RJ_0 Control Register	00h	
00113h	TRJIOC_0	Timer RJ_0 I/O Control Register	00h	
00114h	TRJMR_0	Timer RJ_0 Mode Register	00h	
00115h	TRJISR_0	Timer RJ_0 Event Pin Select Register	00h	
00116h				
00117h				
00118h				
00119h				
0011Ah				
0011Bh				
0011Ch				
0011Dh				
0011Eh				
0011Fh				
00120h				
00121h				
00122h				
00123h				
00124h				
00125h				
00126h				
00127h				
00128h				
00129h				
0012Ah				
0012Bh				
0012Ch				
0012Dh				
0012Eh				
0012Fh				
00130h	TRBCR_0	Timer RB2_0 Control Register	00h	
00131h	TRBOCR_0	Timer RB2_0 One-Shot Control Register	00h	
00132h	TRBIOC_0	Timer RB2_0 I/O Control Register	00h	
00133h	TRBMR_0	Timer RB2_0 Mode Register	00h	
00134h	TRBPRES_0	Timer RB2_0 Prescaler Register	FFh	
00135h	TRBPR_0	Timer RB2_0 Primary Register	FFh	
00136h	TRBSC_0	Timer RB2_0 Secondary Register	FFh	
00137h	TRBIR_0	Timer RB2_0 Interrupt Request Register	00h	
00138h	TRCNT_0	Timer RC_0 Counter	0000h	
00139h				

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.6 SFR Information (6) (1)

Address	Symbol	Register Name	After Reset	Remarks
0013Ah	TRCGRA_0	Timer RC_0 General Register A	FFFFh	
0013Bh				
0013Ch	TRCGRB_0	Timer RC_0 General Register B	FFFFh	
0013Dh				
0013Eh	TRCGRC_0	Timer RC_0 General Register C	FFFFh	
0013Fh				
00140h	TRCGRD_0	Timer RC_0 General Register D	FFFFh	
00141h				
00142h	TRCMR_0	Timer RC_0 Mode Register	01001000b	
00143h	TRCCR1_0	Timer RC_0 Control Register 1	00h	
00144h	TRCIER_0	Timer RC_0 Interrupt Enable Register	01110000b	
00145h	TRCSR_0	Timer RC_0 Status Register	01110000b	
00146h	TRCIOR0_0	Timer RC_0 I/O Control Register 0	10001000b	
00147h	TRCIOR1_0	Timer RC_0 I/O Control Register 1	10001000b	
00148h	TRCCR2_0	Timer RC_0 Control Register 2	00011000b	
00149h	TRCDF_0	Timer RC_0 Digital Filter Function Select Register	00h	
0014Ah	TRCOER_0	Timer RC_0 Output Enable Register	01111111b	
0014Bh	TRCADCR_0	Timer RC_0 A/D Conversion Trigger Control Register	11110000b	
0014Ch	TRCOPR_0	Timer RC_0 Output Waveform Manipulation Register	00h	
0014Dh	TRCELCCR_0	Timer RC_0 ELC Cooperation Control Register	00h	
0014Eh				
0014Fh				
00150h				
00151h				
00152h				
00153h				
00154h				
00155h				
00156h				
00157h				
00158h				
00159h				
0015Ah				
0015Bh				
0015Ch				
0015Dh				
0015Eh				
0015Fh				
00160h				
00161h				
00162h				
00163h				
00164h				
00165h				
00166h				
00167h				
00168h				
00169h				
0016Ah				
0016Bh				
0016Ch				
0016Dh				
0016Eh				
0016Fh				
00170h	TRESEC	Timer RE2 Counter Data Register Timer RE2 Second Data Register	00h	
00171h	TREMIN	Timer RE2 Compare Data Register Timer RE2 Minute Data Register	00h	
00172h	TREHR	Timer RE2 Hour Data Register	00h	
00173h	TREWK	Timer RE2 Day-of-the-Week Data Register	00h	
00174h	TREDY	Timer RE2 Day Data Register	00000001b	
00175h	TREMON	Timer RE2 Month Data Register	00000001b	
00176h	TREYR	Timer RE2 Year Data Register	00h	
00177h	TRECR	Timer RE2 Control Register	00000100b	
00178h	TRECSR	Timer RE2 Count Source Select Register	00001000b	
00179h	TREADJ	Timer RE2 Clock Error Correction Register	00h	

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.12 SFR Information (12) ⁽¹⁾

Address	Symbol	Register Name	After Reset	Remarks
06B00h	TSCUCR0	TSCU Control Register 0	0000h	
06B01h				
06B02h	TSCUCR1	TSCU Control Register 1	000000000010000b	
06B03h				
06B04h	TSCUMR	TSCU Mode Register	000000001000000b	
06B05h				
06B06h	TSCUTCRA	TSCU Timing Control Register 0A	000000000111111b	
06B07h				
06B08h	TSCUTCROB	TSCU Timing Control Register 0B	000000000111111b	
06B09h				
06B0Ah	TSCUTCRI	TSCU Timing Control Register 1	000000000000001b	
06B0Bh				
06B0Ch	TSCUTCRI2	TSCU Timing Control Register 2	0000h	
06B0Dh				
06B0Eh	TSCUTCRI3	TSCU Timing Control Register 3	0000h	
06B0Fh				
06B10h	TSCUCHC	TSCU Channel Control Register	0011111100000000b	
06B11h				
06B12h	TSCUFR	TSCU Flag Register	0000h	
06B13h				
06B14h	TSCUSTC	TSCU Status Counter Register	0000h	
06B15h				
06B16h	TSCUSCS	TSCU Secondary Counter Set Register	000000000010000b	
06B17h				
06B18h	TSCUSCC	TSCU Secondary Counter	000000000010000b	
06B19h				
06B1Ah	TSCUDBR	TSCU Data Buffer Register	0000h	
06B1Bh				
06B1Ch	TSCUPRC	TSCU Primary Counter	0000h	
06B1Dh				
06B1Eh	TSCURVR0	TSCU Random Value Store Register 0	0000h	
06B1Fh				
06B20h	TSCURVR1	TSCU Random Value Store Register 1	0000h	
06B21h				
06B22h	TSCURVR2	TSCU Random Value Store Register 2	0000h	
06B23h				
06B24h	TSCURVR3	TSCU Random Value Store Register 3	0000h	
06B25h				
06B26h	TSIE0	TSCU Input Enable Register 0	0000h	
06B27h				
06B28h	TSIE1	TSCU Input Enable Register 1	0000h	
06B29h				
06B2Ah	TSIE2	TSCU Input Enable Register 2	0000h	
06B2Bh				
06B2Ch	TSCHSEL0	TSCUCHXA Select Register 0	0000h	
06B2Dh				
06B2Eh	TSCHSEL1	TSCUCHXA Select Register 1	0000h	
06B2Fh				
06B30h	TSCHSEL2	TSCUCHXA Select Register 2	0000h	
06B31h				
06B32h to 06BFFh				
06C00h		Area for storing DTC transfer vector 0	XXh	
06C01h		Area for storing DTC transfer vector 1	XXh	
06C02h		Area for storing DTC transfer vector 2	XXh	
06C03h		Area for storing DTC transfer vector 3	XXh	
06C04h		Area for storing DTC transfer vector 4	XXh	
06C05h				
06C06h				
06C07h				
06C08h		Area for storing DTC transfer vector 8	XXh	
06C09h		Area for storing DTC transfer vector 9	XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

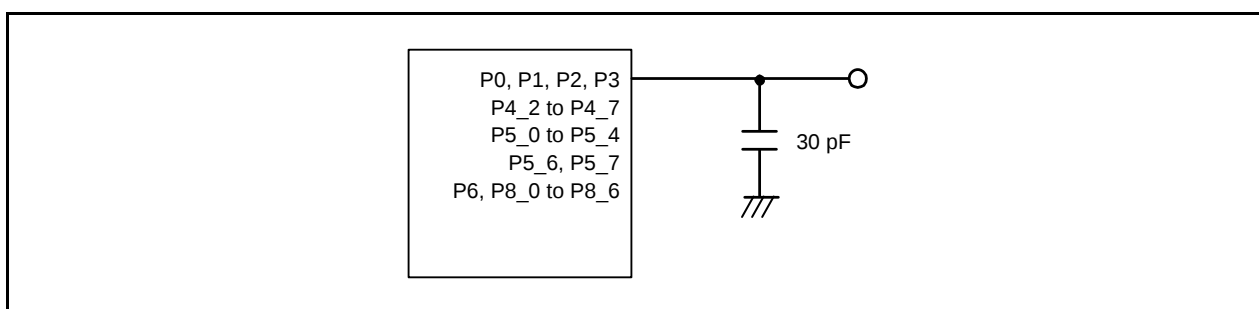


Figure 4.1 Timing Measurement Circuit for Ports P0, P1, P2, P3, P4_2 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6, and P8_0 to P8_6

Table 4.6 Flash Memory (Data flash Block A to Block D) Characteristics
(V_{cc} = 2.7 V to 5.5 V, T_{opr} = –20°C to 85°C (N version)/–40°C to 85°C (D version),
unless otherwise specified)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽¹⁾		10,000 ⁽²⁾	—	—	times
—	Byte program time (Program and erase endurance ≤ 1,000 times)		—	160	950	μs
—	Byte program time (Program and erase endurance > 1,000 times)		—	300	950	μs
—	Block erase time (Program and erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (Program and erase endurance > 1,000 times)		—	0.3	1	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	3 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		—	—	30 + CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		–20 (N ver.) –40 (D ver.)	—	85	°C
—	Data hold time ⁽⁶⁾	Ambient temperature = 55°C ⁽⁷⁾	20	—	—	year

Notes:

- Definition of programming/erasure endurance
 The programming and erasure endurance is defined on a per-block basis.
 If the programming and erasure endurance is n (n = 100, 1,000 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
 However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- The data hold time includes time that the power supply is off or the clock is not supplied.
- The data hold time includes 7,000 hours under an environment of ambient temperature 85°C.

Table 4.8 Voltage Detection 1 Circuit Characteristics
(Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/
–40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
Vdet1	Voltage detection level Vdet1_0 ⁽¹⁾	When Vcc falls	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 ⁽¹⁾	When Vcc falls	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 ⁽¹⁾	When Vcc falls	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 ⁽¹⁾	When Vcc falls	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 ⁽¹⁾	When Vcc falls	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 ⁽¹⁾	When Vcc falls	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 ⁽¹⁾	When Vcc falls	2.80	3.10	3.40	V
	Voltage detection level Vdet1_7 ⁽¹⁾	When Vcc falls	2.95	3.25	3.55	V
	Voltage detection level Vdet1_8 ⁽¹⁾	When Vcc falls	3.10	3.40	3.70	V
	Voltage detection level Vdet1_9 ⁽¹⁾	When Vcc falls	3.25	3.55	3.85	V
	Voltage detection level Vdet1_A ⁽¹⁾	When Vcc falls	3.40	3.70	4.00	V
	Voltage detection level Vdet1_B ⁽¹⁾	When Vcc falls	3.55	3.85	4.15	V
	Voltage detection level Vdet1_C ⁽¹⁾	When Vcc falls	3.70	4.00	4.30	V
	Voltage detection level Vdet1_D ⁽¹⁾	When Vcc falls	3.85	4.15	4.45	V
	Voltage detection level Vdet1_E ⁽¹⁾	When Vcc falls	4.00	4.30	4.60	V
	Voltage detection level Vdet1_F ⁽¹⁾	When Vcc falls	4.15	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_6 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time ⁽²⁾	At the falling of Vcc from 5 V to (Vdet1 – 0.1) V	—	60	150	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	1.7	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

Notes:

1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 4.9 Voltage Detection 2 Circuit Characteristics
(Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/
–40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level Vdet2_0	When Vcc falls	3.70	4.00	4.30	V
—	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		—	0.1	—	μs
—	Voltage detection 2 circuit response time ⁽¹⁾	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	—	20	150	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	1.7	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽²⁾		—	—	100	μs

Notes:

1. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 4.10 Power-On Reset Circuit Characteristics ⁽¹⁾
(Measurement conditions: V_{CC} = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/
–40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
trth	External power VCC rise gradient		0	—	50,000	mV/msec

Note:

- To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

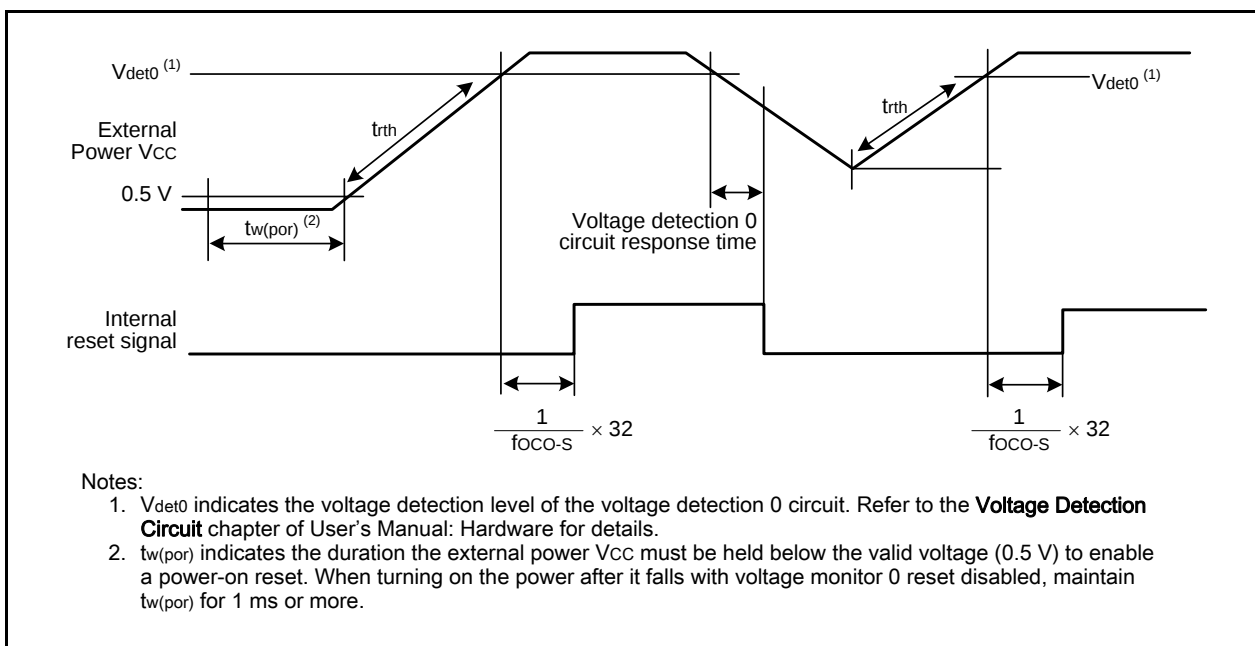


Figure 4.3 Power-on Reset Circuit Characteristics

Table 4.11 High-Speed On-Chip Oscillator Circuit Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	V _{CC} = 1.8 V to 5.5 V, –20°C ≤ Topr ≤ 85°C	—	40	—	MHz
	High-speed on-chip oscillator frequency when 01b or 10b is written to bits FRA25 and FRA24 in the FRA2 register ⁽¹⁾	(N version) –40°C ≤ Topr ≤ 85°C (D version)	—	36.864	—	MHz
	High-speed on-chip oscillator frequency when 10b is written to bits FRA25 and FRA24 in the FRA2 register		—	32	—	MHz
	High-speed on-chip oscillator frequency dependence on temperature and power supply voltage ⁽²⁾		–1.5	—	1.5	%
—	Oscillation stability time	V _{CC} = 5.0 V, Topr = 25°C	—	250	—	μs
—	Self power consumption at oscillation	V _{CC} = 5.0 V, Topr = 25°C	—	500	—	μA

Notes:

- This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.
- This indicates the precision error for the oscillation frequency of the high-speed on-chip oscillator.

Table 4.12 Low-Speed On-Chip Oscillator Circuit Characteristics
(Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/
–40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
f _{LOCO}	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	—	30	100	μs
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	—	3	—	μA

Table 4.13 Power Supply Circuit Characteristics
(Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/
–40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t _{d(P-R)}	Time for internal power supply stabilization during power-on ⁽¹⁾		—	—	2,000	μs

Note:

1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

4.4 DC Characteristics

Table 4.14 DC Characteristics (1) [4.2 V ≤ V_{CC} ≤ 5.5 V]
(Measurement conditions: V_{CC} = 1.8 V to 5.5 V, Topr = −20°C to 85°C (N version)/
−40°C to 85°C (D version))

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output high voltage	Other than XOUT	Drive capacity is high	I _{OH} = −20 mA	V _{CC} − 2.0	—	V _{CC}	V
			Drive capacity is low	I _{OH} = −5 mA	V _{CC} − 2.0	—	V _{CC}	V
				I _{OH} = −200 μA	V _{CC} − 0.3	—	V _{CC}	V
		XOUT		I _{OH} = −200 μA	1.0	—	V _{CC}	V
V _{OL}	Output low voltage	Other than XOUT	Drive capacity is high	I _{OL} = 20 mA	—	—	2.0	V
			Drive capacity is low	I _{OL} = 5 mA	—	—	2.0	V
				I _{OL} = 200 μA	—	—	0.45	V
		XOUT		I _{OL} = 200 μA	—	—	0.5	V
V _{T+} –V _{T–}	Hysteresis	INT0 to INT4, K10 to K13, TRJIO_0, TRCCLK_0, TRCTRG_0, TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0, CLK_0, CLK_1, RXD_0, RXD_1, CTS2, SCL2, SDA2, CLK2, RXD2, SCL_0, SDA_0, SSI_0, SCS_0, SSCK_0, SSO_0			0.1	1.2	—	V
		RESET	V _{CC} = 5.0 V		0.1	1.2	—	V
I _{IH}	Input high current		V _I = 5.0 V		—	—	1.0	μA
I _{IL}	Input low current		V _I = 0 V		—	—	−1.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V		25	50	100	kΩ
R _{FXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R _{FXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

4.5 AC Characteristics

**Table 4.20 Timing Requirements of Clock Synchronous Serial I/O with Chip Select
(during Master Operation)**
(Measurement conditions: $V_{CC} = 1.8\text{ V to }5.5\text{ V}$, $T_{opr} = -20^{\circ}\text{C to }85^{\circ}\text{C}$ (N version)/
 $-40^{\circ}\text{C to }85^{\circ}\text{C}$ (D version))

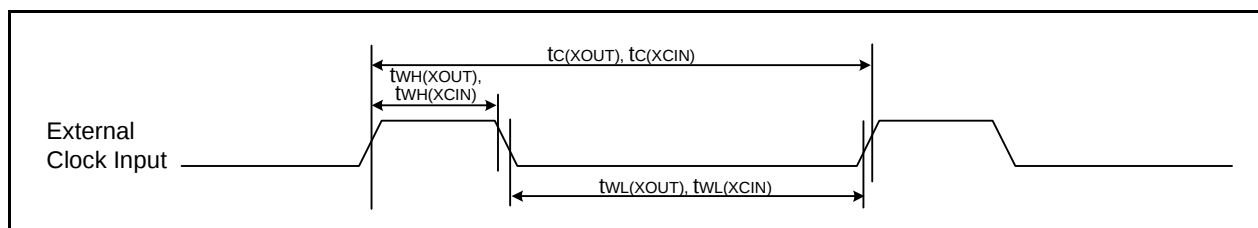
Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time		4.00	—	—	tcyc (1)
thi	SSCK clock high width		0.40	—	0.60	tsucyc
tlo	SSCK clock low width		0.40	—	0.60	tsucyc
trise	SSCK clock rising time	$2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	—	—	0.50	tcyc (1)
		$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$	—	—	1.00	tcyc (1)
tfall	SSCK clock falling time	$2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	—	—	0.50	tcyc (1)
		$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$	—	—	1.00	tcyc (1)
tsu	SSI, SSO data input setup time	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	60	—	—	ns
		$2.7\text{ V} \leq V_{CC} < 4.5\text{ V}$	70	—	—	ns
		$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$	100	—	—	ns
th	SSI, SSO data input hold time	$2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	2.00	—	—	tcyc (1)
		$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$	2.00	—	—	tcyc (1)
tlead	$\overline{\text{SCS}}$ -SCK output delay time		$0.5\text{ tsucyc} - 1\text{ tcyc}$	—	—	ns
tlag	SCK- $\overline{\text{SCS}}$ output valid time		$0.5\text{ tsucyc} - 1\text{ tcyc}$	—	—	ns
tod	SSO data output delay time	$2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	—	—	30.00	ns
		$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$	—	—	1.00	tcyc (1)

Note:

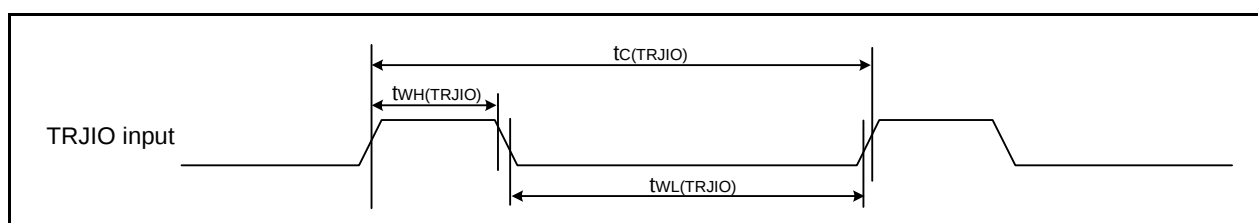
1. $1\text{tcyc} = 1/f_1$ (s)

Table 4.22 External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
t _c (XOUT)	XOUT input cycle time	200	—	50	—	50	—	ns
t _{WH} (XOUT)	XOUT input high width	90	—	24	—	24	—	ns
t _{WL} (XOUT)	XOUT input low width	90	—	24	—	24	—	ns
t _c (XCIN)	XCIN input cycle time	14	—	14	—	14	—	μs
t _{WH} (XCIN)	XCIN input high width	7	—	7	—	7	—	μs
t _{WL} (XCIN)	XCIN input low width	7	—	7	—	7	—	μs

**Figure 4.7 External Clock Input Timing Diagram****Table 4.23 Timing Requirements of TRJIO**

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
t _c (TRJIO)	TRJIO input cycle time	500	—	300	—	100	—	ns
t _{WH} (TRJIO)	TRJIO input high width	200	—	120	—	40	—	ns
t _{WL} (TRJIO)	TRJIO input low width	200	—	120	—	40	—	ns

**Figure 4.8 Input Timing of TRJIO**

Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

