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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2136csnfa-30

1.1.2 Specifications

Tables 1.1 and 1.2 outline Specifications.

Table 1.1 Specifications (1)

Item	Function	Description
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (CPU clock = 20 MHz, VCC = 2.7 V to 5.5 V) 200 ns (CPU clock = 5 MHz, VCC = 1.8 V to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, data flash	Refer to **Table 1.3 Product List**.
Voltage detection	Voltage detection circuit	• Power-on reset • Voltage detection with three check points (the detection levels for voltage detection 0 and voltage detection 1 can be selected.)
I/O ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 59, selectable pull-up resistor • High current drive ports: 59
Clock	Clock generation circuits	• 4 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Divided by 1, 2, 4, 8, or 16 can be selected • Low-power mode: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Number of interrupt vectors: 69 • External interrupt inputs: 9 (INT × 5, key input × 4) • Priority levels: 7
Event link controller (ELC)		• Events output from peripheral functions can be linked to events input to different peripheral functions. (30 sources × 10 types of event link operations) • Events can be handled independently from interrupt requests.
Watchdog timer		• 14 bits × 1 • Selectable reset start function • Selectable low-speed on-chip oscillator for the watchdog timer
DTC (data transfer controller)		• 1 channel • Activation sources: 27 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timers RJ_0	16 bits × 1: 1 circuit integrated on-chip Timer mode (periodic timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB2_0	16 bits × 1: 1 circuit integrated on-chip Timer mode (periodic timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timers RC_0	16 bits (with 4 capture/compare registers) × 1: 1 circuit integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)
	Timer RE2	8 bits × 1 Compare match timer mode, real-time clock mode

1.3 Block Diagram

Figure 1.2 shows the Block Diagram.

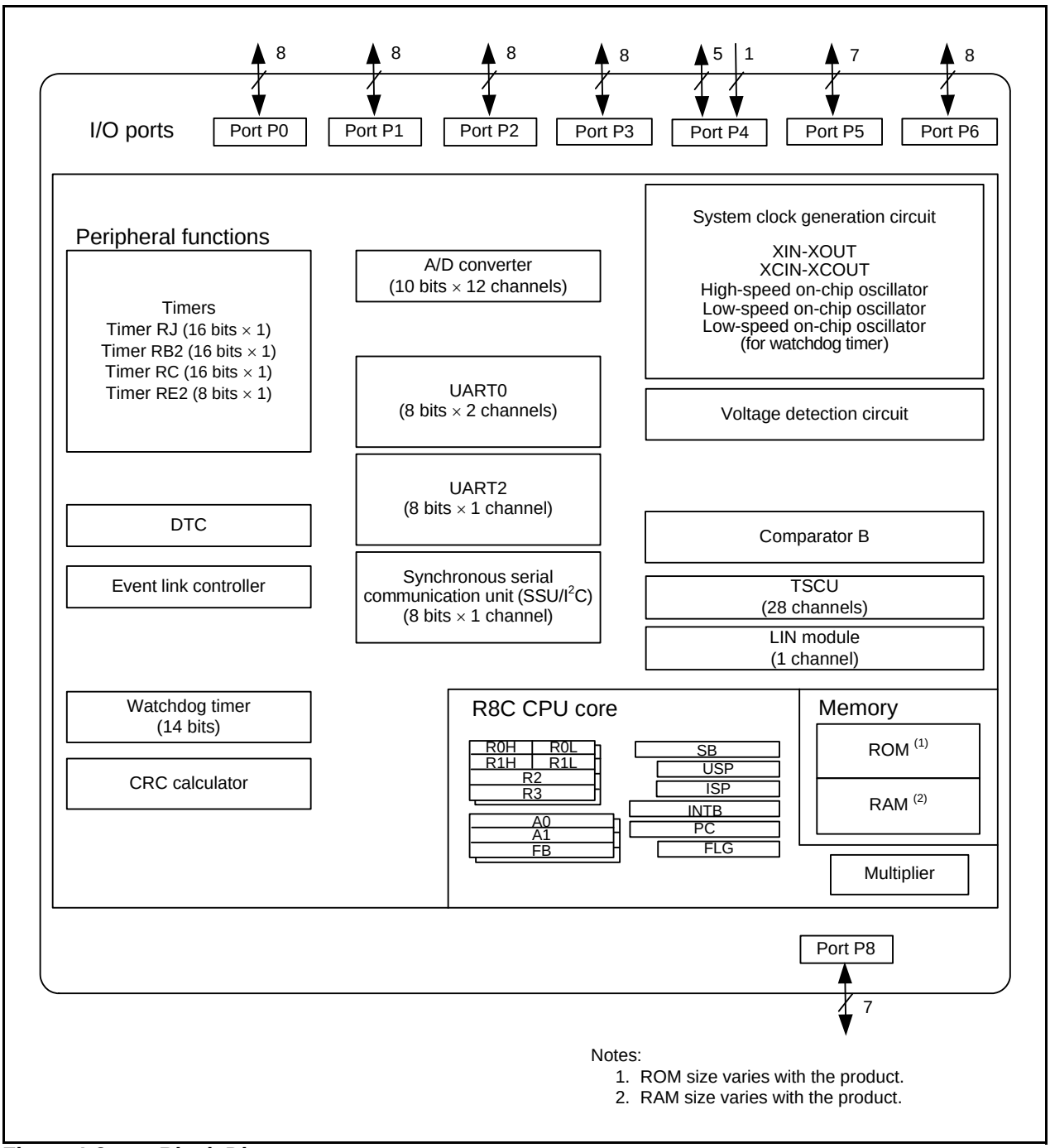


Figure 1.2 Block Diagram

Table 1.6 Pin Name Information by Pin Number (Timer RC, Timer RE2, and Others)

Port	Pin No.	Timer RC						Timer RE2	Others		
		TRCCLK_0	TRCIOA_0	TRCIOB_0	TRCIOC_0	TRCIOD_0	TRCTRG_0	TMRE2O			
P0_0	56		TRCIOA_0				TRCTRG_0		AN7		
P0_1	55		TRCIOA_0				TRCTRG_0		AN6		
P0_2	54		TRCIOA_0				TRCTRG_0		AN5		
P0_3	53			TRCIOB_0					AN4		
P0_4	52			TRCIOB_0				TMRE2O	AN3		
P0_5	51			TRCIOB_0					AN2		
P0_6	50					TRCIOD_0			AN1		
P0_7	49				TRCIOC_0				AN0		
P1_0	48					TRCIOD_0			AN8	$\overline{KI0}$	
P1_1	47		TRCIOA_0				TRCTRG_0		AN9	$\overline{KI1}$	
P1_2	46			TRCIOB_0					AN10	$\overline{KI2}$	
P1_3	45				TRCIOC_0				AN11	$\overline{KI3}$	
P1_4	44	TRCCLK_0									
P1_5	43										
P1_6	42								IVREF1		CH00
P1_7	41								IVCMP1		CH01
P2_0	27			TRCIOB_0							CH16
P2_1	26				TRCIOC_0						CH17
P2_2	25					TRCIOD_0					CH18
P2_3	24										CH19
P2_4	23										CH20
P2_5	22										CH21
P2_6	21										CH22
P2_7	20										CH23
P3_0	1										CH24
P3_1	29										CH10
P3_2	64										CH25
P3_3	19	TRCCLK_0							IVCMP3		
P3_4	18				TRCIOC_0				IVREF3		
P3_5	17					TRCIOD_0					
P3_6	28										CH11
P3_7	16										
P4_2	2								VREF		
P4_3	4								XCIN		
P4_4	5								XCOUT		
P4_5	40								$\overline{ADTRG}$		CH02
P4_6	9								XIN		
P4_7	7								XOUT		
P5_0	15	TRCCLK_0									
P5_1	14		TRCIOA_0				TRCTRG_0				
P5_2	13			TRCIOB_0							
P5_3	12				TRCIOC_0						
P5_4	11					TRCIOD_0					
P5_6	63										CH27
P5_7	62										CH28
P6_0	61							TMRE2O			CH31
P6_1	60										CH32
P6_2	59										CH33
P6_3	58										CH34
P6_4	57										CH35
P6_5	39			TRCIOB_0							CH03
P6_6	38				TRCIOC_0						CH04
P6_7	37					TRCIOD_0					CH05
P8_0	36										CH06
P8_1	35										CH07
P8_2	34										CHxA0
P8_3	33										CHxA1
P8_4	32										CHxB
P8_5	31										CHxC
P8_6	30										CH08

1.5 Pin Functions

Tables 1.7 and 1.8 list Pin Functions.

Table 1.7 Pin Functions (1)

Item	Pin Name	I/O	Description
Power supply input	VCC, VSS	—	Apply 1.8 V through 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply input for the A/D converter. Connect a capacitor between pins AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Applying a low level to this pin resets the MCU.
MODE	MODE	I	Connect this pin to the VCC pin via a resistor.
XIN clock input	XIN	I	I/O for the XIN clock generation circuit. Connect a ceramic resonator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	I/O for the XCIN clock generation circuit. Connect a crystal oscillator between pins XCIN and XCOUT. (1) To use an external clock, input it to the XCOUT pin and leave the XCIN pin open.
XCIN clock output	XCOUT	I/O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$	I	$\overline{\text{INT}}$ interrupt input.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input.
Timer RJ_0	TRJIO_0	I/O	Input/output for timer RJ.
	TRJO_0	O	Output for timer RJ.
Timer RB2_0	TRBO_0	O	Output for timer RB2.
Timer RC_0	TRCCLK_0	I	External clock input.
	TRCTRG_0	I	External trigger input.
	TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0	I/O	Input/output for timer RC.
Timer RE2	TMRE2O	O	Divided clock output.
Serial interface (UART0)	CLK_0, CLK_1	I/O	Transfer clock input/output.
	RXD_0, RXD_1	I	Serial data input.
	TXD_0, TXD_1	O	Serial data output.
Serial interface (UART2)	$\overline{\text{CTS2}}$	I	Input for transmission control.
	$\overline{\text{RTS2}}$	O	Output for reception control.
	SCL2	I/O	I^2C mode clock input/output.
	SDA2	I/O	I^2C mode data input/output.
	RXD2	I	Serial data input.
	TXD2	O	Serial data output.
	CLK2	I/O	Transfer clock input/output.
Synchronous serial communication unit (SSU_0)	SSI_0	I/O	Data input/output.
	$\overline{\text{SCS\_0}}$	I/O	Chip-select input/output.
	$\overline{\text{SSCK\_0}}$	I/O	Clock input/output.
	SSO_0	I/O	Data input/output.
I^2C bus (I^2C_0)	SCL_0	I/O	Clock input/output.
	SDA_0	I/O	Data input/output.
Reference voltage input	VREF	I	Reference voltage input for the A/D converter.

Note:
1. Contact the oscillator manufacturer for oscillation characteristics.

Table 1.8 Pin Functions (2)

Item	Pin Name	I/O	Description
A/D converter	AN0 to AN11	I	Analog input for the A/D converter.
	$\overline{\text{ADTRG}}$	I	External trigger input for the A/D converter.
Comparator B	IVCMP1, IVCMP3	I	Analog voltage input for comparator B.
	IVREF1, IVREF3	I	Reference voltage input for comparator B.
Touch sensor control unit	CHxA0, CHxA1, CHxB, CHxC	I/O	Control pins for electrostatic capacitive touch detection.
	CH00 to CH08, CH10, CH11, CH16 to CH25, CH27, CH28, CH31 to CH35	I	Electrostatic capacitive touch detection pins.
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6_0 to P6_7, P8_0 to P8_6	I/O	8-bit CMOS input/output ports. Each port has an I/O select direction register, enabling switching input and output for each pin. For input ports, the presence or absence of a pull-up resistor can be selected by a program. All ports can be used as LED drive (high drive) ports.
Input port	P4_2	I	Input-only port.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts. Interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction for a software interrupt numbered from 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns eight processor interrupt priority levels from 0 to 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

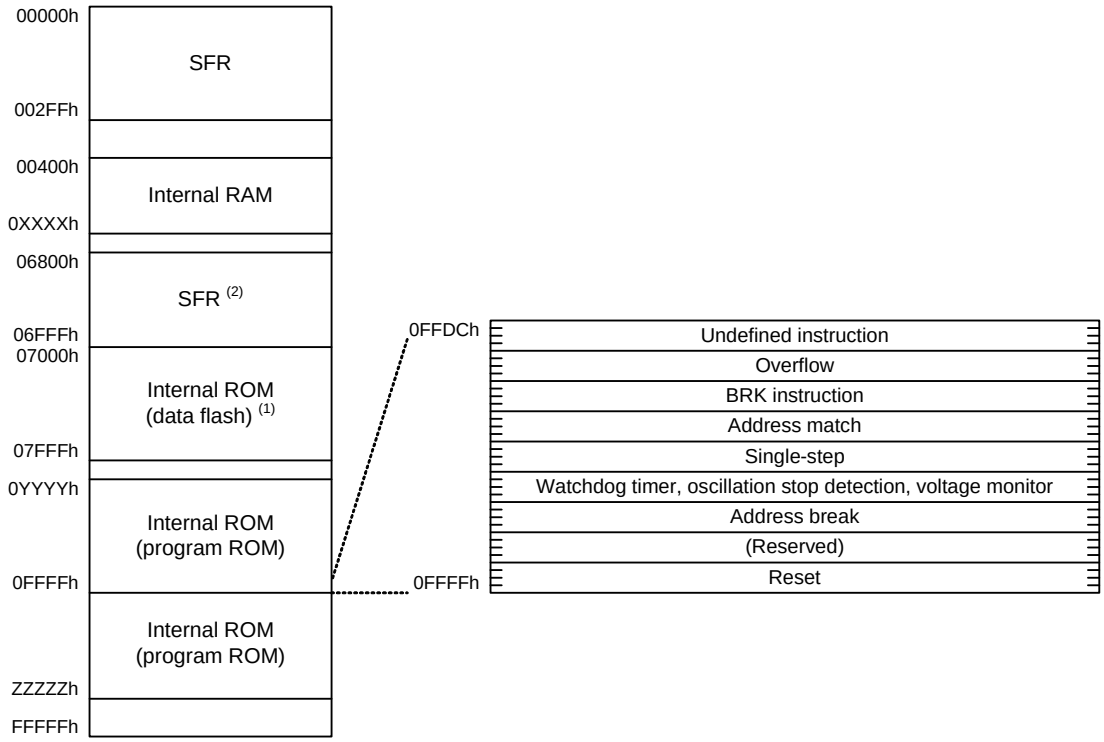
2.8.10 Reserved Bit

The write value must be 0. The read value is undefined.

3. Address Space

3.1 Memory Map

Figure 3.1 shows the Memory Map. The R8C/36T-A Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. Up to 32 Kbytes of the internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. The area in excess of 32 Kbytes is allocated at higher addresses, beginning with address 10000h. For example, a 64-Kbyte internal ROM is allocated at addresses 08000h to 17FFFh.
The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated at addresses 07000h to 07FFFh.
The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM is allocated at addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated at addresses 00000h to 02FFFh and addresses 06800h to 06FFFh. Peripheral function control registers are allocated here. All unallocated locations within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. Addresses 06800h to 06FFFh are used for the ELC, DTC, and TSCU SFR areas.
3. The blank areas are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM	
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh
R5F21368SNFP/FA, R5F21368SDFP/FA	64 Kbytes	08000h	17FFFh	6 Kbytes	01BFFh
R5F21368SNFP/FA, R5F21368SDFP/FA	96 Kbytes	08000h	1FFFFh	8 Kbytes	023FFh
R5F21368SNFP/FA, R5F21368SDFP/FA	128 Kbytes	08000h	27FFFh	10 Kbytes	02BFFh

Figure 3.1 Memory Map

Table 3.2 SFR Information (2) (1)

Address	Symbol	Register Name	After Reset	Remarks
0003Ah	VW2C	Voltage Monitor 2 Circuit Control Register	10001010b	
0003Bh				
0003Ch				
0003Dh				
0003Eh				
0003Fh				
00040h				
00041h	FMRDYIC	Interrupt Control Register	00h	
00042h				
00043h				
00044h				
00045h				
00046h	INT4IC	Interrupt Control Register	00h	
00047h	TRCIC_0	Interrupt Control Register	00h	
00048h				
00049h				
0004Ah	TRE2IC	Interrupt Control Register	00h	
0004Bh	U2TIC	Interrupt Control Register	00h	
0004Ch	U2RIC	Interrupt Control Register	00h	
0004Dh	KUPIC	Interrupt Control Register	00h	
0004Eh	ADIC	Interrupt Control Register	00h	
0004Fh	SSUIC_0/IICIC_0	Interrupt Control Register	00h	
00050h				
00051h	U0TIC_0	Interrupt Control Register	00h	
00052h	U0RIC_0	Interrupt Control Register	00h	
00053h	U0TIC_1	Interrupt Control Register	00h	
00054h	U0RIC_1	Interrupt Control Register	00h	
00055h	INT2IC	Interrupt Control Register	00h	
00056h	TRJIC_0	Interrupt Control Register	00h	
00057h				
00058h	TRB2IC_0	Interrupt Control Register	00h	
00059h	INT1IC	Interrupt Control Register	00h	
0005Ah	INT3IC	Interrupt Control Register	00h	
0005Bh				
0005Ch				
0005Dh	INT0IC	Interrupt Control Register	00h	
0005Eh	U2BCNIC	Interrupt Control Register	00h	
0005Fh				
00060h				
00061h				
00062h				
00063h				
00064h				
00065h				
00066h				
00067h				
00068h				
00069h				
0006Ah				
0006Bh				
0006Ch				
0006Dh				
0006Eh				
0006Fh				
00070h				
00071h				
00072h	VCMP1IC	Interrupt Control Register	00h	
00073h	VCMP2IC	Interrupt Control Register	00h	
00074h				
00075h	TSCUIC	Interrupt Control Register	00h	
00076h				
00077h				
00078h				
00079h				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.3 SFR Information (3) (1)

Address	Symbol	Register Name	After Reset	Remarks
0007Ah				
0007Bh				
0007Ch				
0007Dh				
0007Eh				
0007Fh				
00080h	U0MR_0	UART0_0 Transmit/Receive Mode Register	00h	
00081h	U0BRG_0	UART0_0 Bit Rate Register	XXh	
00082h	U0TB_0	UART0_0 Transmit Buffer Register	XXh	
00083h			XXh	
00084h	U0C0_0	UART0_0 Transmit/Receive Control Register 0	00001000b	
00085h	U0C1_0	UART0_0 Transmit/Receive Control Register 1	00000010b	
00086h	U0RB_0	UART0_0 Receive Buffer Register	XXXXh	
00087h				
00088h	U0IR_0	UART0_0 Interrupt Flag and Enable Register	00h	
00089h				
0008Ah				
0008Bh				
0008Ch	LINCR2_0	LIN_0 Special Function Register	00h	
0008Dh				
0008Eh	LINCT_0	LIN_0 Control Register	00h	
0008Fh	LINST_0	LIN_0 Status Register	00h	
00090h	U0MR_1	UART0_1 Transmit/Receive Mode Register	00h	
00091h	U0BRG_1	UART0_1 Bit Rate Register	XXh	
00092h	U0TB_1	UART0_1 Transmit Buffer Register	XXh	
00093h			XXh	
00094h	U0C0_1	UART0_1 Transmit/Receive Control Register 0	00001000b	
00095h	U0C1_1	UART0_1 Transmit/Receive Control Register 1	00000010b	
00096h	U0RB_1	UART0_1 Receive Buffer Register	XXXXh	
00097h				
00098h	U0IR_1	UART0_1 Interrupt Flag and Enable Register	00h	
00099h				
0009Ah				
0009Bh				
0009Ch				
0009Dh				
0009Eh				
0009Fh				
000A0h				
000A1h				
000A2h				
000A3h				
000A4h				
000A5h				
000A8h				
000A9h				
000AAh				
000ABh				
000ACh				
000ADh				
000AEh				
000AFh				
000B0h				
000B1h				
000B4h				
000B5h				
000B8h				
000B9h				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.4 SFR Information (4) (1)

Address	Symbol	Register Name	After Reset	Remarks
000BAh				
000BBh				
000BCh				
000BDh				
000BEh				
000BFh				
000C0h	U2MR	UART2 Transmit/Receive Mode Register	00h	
000C1h	U2BRG	UART2 Bit Rate Register	00h	
000C2h	U2TB	UART2 Transmit Buffer Register	00h	
000C3h			00h	
000C4h	U2C0	UART2 Transmit/Receive Control Register 0	00001000b	
000C5h	U2C1	UART2 Transmit/Receive Control Register 1	00000010b	
000C6h	U2RB	UART2 Receive Buffer Register	0000h	
000C7h				
000C8h	U2RXDF	UART2 Digital Filter Function Select Register	00h	
000C9h				
000CAh				
000CBh				
000CCh				
000CDh				
000CEh				
000CFh				
000D0h	U2SMR5	UART2 Special Mode Register 5	00h	
000D1h				
000D2h				
000D3h				
000D4h	U2SMR4	UART2 Special Mode Register 4	00h	
000D5h	U2SMR3	UART2 Special Mode Register 3	00h	
000D6h	U2SMR2	UART2 Special Mode Register 2	00h	
000D7h	U2SMR	UART2 Special Mode Register	00h	
000D8h				
000D9h				
000DAh				
000DBh				
000DCh				
000DDh				
000DEh				
000DFh				
000E0h	IICCR_0	I²C_0 Control Register	00001110b	
000E1h	SSBR_0	SS_0 Bit Counter Register	11111000b	
000E2h	SITDR_0	SI_0 Transmit Data Register	FFh	
000E3h			FFh	
000E4h	SIRDR_0	SI_0 Receive Data Register	FFh	
000E5h			FFh	
000E6h	SICR1_0	SI_0 Control Register 1	00h	
000E7h	SICR2_0	SI_0 Control Register 2	01111101b	
000E8h	SIMR1_0	SI_0 Mode Register 1	00010000b	
000E9h	SIER_0	SI_0 Interrupt Enable Register	00h	
000EAh	SISR_0	SI_0 Status Register	00h	
000EBh	SIMR2_0	SI_0 Mode Register 2	00h	
000ECh				
000EDh				
000EEh				
000EFh				
000F0h				
000F1h				
000F2h				
000F3h				
000F4h				
000F5h				
000F6h				
000F7h				
000F8h				
000F9h				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.8 SFR Information (8) (1)

Address	Symbol	Register Name	After Reset	Remarks
0023Ah	MSTCR2	Module Standby Control Register 2	00h	
0023Bh	MSTCR3	Module Standby Control Register 3	00h	
0023Ch	MSTCR4	Module Standby Control Register 4	00h	
0023Dh				
0023Eh				
0023Fh				
00240h				
00241h				
00242h				
00243h				
00244h				
00245h				
00246h				
00247h				
00248h				
00249h				
0024Ah				
0024Bh				
0024Ch				
0024Dh				
0024Eh				
0024Fh				
00250h				
00251h				
00252h	FST	Flash Memory Status Register	10000X00b	
00253h				
00254h	FMR0	Flash Memory Control Register 0	00h	
00255h	FMR1	Flash Memory Control Register 1	00h	
00256h	FMR2	Flash Memory Control Register 2	00h	
00257h				
00258h				
00259h				
0025Ah				
0025Bh				
0025Ch				
0025Dh				
0025Eh				
0025Fh				
00260h	AIADR0L	Address Match Interrupt Address 0L Register	XXXXh	
00261h				
00262h	AIADR0H	Address Match Interrupt Address 0H Register	0000XXXXb	
00263h	AIEN0	Address Match Interrupt Enable 0 Register	00h	
00264h	AIADR1L	Address Match Interrupt Address 1L Register	XXXXh	
00265h				
00266h	AIADR1H	Address Match Interrupt Address 1H Register	0000XXXXb	
00267h	AIEN1	Address Match Interrupt Enable 1 Register	00h	
00268h				
00269h				
0026Ah				
0026Bh				
0026Ch				
0026Dh				
0026Eh				
0026Fh				
00270h				
00271h				
00272h				
00273h				
00274h				
00275h				
00276h				
00277h				
00278h				
00279h				
0027Ah				
0027Bh				
0027Ch				
0027Dh				
0027Eh				
0027Fh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.16 SFR Information (16) (1)

Address	Symbol	Register Name	After Reset	Remarks
06CD0h	DTCCR18	DTC Control Register 18	XXh	
06CD1h	DTBLS18	DTC Block Size Register 18	XXh	
06CD2h	DTCCT18	DTC Transfer Count Register 18	XXh	
06CD3h	DTRLD18	DTC Transfer Count Reload Register 18	XXh	
06CD4h	DTSAR18	DTC Source Address Register 18	XXXXh	
06CD5h				
06CD6h	DTDAR18	DTC Destination Address Register 18	XXXXh	
06CD7h				
06CD8h	DTCCR19	DTC Control Register 19	XXh	
06CD9h	DTBLS19	DTC Block Size Register 19	XXh	
06CDAh	DTCCT19	DTC Transfer Count Register 19	XXh	
06CDBh	DTRLD19	DTC Transfer Count Reload Register 19	XXh	
06CDCh	DTSAR19	DTC Source Address Register 19	XXXXh	
06CDDh				
06CDEh	DTDAR19	DTC Destination Address Register 19	XXXXh	
06CDFh				
06CE0h	DTCCR20	DTC Control Register 20	XXh	
06CE1h	DTBLS20	DTC Block Size Register 20	XXh	
06CE2h	DTCCT20	DTC Transfer Count Register 20	XXh	
06CE3h	DTRLD20	DTC Transfer Count Reload Register 20	XXh	
06CE4h	DTSAR20	DTC Source Address Register 20	XXXXh	
06CE5h				
06CE6h	DTDAR20	DTC Destination Address Register 20	XXXXh	
06CE7h				
06CE8h	DTCCR21	DTC Control Register 21	XXh	
06CE9h	DTBLS21	DTC Block Size Register 21	XXh	
06CEAh	DTCCT21	DTC Transfer Count Register 21	XXh	
06CEBh	DTRLD21	DTC Transfer Count Reload Register 21	XXh	
06CECh	DTSAR21	DTC Source Address Register 21	XXXXh	
06CEDh				
06CEEh	DTDAR21	DTC Destination Address Register 21	XXXXh	
06CEFh				
06CF0h	DTCCR22	DTC Control Register 22	XXh	
06CF1h	DTBLS22	DTC Block Size Register 22	XXh	
06CF2h	DTCCT22	DTC Transfer Count Register 22	XXh	
06CF3h	DTRLD22	DTC Transfer Count Reload Register 22	XXh	
06CF4h	DTSAR22	DTC Source Address Register 22	XXXXh	
06CF5h				
06CF6h	DTDAR22	DTC Destination Address Register 22	XXXXh	
06CF7h				
06CF8h	DTCCR23	DTC Control Register 23	XXh	
06CF9h	DTBLS23	DTC Block Size Register 23	XXh	
06CFAh	DTCCT23	DTC Transfer Count Register 23	XXh	
06CFBh	DTRLD23	DTC Transfer Count Reload Register 23	XXh	
06CFCh	DTSAR23	DTC Source Address Register 23	XXXXh	
06CFDh				
06CFEh	DTDAR23	DTC Destination Address Register 23	XXXXh	
06CFFh				
06D00h to 06FFFh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

4.2 Recommended Operating Conditions

Table 4.2 Recommended Operating Conditions (1)
(Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage					1.8	—	5.5	V
V_{SS}/AV_{SS}	Supply voltage					—	0	—	V
V_{IH}	Input high voltage	Other than CMOS input				0.8V_{CC}	—	V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.5V_{CC}	—	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.55V_{CC}	—	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.65V_{CC}	—	V_{CC}	V
				Input level selection: 0.5V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.65V_{CC}	—	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.7V_{CC}	—	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.8V_{CC}	—	V_{CC}	V
				Input level selection: 0.7V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.85V_{CC}	—	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.85V_{CC}	—	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.85V_{CC}	—	V_{CC}	V
		External clock input (XOUT)				1.2	—	V_{CC}	V
V_{IL}	Input low voltage	Other than CMOS input				0	—	0.2V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	—	0.2V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	—	0.2V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	—	0.2V_{CC}	V
				Input level selection: 0.5V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	—	0.4V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	—	0.3V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	—	0.2V_{CC}	V
				Input level selection: 0.7V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	—	0.55V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	—	0.45V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	—	0.35V_{CC}	V
		External clock input (XOUT)				0	—	0.4	V
$I_{OH(sum)}$	Peak sum output high current		Sum of all pins $I_{OH(peak)}$			—	—	–80	mA
$I_{OH(sum)}$	Average sum output high current		Sum of all pins $I_{OH(avg)}$			—	—	–40	mA
$I_{OH(peak)}$	Peak output high current		When drive capacity is low			—	—	–10	mA
			When drive capacity is high			—	—	–40	mA
$I_{OH(avg)}$	Average output high current		When drive capacity is low			—	—	–5	mA
			When drive capacity is high			—	—	–20	mA
$I_{OL(sum)}$	Peak sum output low current		Sum of all pins $I_{OL(peak)}$			—	—	80	mA
$I_{OL(sum)}$	Average sum output low current		Sum of all pins $I_{OL(avg)}$			—	—	40	mA
$I_{OL(peak)}$	Peak output low current		When drive capacity is low			—	—	10	mA
			When drive capacity is high			—	—	40	mA
$I_{OL(avg)}$	Average output low current		When drive capacity is low			—	—	5	mA
			When drive capacity is high			—	—	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
$f_{(XCIN)}$	XCIN clock input oscillation frequency				1.8 V ≤ V_{CC} ≤ 5.5 V	—	32.768	50	kHz
fHOCO	Count source for timer RC				2.7 V ≤ V_{CC} ≤ 5.5 V	32	—	40	MHz
fHOCO-F	fHOCO-F frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
—	System clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
$f_{(BCLK)}$	CPU clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz

Note:
1. The average output current indicates the average value of current measured during 100 ms.

Table 4.8 Voltage Detection 1 Circuit Characteristics (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (1)	When Vcc falls	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (1)	When Vcc falls	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (1)	When Vcc falls	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (1)	When Vcc falls	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (1)	When Vcc falls	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (1)	When Vcc falls	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (1)	When Vcc falls	2.80	3.10	3.40	V
	Voltage detection level Vdet1_7 (1)	When Vcc falls	2.95	3.25	3.55	V
	Voltage detection level Vdet1_8 (1)	When Vcc falls	3.10	3.40	3.70	V
	Voltage detection level Vdet1_9 (1)	When Vcc falls	3.25	3.55	3.85	V
	Voltage detection level Vdet1_A (1)	When Vcc falls	3.40	3.70	4.00	V
	Voltage detection level Vdet1_B (1)	When Vcc falls	3.55	3.85	4.15	V
	Voltage detection level Vdet1_C (1)	When Vcc falls	3.70	4.00	4.30	V
	Voltage detection level Vdet1_D (1)	When Vcc falls	3.85	4.15	4.45	V
	Voltage detection level Vdet1_E (1)	When Vcc falls	4.00	4.30	4.60	V
	Voltage detection level Vdet1_F (1)	When Vcc falls	4.15	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_6 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time (2)	At the falling of Vcc from 5 V to (Vdet1 – 0.1) V	—	60	150	µs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 4.9 Voltage Detection 2 Circuit Characteristics (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0	When Vcc falls	3.70	4.00	4.30	V
—	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		—	0.1	—	µs
—	Voltage detection 2 circuit response time (1)	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	—	20	150	µs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (2)		—	—	100	µs

Notes:
1. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 4.15 DC Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V] (Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter	Conditions								Standard (4)			Unit
			Oscillation		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ.	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—		—	6.5	15	mA
			16 MHz	Off	Off	125 kHz	No division	—		—	5.3	12.5	mA
			10 MHz	Off	Off	125 kHz	No division	—		—	3.6	—	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	—		—	3.0	—	mA
			16 MHz	Off	Off	125 kHz	Divide-by-8	—		—	2.2	—	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	—		—	1.5	—	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz (3)	125 kHz	No division	—		—	7.0	15	mA
			Off	Off	20 MHz (3)	125 kHz	Divide-by-8	—		—	3.0	—	mA
			Off	Off	4 MHz (3)	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRC = 1		—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 SVC0 = 0		—	90	400	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	—	FMR27 = 1 SVC0 = 0		—	85	400	µA
			Off	32 kHz	Off	Off	—	FMSTP = 1 SVC0 = 0	Program operation on RAM Flash memory off	—	47	—	µA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	100	µA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	4	90	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	—	2.2	6.0	µA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	—	30	—	µA

Notes:
1. Vcc = 3.3 V to 5.5 V, single-chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Table 4.16 DC Characteristics (3) [2.7 V ≤ Vcc < 4.2 V]
(Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	Other than XOUT	Drive capacity is high	I_{OH} = –5 mA	Vcc – 0.5	—	Vcc	V
			Drive capacity is low	I_{OH} = –1 mA	Vcc – 0.5	—	Vcc	V
		XOUT		I_{OH} = –200 µA	1.0	—	Vcc	V
V_{OL}	Output low voltage	Other than XOUT	Drive capacity is high	I_{OL} = 5 mA	—	—	0.5	V
			Drive capacity is low	I_{OL} = 1 mA	—	—	0.5	V
		XOUT		I_{OL} = 200 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRJIO_0, TRCCLK_0, TRCTRG_0, TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0, CLK_0, CLK_1, RXD_0, RXD_1, $\overline{CTS2}$, SCL2, SDA2, CLK2, RXD2, $\underline{SCL\_0}$, SDA_0, SSI_0, $\overline{SCS\_0}$, SSCK_0, SSO_0			0.1	0.4	—	V
		$\overline{RESET}$	Vcc = 3.0 V		0.1	0.5	—	V
I_{IH}	Input high current		V_I = 3.0 V		—	—	1.0	µA
I_{IL}	Input low current		V_I = 0 V		—	—	–1.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Table 4.17 DC Characteristics (4) [2.7 V ≤ Vcc < 3.3 V] (Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified))

Symbol	Parameter	Conditions								Standard (4)			Unit
			Oscillation		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ.	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	10 MHz	Off	Off	125 kHz	No division	—		—	3.5	10	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	—		—	1.5	7.5	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz (3)	125 kHz	No division	—		—	7.0	15	mA
			Off	Off	20 MHz (3)	125 kHz	Divide-by-8	—		—	3.0	—	mA
			Off	Off	10 MHz (3)	125 kHz	No division	—		—	4.0	—	mA
			Off	Off	10 MHz (3)	125 kHz	Divide-by-8	—		—	1.5	—	mA
			Off	Off	4 MHz (3)	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRC = 1		—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 SVC0 = 0		—	90	390	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 SVC0 = 0		—	80	400	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 SVC0 = 0	Program operation on RAM Flash memory off	—	40	—	µA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	90	µA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	4	80	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	—	2.2	6.0	µA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	—	30	—	µA

Notes:
1. Vcc = 2.7 V to 3.3 V, single-chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

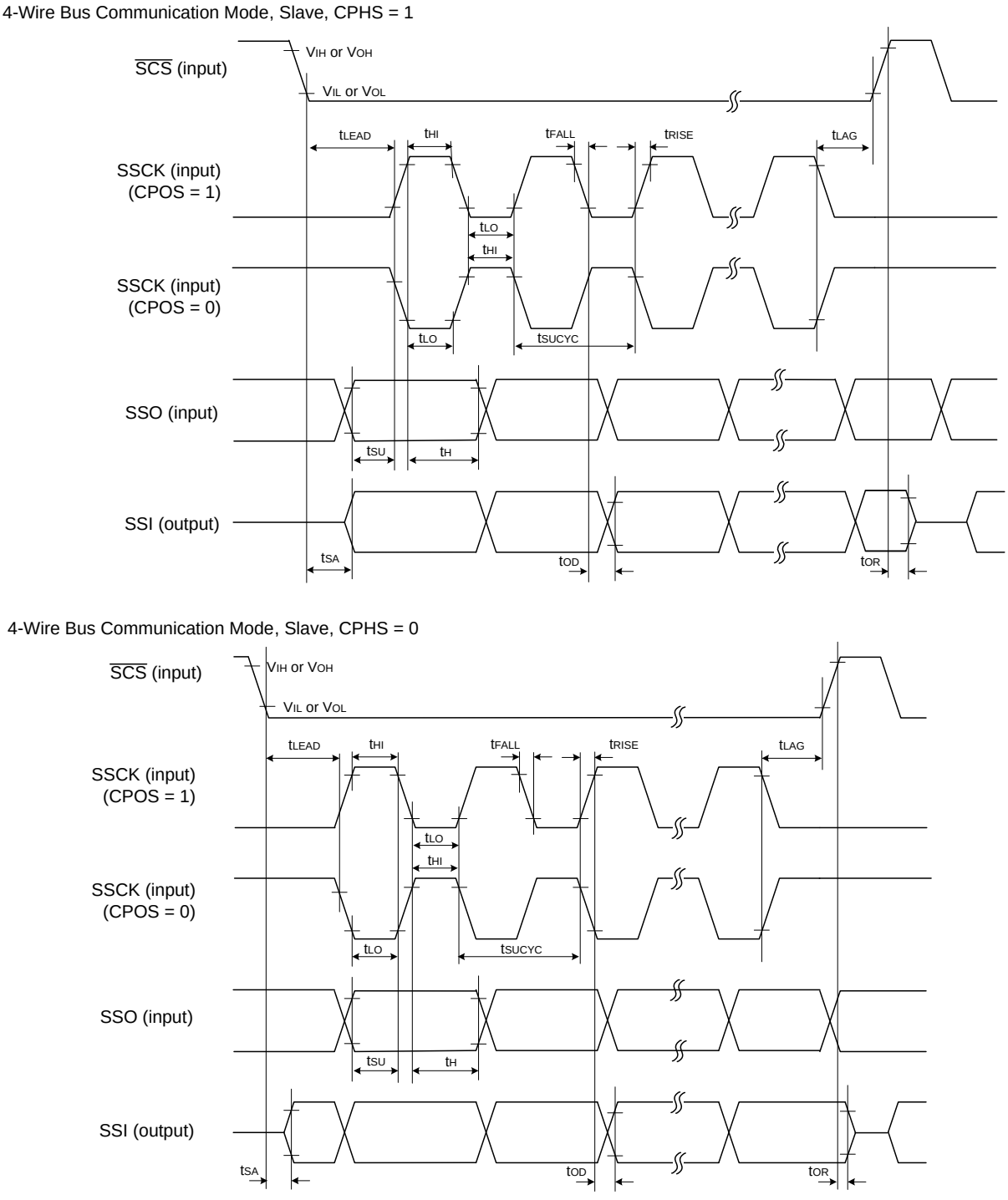
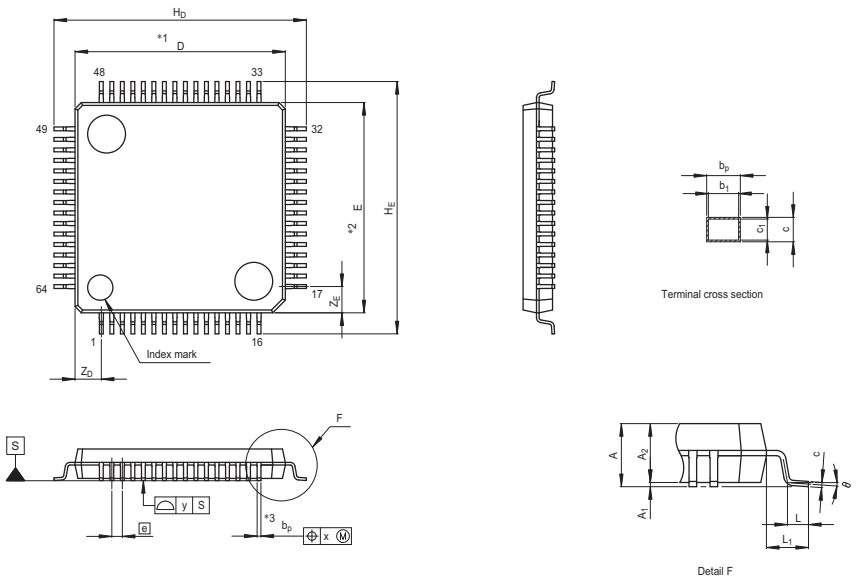


Figure 4.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

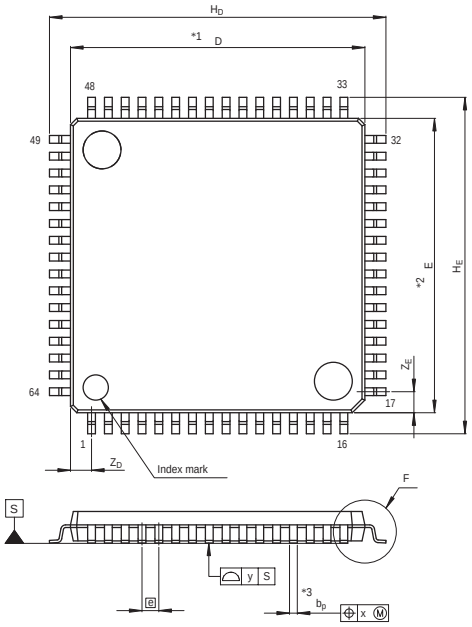
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g

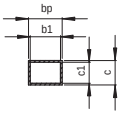


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

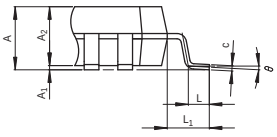
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—