Renesas Electronics America Inc - R5F2136CSNFA#X4 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2136csnfa-x4

Table 1.2 Specifications (2)

Item	Function	Description
Serial interface	UART0_0 and UART0_1	2 channels Clock synchronous serial I/O mode, clock asynchronous serial I/O mode
	UART2	1 channel Clock synchronous serial I/O mode, clock asynchronous serial I/O mode, I^2C mode (I^2C-bus), multiprocessor communication mode
Clock Synchronous serial interface	(SSU) SSU_0	1 channel (also used for the I^2C bus)
	(I^2C bus) I^2C_0	1 channel (also used for the SSU)
LIN module	HW-LIN_0	Hardware LIN 1 channel (timer RJ_0, UART0_0, or UART0_1 used)
A/D converter		Resolution: 10 bits × 12 channels, sample and hold function, sweep mode
Comparator B		2 circuits
Touch Sensor control unit (TSCU)		System CH × 4, electrostatic capacitive touch detection × 28
CRC calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash memory		• Program/erase voltage: VCC = 2.7 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • BGO (background operation) function (data flash)
Operating frequency/ Power supply voltage		CPU clock = 20 MHz (VCC = 2.7 V to 5.5 V) CPU clock = 5 MHz (VCC = 1.8 V to 5.5 V)
Current consumption		Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 4.0 μA (VCC = 3.0 V, wait mode f(XCIN) = 32 kHz) Typ. 2.2 μA (VCC = 3.0 V, stop mode)
Operating ambient temperature		-20°C to 85°C (N version) -40°C to 85°C (D version) (1)
Package		64-pin LQFP Package code: PLQP0064KB-A (previous code: 64P6Q-A) Package code: PLQP0064GA-A (previous code: 64P6U-A)

Note:
1. Specify the D version if it is to be used.

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Tables 1.4 to 1.6 list the Pin Name Information by Pin Number.

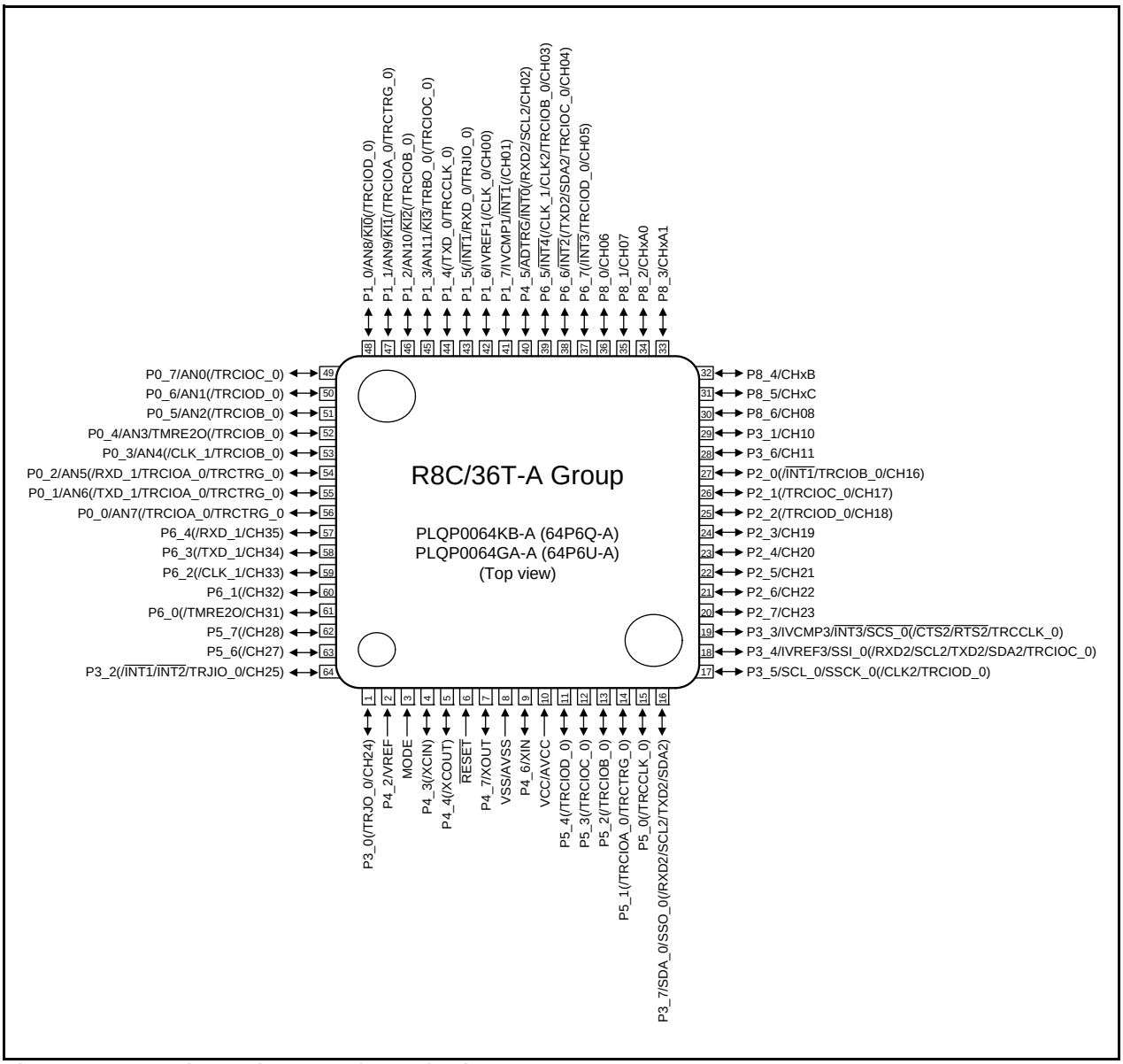


Figure 1.3 Pin Assignment (Top View)

Table 1.4 Pin Name Information by Pin Number (INT, URAT0, and UART2)

Port	Pin No.	INT					UART0						UART2						
		$\overline{INT0}$	$\overline{INT1}$	$\overline{INT2}$	$\overline{INT3}$	$\overline{INT4}$	TXD_0	TXD_1	RXD_0	RXD_1	CLK_0	CLK_1	TXD2	RXD2	$\overline{CTS2}$	$\overline{RTS2}$	SDA2	SCL2	CLK2
P0_0	56																		
P0_1	55							TXD_1											
P0_2	54									RXD_1									
P0_3	53											CLK_1							
P0_4	52																		
P0_5	51																		
P0_6	50																		
P0_7	49																		
P1_0	48																		
P1_1	47																		
P1_2	46																		
P1_3	45																		
P1_4	44						TXD_0												
P1_5	43		$\overline{INT1}$						RXD_0										
P1_6	42										CLK_0								
P1_7	41		$\overline{INT1}$																
P2_0	27		$\overline{INT1}$																
P2_1	26																		
P2_2	25																		
P2_3	24																		
P2_4	23																		
P2_5	22																		
P2_6	21																		
P2_7	20																		
P3_0	1																		
P3_1	29																		
P3_2	64		$\overline{INT1}$	$\overline{INT2}$															
P3_3	19				$\overline{INT3}$										$\overline{CTS2}$	$\overline{RTS2}$			
P3_4	18												TXD2	RXD2			SDA2	SCL2	
P3_5	17																		CLK2
P3_6	28																		
P3_7	16												TXD2	RXD2			SDA2	SCL2	
P4_2	2																		
P4_3	4																		
P4_4	5																		
P4_5	40	$\overline{INT0}$												RXD2				SCL2	
P4_6	9																		
P4_7	7																		
P5_0	15																		
P5_1	14																		
P5_2	13																		
P5_3	12																		
P5_4	11																		
P5_6	63																		
P5_7	62																		
P6_0	61																		
P6_1	60																		
P6_2	59											CLK_1							
P6_3	58							TXD_1											
P6_4	57									RXD_1									
P6_5	39					$\overline{INT4}$						CLK_1							CLK2
P6_6	38			$\overline{INT2}$									TXD2				SDA2		
P6_7	37				$\overline{INT3}$														
P8_0	36																		
P8_1	35																		
P8_2	34																		
P8_3	33																		
P8_4	32																		
P8_5	31																		
P8_6	30																		

Table 1.5 Pin Name Information by Pin Number (SSU/I²C, Timer RJ, and Timer RB2)

Port	Pin No.	SSU/I²C						Timer RJ		Timer RB2
		SCL_0	SDA_0	SSI_0	$\overline{SCS\_0}$	SSCK_0	SSO_0	TRJO_0	TRJIO_0	TRBO_0
P0_0	56									
P0_1	55									
P0_2	54									
P0_3	53									
P0_4	52									
P0_5	51									
P0_6	50									
P0_7	49									
P1_0	48									
P1_1	47									
P1_2	46									
P1_3	45									TRBO_0
P1_4	44									
P1_5	43								TRJIO_0	
P1_6	42									
P1_7	41									
P2_0	27									
P2_1	26									
P2_2	25									
P2_3	24									
P2_4	23									
P2_5	22									
P2_6	21									
P2_7	20									
P3_0	1							TRJO_0		
P3_1	29									
P3_2	64								TRJIO_0	
P3_3	19				$\overline{SCS\_0}$					
P3_4	18			SSI_0						
P3_5	17	SCL_0				SSCK_0				
P3_6	28									
P3_7	16		SDA_0				SSO_0			
P4_2	2									
P4_3	4									
P4_4	5									
P4_5	40									
P4_6	9									
P4_7	7									
P5_0	15									
P5_1	14									
P5_2	13									
P5_3	12									
P5_4	11									
P5_6	63									
P5_7	62									
P6_0	61									
P6_1	60									
P6_2	59									
P6_3	58									
P6_4	57									
P6_5	39									
P6_6	38									
P6_7	37									
P8_0	36									
P8_1	35									
P8_2	34									
P8_3	33									
P8_4	32									
P8_5	31									
P8_6	30									

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 through R3. R0 can be split into high-order (R0H) and low-order (R0L) registers to be used separately as 8-bit data registers. The same applies to R1H and R1L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). Similarly, R3 and R1 can be used as a 32-bit data register.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 functions in the same manner as A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

PC is a 20-bit register that indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of the FLG register is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated in the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. It must only be set to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0. Otherwise it is set to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value. Otherwise it is set to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow. Otherwise it is set to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts. Interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction for a software interrupt numbered from 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns eight processor interrupt priority levels from 0 to 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

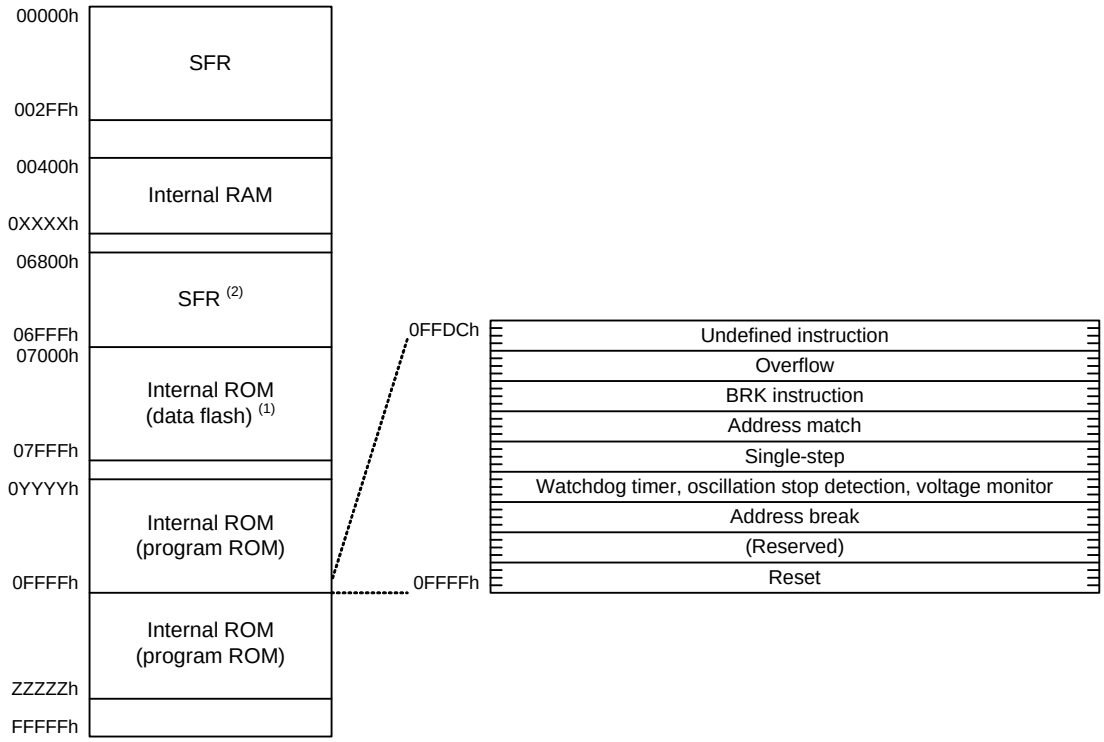
2.8.10 Reserved Bit

The write value must be 0. The read value is undefined.

3. Address Space

3.1 Memory Map

Figure 3.1 shows the Memory Map. The R8C/36T-A Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. Up to 32 Kbytes of the internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. The area in excess of 32 Kbytes is allocated at higher addresses, beginning with address 10000h. For example, a 64-Kbyte internal ROM is allocated at addresses 08000h to 17FFFh.
The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated at addresses 07000h to 07FFFh.
The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM is allocated at addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated at addresses 00000h to 02FFFh and addresses 06800h to 06FFFh. Peripheral function control registers are allocated here. All unallocated locations within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. Addresses 06800h to 06FFFh are used for the ELC, DTC, and TSCU SFR areas.
3. The blank areas are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM	
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh
R5F21368SNFP/FA, R5F21368SDFP/FA	64 Kbytes	08000h	17FFFh	6 Kbytes	01BFFh
R5F21368SNFP/FA, R5F21368SDFP/FA	96 Kbytes	08000h	1FFFFh	8 Kbytes	023FFh
R5F21368SNFP/FA, R5F21368SDFP/FA	128 Kbytes	08000h	27FFFh	10 Kbytes	02BFFh

Figure 3.1 Memory Map

Table 3.5 SFR Information (5) (1)

Address	Symbol	Register Name	After Reset	Remarks
000FAh				
000FBh				
000FCh				
000FDh				
000FEh				
000FFh				
00100h				
00101h				
00102h				
00103h				
00104h				
00105h				
00106h				
00107h				
00108h				
00109h				
0010Ah				
0010Bh				
0010Ch				
0010Dh				
0010Eh				
0010Fh				
00110h	TRJ_0	Timer RJ_0 Counter Register	FFFFh	
00111h				
00112h	TRJCR_0	Timer RJ_0 Control Register	00h	
00113h	TRJIOC_0	Timer RJ_0 I/O Control Register	00h	
00114h	TRJMR_0	Timer RJ_0 Mode Register	00h	
00115h	TRJISR_0	Timer RJ_0 Event Pin Select Register	00h	
00116h				
00117h				
00118h				
00119h				
0011Ah				
0011Bh				
0011Ch				
0011Dh				
0011Eh				
0011Fh				
00120h				
00121h				
00122h				
00123h				
00124h				
00125h				
00126h				
00127h				
00128h				
00129h				
0012Ah				
0012Bh				
0012Ch				
0012Dh				
0012Eh				
0012Fh				
00130h	TRBCR_0	Timer RB2_0 Control Register	00h	
00131h	TRBOCR_0	Timer RB2_0 One-Shot Control Register	00h	
00132h	TRBIOC_0	Timer RB2_0 I/O Control Register	00h	
00133h	TRBMR_0	Timer RB2_0 Mode Register	00h	
00134h	TRBPRE_0	Timer RB2_0 Prescaler Register	FFh	
00135h	TRBPR_0	Timer RB2_0 Primary Register	FFh	
00136h	TRBSC_0	Timer RB2_0 Secondary Register	FFh	
00137h	TRBIR_0	Timer RB2_0 Interrupt Request Register	00h	
00138h	TRCCNT_0	Timer RC_0 Counter	0000h	
00139h				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.7 SFR Information (7) (1)

Address	Symbol	Register Name	After Reset	Remarks
0017Ah	TREIFR	Timer RE2 Interrupt Flag Register	00h	
0017Bh	TREIER	Timer RE2 Interrupt Enable Register	00h	
0017Ch	TREAMN	Timer RE2 Alarm Minute Register	00h	
0017Dh	TREAHR	Timer RE2 Alarm Hour Register	00h	
0017Eh	TREAWK	Timer RE2 Alarm Day-of-the-Week Register	00h	
0017Fh	TREPRC	Timer RE2 Protect Register	00h	
00180h to 001FFh				
00200h	AD0	A/D Register 0	00h	
00201h			00h	
00202h	AD1	A/D Register 1	00h	
00203h			00h	
00204h	AD2	A/D Register 2	00h	
00205h			00h	
00206h	AD3	A/D Register 3	00h	
00207h			00h	
00208h	AD4	A/D Register 4	00h	
00209h			00h	
0020Ah	AD5	A/D Register 5	00h	
0020Bh			00h	
0020Ch	AD6	A/D Register 6	00h	
0020Dh			00h	
0020Eh	AD7	A/D Register 7	00h	
0020Fh			00h	
00210h				
00211h				
00212h				
00213h				
00214h	ADMOD	A/D Mode Register	00h	
00215h	ADINSEL	A/D Input Select Register	11000000b	
00216h	ADCON0	A/D Control Register 0	00h	
00217h	ADCON1	A/D Control Register 1	00h	
00218h				
00219h				
0021Ah				
0021Bh				
0021Ch				
0021Dh				
0021Eh				
0021Fh				
00220h				
00221h				
00222h				
00223h				
00224h				
00225h				
00226h				
00227h				
00228h	INTCMP	Comparator B Control Register 0	00h	
00229h				
0022Ah				
0022Bh				
0022Ch				
0022Dh				
0022Eh				
0022Fh				
00230h	INTEN	External Input Enable Register 0	00h	
00231h	INTEN1	External Input Enable Register 1	00h	
00232h	INTF	INT Input Filter Select Register 0	00h	
00233h	INTF1	INT Input Filter Select Register 1	00h	
00234h	INTPOL	INT Input Polarity Switch Register	00h	
00235h				
00236h	KIEN	Key Input Interrupt Enable Register	00h	
00237h				
00238h	MSTCR0	Module Standby Control Register 0	00h	
00239h	MSTCR1	Module Standby Control Register 1	00h	

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.9 SFR Information (9) (1)

Address	Symbol	Register Name	After Reset	Remarks
00280h	DTCTL	DTC Activation Control Register	00h	
00281h				
00282h				
00283h				
00284h				
00285h				
00286h				
00287h				
00288h	DTCEN0	DTC Activation Enable Register 0	00h	
00289h	DTCEN1	DTC Activation Enable Register 1	00h	
0028Ah	DTCEN2	DTC Activation Enable Register 2	00h	
0028Bh	DTCEN3	DTC Activation Enable Register 3	00h	
0028Ch				
0028Dh	DTCEN5	DTC Activation Enable Register 5	00h	
0028Eh	DTCEN6	DTC Activation Enable Register 6	00h	
0028Fh				
00290h	CRCSAR	SFR Snoop Address Register	0000h	
00291h				
00292h	CRCMR	CRC Control Register	00h	
00293h				
00294h	CRCD	CRC Data Register	0000h	
00295h				
00296h	CRCIN	CRC Input Register	00h	
00297h				
00298h				
00299h				
0029Ah				
0029Bh				
0029Ch				
0029Dh				
0029Eh				
0029Fh				
002A0h	TRJ_0SR	Timer RJ_0 Pin Select Register	08h	
002A1h				
002A2h				
002A3h				
002A4h				
002A5h	TRCCLKSR	Timer RCCLK Pin Select Register	00h	
002A6h	TRC_0SR0	Timer RC_0 Pin Select Register 0	00h	
002A7h	TRC_0SR1	Timer RC_0 Pin Select Register 1	00h	
002A8h				
002A9h				
002AAh				
002ABh				
002ACh				
002ADh	TIMSR	Timer Pin Select Register	00h	
002AEh	U_0SR	UART0_0 Pin Select Register	00h	
002AFh	U_1SR	UART0_1 Pin Select Register	00h	
002B0h				
002B1h				
002B2h	U2SR0	UART2 Pin Select Register 0	00h	
002B3h	U2SR1	UART2 Pin Select Register 1	00h	
002B4h				
002B5h				
002B6h	INTSR0	INT Interrupt Input Pin Select Register 0	00h	
002B7h				
002B8h				
002B9h	PINSR	I/O Function Pin Select Register	00h	
002BAh				
002BBh				
002BCh				
002BDh				
002BEh	PMCSEL	Pin Assignment Select Register	00h	
002BFh				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.13 SFR Information (13) (1)

Address	Symbol	Register Name	After Reset	Remarks
06C0Ah		Area for storing DTC transfer vector 10	XXh	
06C0Bh		Area for storing DTC transfer vector 11	XXh	
06C0Ch		Area for storing DTC transfer vector 12	XXh	
06C0Dh		Area for storing DTC transfer vector 13	XXh	
06C0Eh		Area for storing DTC transfer vector 14	XXh	
06C0Fh		Area for storing DTC transfer vector 15	XXh	
06C10h		Area for storing DTC transfer vector 16	XXh	
06C11h		Area for storing DTC transfer vector 17	XXh	
06C12h		Area for storing DTC transfer vector 18	XXh	
06C13h		Area for storing DTC transfer vector 19	XXh	
06C14h				
06C15h				
06C16h		Area for storing DTC transfer vector 22	XXh	
06C17h		Area for storing DTC transfer vector 23	XXh	
06C18h		Area for storing DTC transfer vector 24	XXh	
06C19h		Area for storing DTC transfer vector 25	XXh	
06C1Ah				
06C1Bh				
06C1Ch				
06C1Dh				
06C1Eh				
06C1Fh				
06C20h				
06C21h				
06C22h				
06C23h				
06C24h				
06C25h				
06C26h				
06C27h				
06C28h				
06C29h				
06C2Ah		Area for storing DTC transfer vector 42	XXh	
06C2Bh				
06C2Ch				
06C2Dh				
06C2Eh				
06C2Fh				
06C30h				
06C31h		Area for storing DTC transfer vector 49	XXh	
06C32h				
06C33h		Area for storing DTC transfer vector 51	XXh	
06C34h		Area for storing DTC transfer vector 52	XXh	
06C35h		Area for storing DTC transfer vector 53	XXh	
06C36h		Area for storing DTC transfer vector 54	XXh	
06C37h				
06C38h				
06C39h				
06C3Ah				
06C3Bh				
06C3Ch				
06C3Dh				
06C3Eh				
06C3Fh				
06C40h	DTCCR0	DTC Control Register 0	XXh	
06C41h	DTBLS0	DTC Block Size Register 0	XXh	
06C42h	DTCCT0	DTC Transfer Count Register 0	XXh	
06C43h	DTRLD0	DTC Transfer Count Reload Register 0	XXh	
06C44h	DTSAR0	DTC Source Address Register 0	XXXXh	
06C45h				
06C46h	DTDAR0	DTC Destination Address Register 0	XXXXh	
06C47h				
06C48h	DTCCR1	DTC Control Register 1	XXh	
06C49h	DTBLS1	DTC Block Size Register 1	XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.8 Voltage Detection 1 Circuit Characteristics (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (1)	When Vcc falls	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (1)	When Vcc falls	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (1)	When Vcc falls	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (1)	When Vcc falls	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (1)	When Vcc falls	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (1)	When Vcc falls	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (1)	When Vcc falls	2.80	3.10	3.40	V
	Voltage detection level Vdet1_7 (1)	When Vcc falls	2.95	3.25	3.55	V
	Voltage detection level Vdet1_8 (1)	When Vcc falls	3.10	3.40	3.70	V
	Voltage detection level Vdet1_9 (1)	When Vcc falls	3.25	3.55	3.85	V
	Voltage detection level Vdet1_A (1)	When Vcc falls	3.40	3.70	4.00	V
	Voltage detection level Vdet1_B (1)	When Vcc falls	3.55	3.85	4.15	V
	Voltage detection level Vdet1_C (1)	When Vcc falls	3.70	4.00	4.30	V
	Voltage detection level Vdet1_D (1)	When Vcc falls	3.85	4.15	4.45	V
	Voltage detection level Vdet1_E (1)	When Vcc falls	4.00	4.30	4.60	V
	Voltage detection level Vdet1_F (1)	When Vcc falls	4.15	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_6 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time (2)	At the falling of Vcc from 5 V to (Vdet1 – 0.1) V	—	60	150	µs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 4.9 Voltage Detection 2 Circuit Characteristics (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0	When Vcc falls	3.70	4.00	4.30	V
—	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		—	0.1	—	µs
—	Voltage detection 2 circuit response time (1)	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	—	20	150	µs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (2)		—	—	100	µs

Notes:
1. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 4.19 DC Characteristics (6) [1.8 V ≤ Vcc < 2.7 V] (Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter	Conditions								Standard (4)			Unit
			Oscillation		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ.	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	5 MHz	Off	Off	125 kHz	No division	—		—	2.2	—	mA
			5 MHz	Off	Off	125 kHz	Divide-by-8	—		—	0.8	—	mA
		High-speed on-chip oscillator mode	Off	Off	5 MHz (3)	125 kHz	No division	—		—	2.5	10	mA
			Off	Off	5 MHz (3)	125 kHz	Divide-by-8	—		—	1.7	—	mA
			Off	Off	4 MHz (3)	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRC = 1		—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 SVC0 = 0		—	90	300	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 SVC0 = 0		—	80	350	µA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	90	µA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	4	80	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	—	2.2	6	µA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	—	30	—	µA

Notes:
1. Vcc = 1.8 V to 2.7 V, single-chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

4.5 AC Characteristics

Table 4.20 Timing Requirements of Clock Synchronous Serial I/O with Chip Select (during Master Operation) (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time		4.00	—	—	t_{CYC} (1)
t_{HI}	SSCK clock high width		0.40	—	0.60	t_{SUCYC}
t_{LO}	SSCK clock low width		0.40	—	0.60	t_{SUCYC}
t_{RISE}	SSCK clock rising time	2.7 V ≤ Vcc ≤ 5.5 V	—	—	0.50	t_{CYC} (1)
		1.8 V ≤ Vcc < 2.7 V	—	—	1.00	t_{CYC} (1)
t_{FALL}	SSCK clock falling time	2.7 V ≤ Vcc ≤ 5.5 V	—	—	0.50	t_{CYC} (1)
		1.8 V ≤ Vcc < 2.7 V	—	—	1.00	t_{CYC} (1)
t_{SU}	SSI, SSO data input setup time	4.5 V ≤ Vcc ≤ 5.5 V	60	—	—	ns
		2.7 V ≤ Vcc < 4.5 V	70	—	—	ns
		1.8 V ≤ Vcc < 2.7 V	100	—	—	ns
t_H	SSI, SSO data input hold time	2.7 V ≤ Vcc ≤ 5.5 V	2.00	—	—	t_{CYC} (1)
		1.8 V ≤ Vcc < 2.7 V	2.00	—	—	t_{CYC} (1)
t_{LEAD}	$\overline{SCS}$-SCK output delay time		0.5 t_{SUCYC} - 1 t_{CYC}	—	—	ns
t_{LAG}	SCK -$\overline{SCS}$ output valid time		0.5 t_{SUCYC} - 1 t_{CYC}	—	—	ns
t_{OD}	SSO data output delay time	2.7 V ≤ Vcc ≤ 5.5 V	—	—	30.00	ns
		1.8 V ≤ Vcc < 2.7 V	—	—	1.00	t_{CYC} (1)

Note:
1. $1t_{CYC} = 1/f1$ (s)

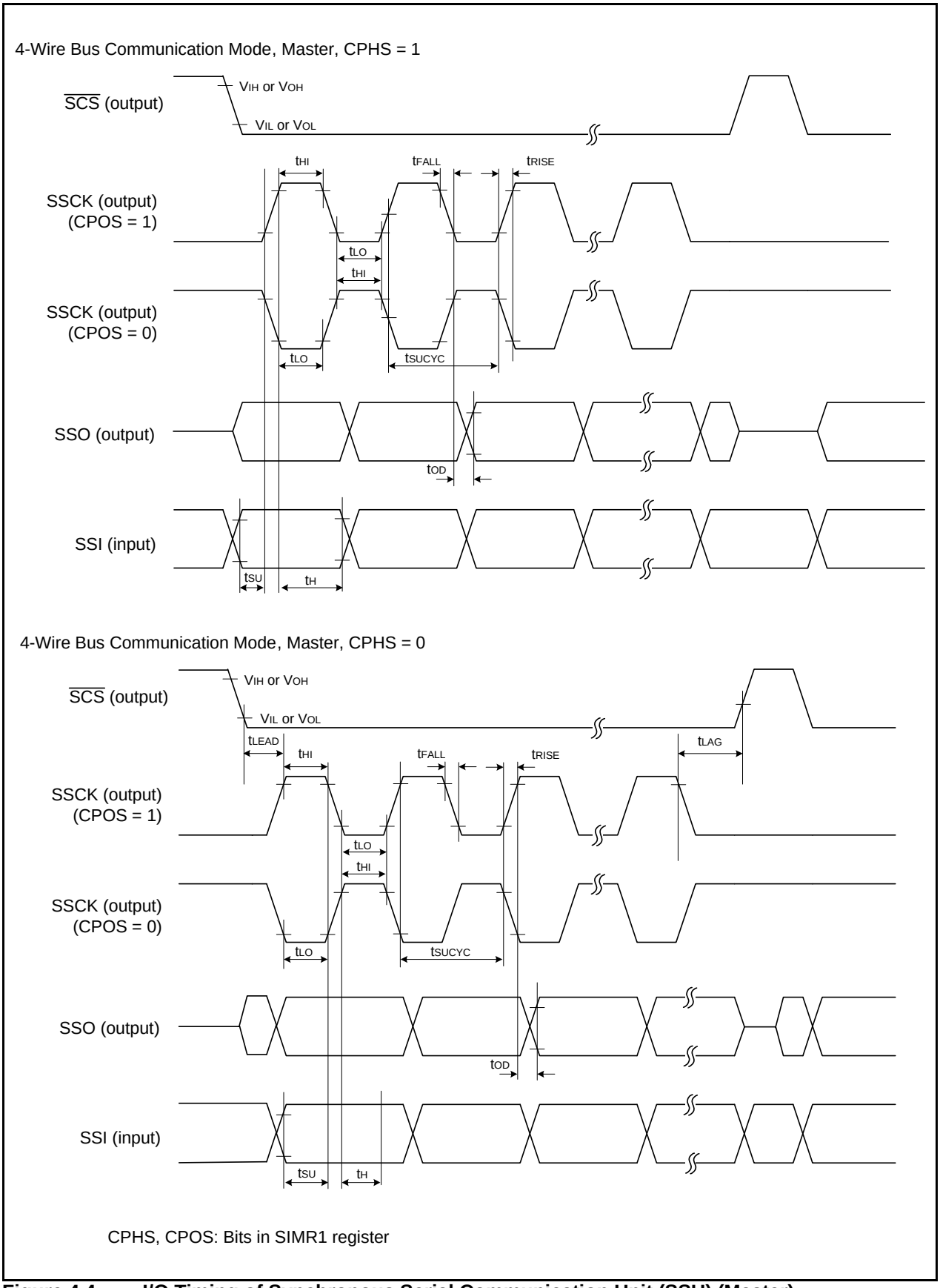


Figure 4.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

Table 4.22 External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	200	—	50	—	50	—	ns
$t_{WH(XOUT)}$	XOUT input high width	90	—	24	—	24	—	ns
$t_{WL(XOUT)}$	XOUT input low width	90	—	24	—	24	—	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	—	14	—	14	—	µs
$t_{WH(XCIN)}$	XCIN input high width	7	—	7	—	7	—	µs
$t_{WL(XCIN)}$	XCIN input low width	7	—	7	—	7	—	µs

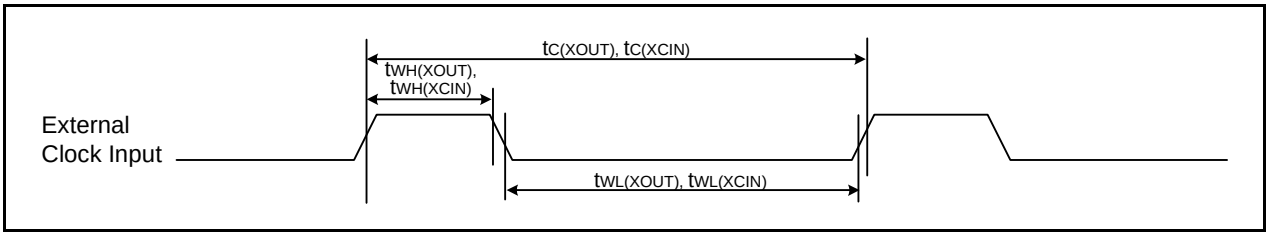


Figure 4.7 External Clock Input Timing Diagram

Table 4.23 Timing Requirements of TRJIO

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	500	—	300	—	100	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	200	—	120	—	40	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	200	—	120	—	40	—	ns

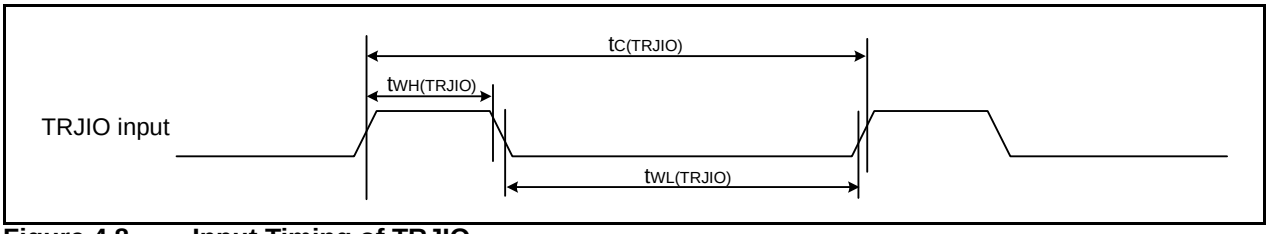


Figure 4.8 Input Timing of TRJIO

Table 4.24 Timing Requirements of Serial Interface (Internal clock selected as transfer clock (master communication))

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{d(C-Q)}$	TXDi output delay time	—	200	—	30	—	10	ns
$t_{su(D-C)}$	RXDi input setup time (1)	150	—	120	—	90	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	90	—	90	—	ns

i = 0 or 1

Note:

1. External pin load condition CL = 30 pF

Table 4.25 Timing Requirements of Serial Interface (External clock selected as transfer clock (slave communication))

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	300	—	200	—	ns
$t_{w(CKH)}$	CLKi input high width	400	—	150	—	100	—	ns
$t_{w(CKL)}$	CLKi input low width	400	—	150	—	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	—	120	—	90	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	30	—	10	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	90	—	90	—	ns

i = 0 or 1

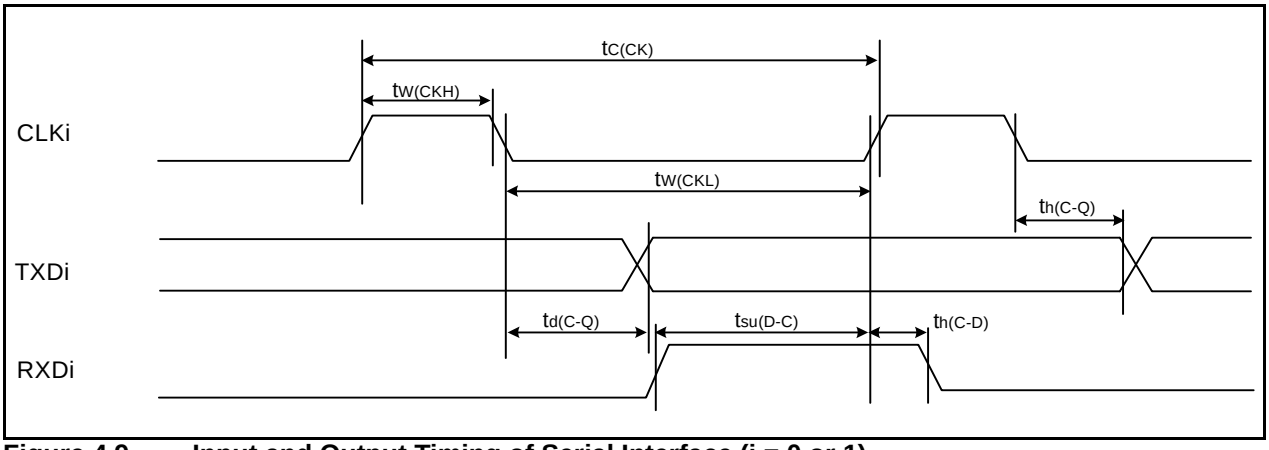


Figure 4.9 Input and Output Timing of Serial Interface (i = 0 or 1)

Table 4.26 Timing Requirements of External Interrupt $\overline{INTi}$ (i = 0 to 4) and Key Input Interrupt $\overline{KIj}$ (j = 0 to 3)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIj}$ input high width	1000 (1)	—	380 (1)	—	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIj}$ input low width	1000 (2)	—	380 (2)	—	250 (2)	—	ns

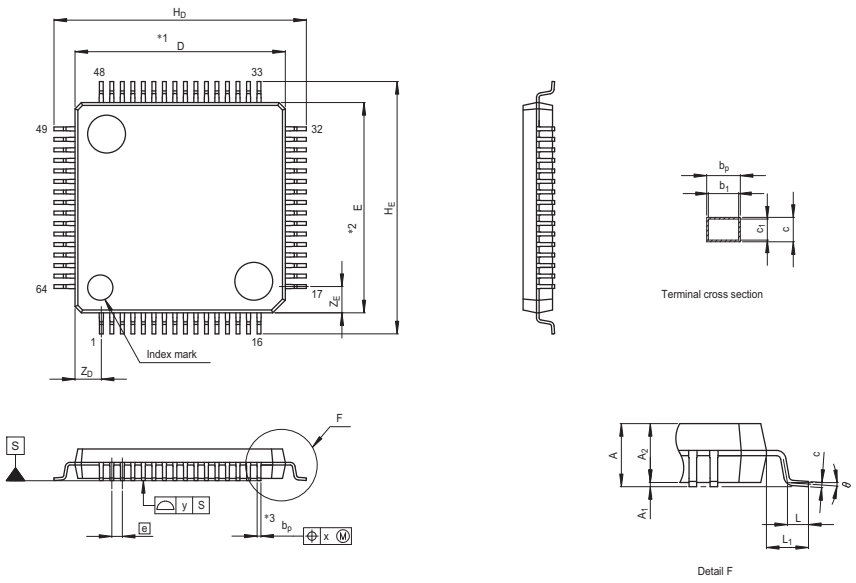
Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input high pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input low pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.

Figure 4.10 Input Timing of External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIj}$ (i = 0 to 4; j = 0 to 3)

Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.