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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2136csnfp-30

1.1.2 Specifications

Tables 1.1 and 1.2 outline Specifications.

Table 1.1 Specifications (1)

Item	Function	Description
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (CPU clock = 20 MHz, VCC = 2.7 V to 5.5 V) 200 ns (CPU clock = 5 MHz, VCC = 1.8 V to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, data flash	Refer to **Table 1.3 Product List**.
Voltage detection	Voltage detection circuit	• Power-on reset • Voltage detection with three check points (the detection levels for voltage detection 0 and voltage detection 1 can be selected.)
I/O ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 59, selectable pull-up resistor • High current drive ports: 59
Clock	Clock generation circuits	• 4 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Divided by 1, 2, 4, 8, or 16 can be selected • Low-power mode: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Number of interrupt vectors: 69 • External interrupt inputs: 9 (INT × 5, key input × 4) • Priority levels: 7
Event link controller (ELC)		• Events output from peripheral functions can be linked to events input to different peripheral functions. (30 sources × 10 types of event link operations) • Events can be handled independently from interrupt requests.
Watchdog timer		• 14 bits × 1 • Selectable reset start function • Selectable low-speed on-chip oscillator for the watchdog timer
DTC (data transfer controller)		• 1 channel • Activation sources: 27 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timers RJ_0	16 bits × 1: 1 circuit integrated on-chip Timer mode (periodic timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB2_0	16 bits × 1: 1 circuit integrated on-chip Timer mode (periodic timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timers RC_0	16 bits (with 4 capture/compare registers) × 1: 1 circuit integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)
	Timer RE2	8 bits × 1 Compare match timer mode, real-time clock mode

Table 1.2 Specifications (2)

Item	Function	Description
Serial interface	UART0_0 and UART0_1	2 channels Clock synchronous serial I/O mode, clock asynchronous serial I/O mode
	UART2	1 channel Clock synchronous serial I/O mode, clock asynchronous serial I/O mode, I^2C mode (I^2C-bus), multiprocessor communication mode
Clock Synchronous serial interface	(SSU) SSU_0	1 channel (also used for the I^2C bus)
	(I^2C bus) I^2C_0	1 channel (also used for the SSU)
LIN module	HW-LIN_0	Hardware LIN 1 channel (timer RJ_0, UART0_0, or UART0_1 used)
A/D converter		Resolution: 10 bits × 12 channels, sample and hold function, sweep mode
Comparator B		2 circuits
Touch Sensor control unit (TSCU)		System CH × 4, electrostatic capacitive touch detection × 28
CRC calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash memory		• Program/erase voltage: VCC = 2.7 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • BGO (background operation) function (data flash)
Operating frequency/ Power supply voltage		CPU clock = 20 MHz (VCC = 2.7 V to 5.5 V) CPU clock = 5 MHz (VCC = 1.8 V to 5.5 V)
Current consumption		Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 4.0 μA (VCC = 3.0 V, wait mode f(XCIN) = 32 kHz) Typ. 2.2 μA (VCC = 3.0 V, stop mode)
Operating ambient temperature		-20°C to 85°C (N version) -40°C to 85°C (D version) (1)
Package		64-pin LQFP Package code: PLQP0064KB-A (previous code: 64P6Q-A) Package code: PLQP0064GA-A (previous code: 64P6U-A)

Note:
1. Specify the D version if it is to be used.

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Tables 1.4 to 1.6 list the Pin Name Information by Pin Number.

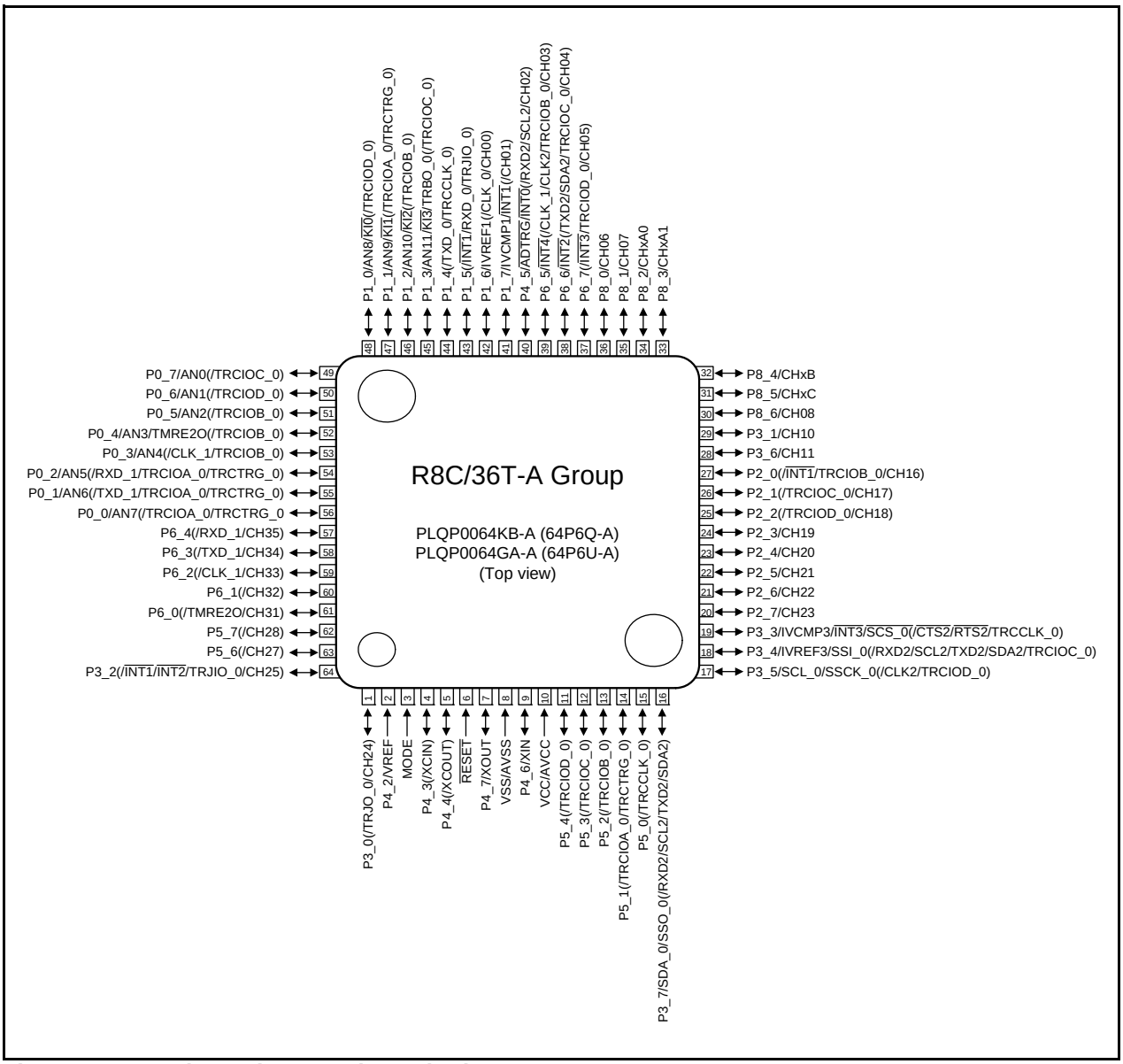


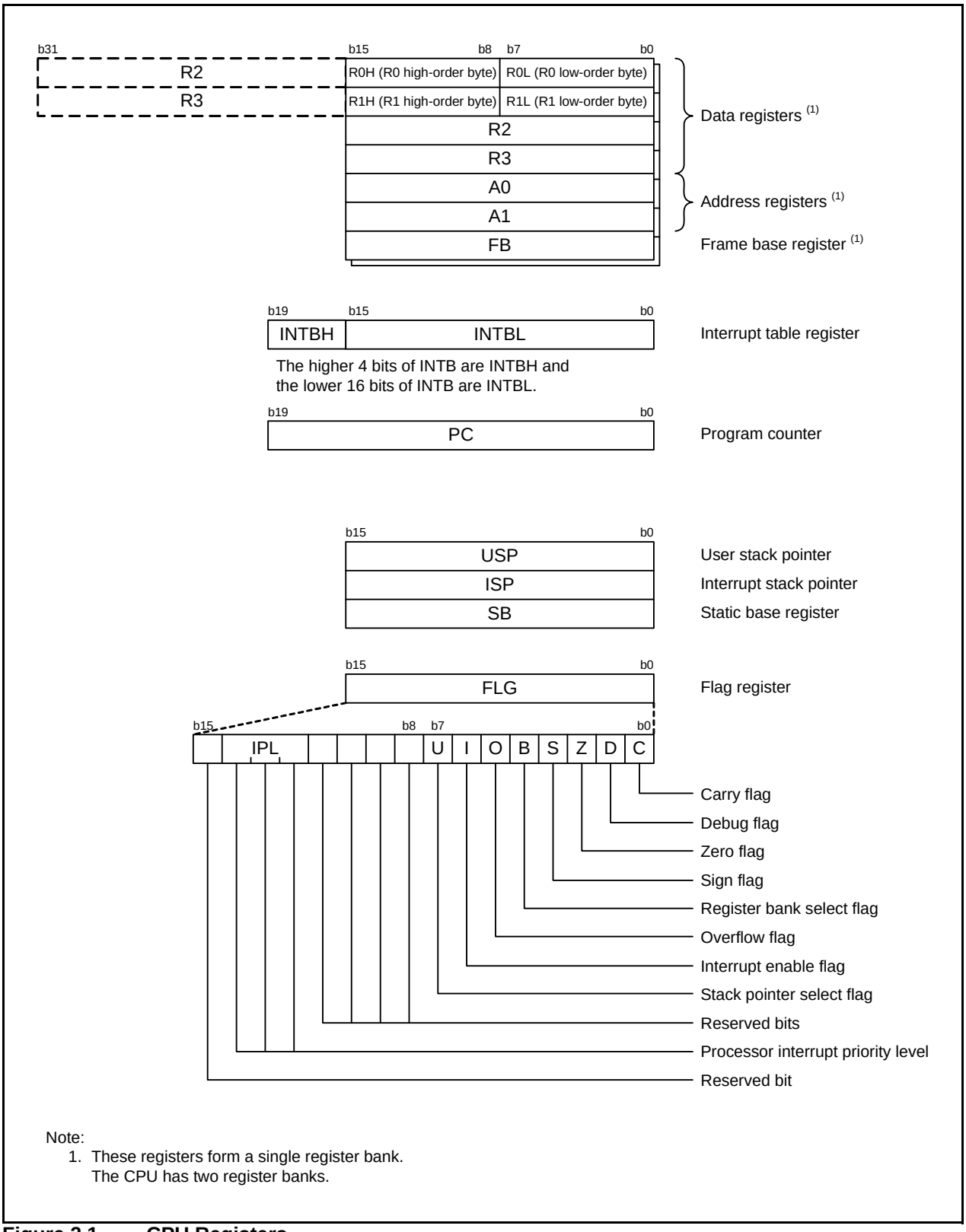
Figure 1.3 Pin Assignment (Top View)

Table 1.8 Pin Functions (2)

Item	Pin Name	I/O	Description
A/D converter	AN0 to AN11	I	Analog input for the A/D converter.
	$\overline{\text{ADTRG}}$	I	External trigger input for the A/D converter.
Comparator B	IVCMP1, IVCMP3	I	Analog voltage input for comparator B.
	IVREF1, IVREF3	I	Reference voltage input for comparator B.
Touch sensor control unit	CHxA0, CHxA1, CHxB, CHxC	I/O	Control pins for electrostatic capacitive touch detection.
	CH00 to CH08, CH10, CH11, CH16 to CH25, CH27, CH28, CH31 to CH35	I	Electrostatic capacitive touch detection pins.
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6_0 to P6_7, P8_0 to P8_6	I/O	8-bit CMOS input/output ports. Each port has an I/O select direction register, enabling switching input and output for each pin. For input ports, the presence or absence of a pull-up resistor can be selected by a program. All ports can be used as LED drive (high drive) ports.
Input port	P4_2	I	Input-only port.

2. Central Processing Unit (CPU)

Figure 2.1 shows the 13 CPU Registers. The registers R0, R1, R2, R3, A0, A1, and FB form a single register bank. The CPU has two register banks.



Note:
1. These registers form a single register bank.
The CPU has two register banks.

Figure 2.1 CPU Registers

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts. Interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction for a software interrupt numbered from 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns eight processor interrupt priority levels from 0 to 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

The write value must be 0. The read value is undefined.

Table 3.6 SFR Information (6) (1)

Address	Symbol	Register Name	After Reset	Remarks
0013Ah	TRCGRA_0	Timer RC_0 General Register A	FFFFh	
0013Bh				
0013Ch	TRCGRB_0	Timer RC_0 General Register B	FFFFh	
0013Dh				
0013Eh	TRCGRC_0	Timer RC_0 General Register C	FFFFh	
0013Fh				
00140h	TRCGRD_0	Timer RC_0 General Register D	FFFFh	
00141h				
00142h	TRCMR_0	Timer RC_0 Mode Register	01001000b	
00143h	TRCCR1_0	Timer RC_0 Control Register 1	00h	
00144h	TRCIER_0	Timer RC_0 Interrupt Enable Register	01110000b	
00145h	TRCSR_0	Timer RC_0 Status Register	01110000b	
00146h	TRCIOR0_0	Timer RC_0 I/O Control Register 0	10001000b	
00147h	TRCIOR1_0	Timer RC_0 I/O Control Register 1	10001000b	
00148h	TRCCR2_0	Timer RC_0 Control Register 2	00011000b	
00149h	TRCDF_0	Timer RC_0 Digital Filter Function Select Register	00h	
0014Ah	TRCOER_0	Timer RC_0 Output Enable Register	01111111b	
0014Bh	TRCADCR_0	Timer RC_0 A/D Conversion Trigger Control Register	11110000b	
0014Ch	TRCOPR_0	Timer RC_0 Output Waveform Manipulation Register	00h	
0014Dh	TRCELCCR_0	Timer RC_0 ELC Cooperation Control Register	00h	
0014Eh				
0014Fh				
00150h				
00151h				
00152h				
00153h				
00154h				
00155h				
00156h				
00157h				
00158h				
00159h				
0015Ah				
0015Bh				
0015Ch				
0015Dh				
0015Eh				
0015Fh				
00160h				
00161h				
00162h				
00163h				
00164h				
00165h				
00166h				
00167h				
00168h				
00169h				
0016Ah				
0016Bh				
0016Ch				
0016Dh				
0016Eh				
0016Fh				
00170h	TRESEC	Timer RE2 Counter Data Register Timer RE2 Second Data Register	00h	
00171h	TREMIN	Timer RE2 Compare Data Register Timer RE2 Minute Data Register	00h	
00172h	TREHR	Timer RE2 Hour Data Register	00h	
00173h	TREWK	Timer RE2 Day-of-the-Week Data Register	00h	
00174h	TREDY	Timer RE2 Day Data Register	00000001b	
00175h	TREMON	Timer RE2 Month Data Register	00000001b	
00176h	TREYR	Timer RE2 Year Data Register	00h	
00177h	TRECR	Timer RE2 Control Register	00000100b	
00178h	TRECSR	Timer RE2 Count Source Select Register	00001000b	
00179h	TREADJ	Timer RE2 Clock Error Correction Register	00h	

Note:
1. The blank areas are reserved. No access is allowed.

4.2 Recommended Operating Conditions

Table 4.2 Recommended Operating Conditions (1)
(Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage					1.8	—	5.5	V
V_{SS}/AV_{SS}	Supply voltage					—	0	—	V
V_{IH}	Input high voltage	Other than CMOS input				0.8V_{CC}	—	V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.5V_{CC}	—	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.55V_{CC}	—	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.65V_{CC}	—	V_{CC}	V
				Input level selection: 0.5V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.65V_{CC}	—	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.7V_{CC}	—	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.8V_{CC}	—	V_{CC}	V
				Input level selection: 0.7V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.85V_{CC}	—	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.85V_{CC}	—	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.85V_{CC}	—	V_{CC}	V
		External clock input (XOUT)				1.2	—	V_{CC}	V
V_{IL}	Input low voltage	Other than CMOS input				0	—	0.2V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	—	0.2V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	—	0.2V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	—	0.2V_{CC}	V
				Input level selection: 0.5V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	—	0.4V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	—	0.3V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	—	0.2V_{CC}	V
				Input level selection: 0.7V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	—	0.55V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	—	0.45V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	—	0.35V_{CC}	V
		External clock input (XOUT)				0	—	0.4	V
$I_{OH(sum)}$	Peak sum output high current		Sum of all pins $I_{OH(peak)}$			—	—	–80	mA
$I_{OH(sum)}$	Average sum output high current		Sum of all pins $I_{OH(avg)}$			—	—	–40	mA
$I_{OH(peak)}$	Peak output high current		When drive capacity is low			—	—	–10	mA
			When drive capacity is high			—	—	–40	mA
$I_{OH(avg)}$	Average output high current		When drive capacity is low			—	—	–5	mA
			When drive capacity is high			—	—	–20	mA
$I_{OL(sum)}$	Peak sum output low current		Sum of all pins $I_{OL(peak)}$			—	—	80	mA
$I_{OL(sum)}$	Average sum output low current		Sum of all pins $I_{OL(avg)}$			—	—	40	mA
$I_{OL(peak)}$	Peak output low current		When drive capacity is low			—	—	10	mA
			When drive capacity is high			—	—	40	mA
$I_{OL(avg)}$	Average output low current		When drive capacity is low			—	—	5	mA
			When drive capacity is high			—	—	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
$f_{(XCIN)}$	XCIN clock input oscillation frequency				1.8 V ≤ V_{CC} ≤ 5.5 V	—	32.768	50	kHz
fHOCO	Count source for timer RC				2.7 V ≤ V_{CC} ≤ 5.5 V	32	—	40	MHz
fHOCO-F	fHOCO-F frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
—	System clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
$f_{(BCLK)}$	CPU clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz

Note:
1. The average output current indicates the average value of current measured during 100 ms.

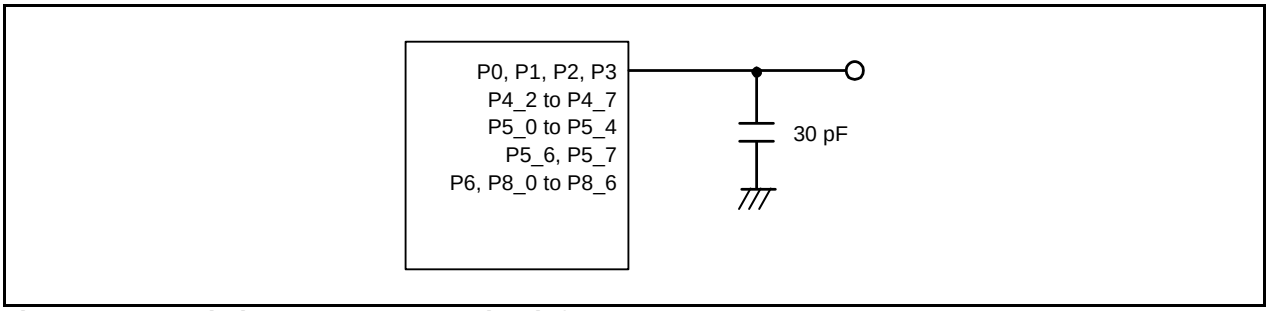


Figure 4.1 Timing Measurement Circuit for Ports P0, P1, P2, P3, P4_2 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6, and P8_0 to P8_6

4.3 Peripheral Function Characteristics

Table 4.3 A/D Converter Characteristics (Vcc/AVcc = Vref = 2.2 V to 5.5 V, Vss = 0 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		V_{ref} = AVcc		—	—	10	Bit
—	Absolute accuracy	10-bit mode	V_{ref} = AVcc = 5.0 V	AN0 to AN11 input	—	—	±3	LSB
			V_{ref} = AVcc = 3.3 V	AN0 to AN11 input	—	—	±5	LSB
			V_{ref} = AVcc = 3.0 V	AN0 to AN11 input	—	—	±5	LSB
			V_{ref} = AVcc = 2.2 V	AN0 to AN11 input	—	—	±5	LSB
		8-bit mode	V_{ref} = AVcc = 5.0 V	AN0 to AN11 input	—	—	±2	LSB
			V_{ref} = AVcc = 3.3 V	AN0 to AN11 input	—	—	±2	LSB
			V_{ref} = AVcc = 3.0 V	AN0 to AN11 input	—	—	±2	LSB
			V_{ref} = AVcc = 2.2 V	AN0 to AN11 input	—	—	±2	LSB
ϕAD	A/D conversion clock		4.0 V ≤ V_{ref} = AVcc ≤ 5.5 V (1)		2	—	20	MHz
			3.2 V ≤ V_{ref} = AVcc ≤ 5.5 V (1)		2	—	16	MHz
			2.7 V ≤ V_{ref} = AVcc ≤ 5.5 V (1)		2	—	10	MHz
			2.2 V ≤ V_{ref} = AVcc ≤ 5.5 V (1)		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
I_{vref}	Vref current		Vcc = 5 V, XIN = f1 = fAD = 20 MHz		—	45	—	µA
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	—	—	µs
		8-bit mode	V_{ref} = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	—	—	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	—	—	µs
V_{ref}	Reference voltage				2.2	—	AVcc	V
V_{IA}	Analog input voltage (2)				0	—	V_{ref}	V
OCVREF	On-chip reference voltage		2MHz ≤ ϕAD ≤ 4MHz		1.19	1.34	1.49	V

Notes:
1. If the CPU and the flash memory stop, the A/D conversion result will be undefined.
2. When the analog input voltage exceeds the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 4.4 Comparator B Characteristics (Vcc/AVcc = 2.2 V to 5.5 V, Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	Vcc – 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		–0.3	—	Vcc + 0.3	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time (1)	V_I = V_{ref} ±100 mV	—	0.1	—	µs
I_{CMP}	Comparator operating current	Vcc = 5.0 V	—	17.5	—	µA

Note:
1. When the digital filter is not selected.

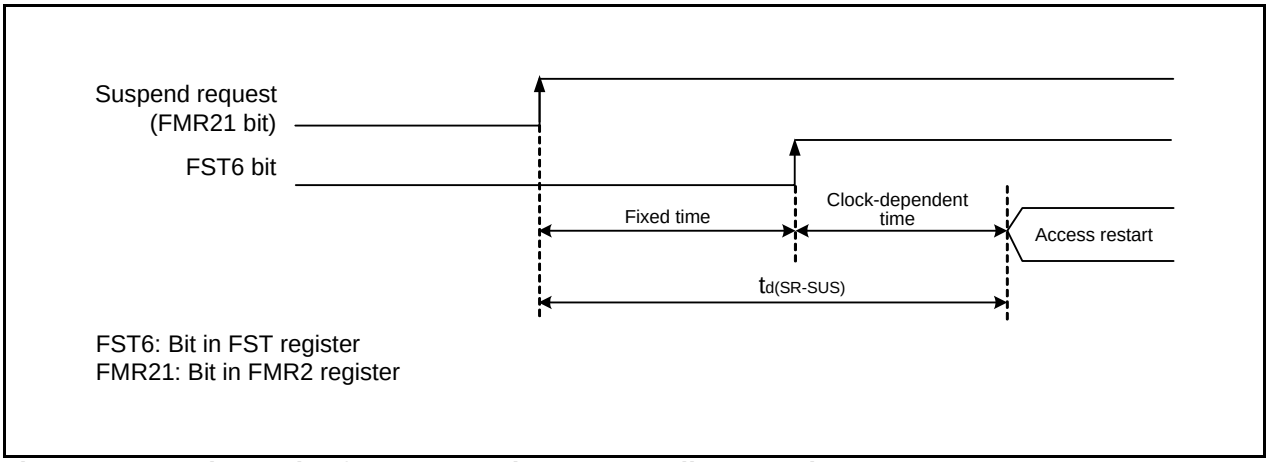


Figure 4.2 Time Delay from Suspend Request until Suspend

Table 4.7 Voltage Detection 0 Circuit Characteristics (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

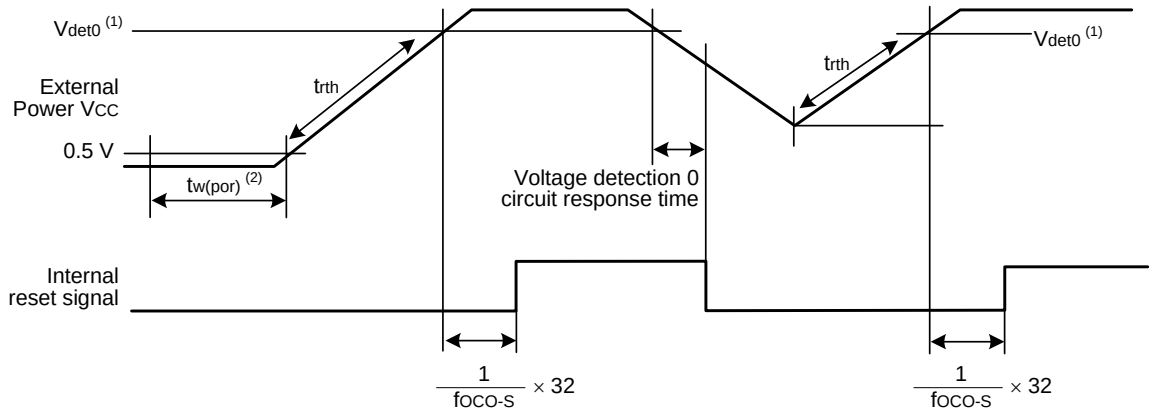
Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (1)	When Vcc falls	1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (1)	When Vcc falls	2.15	2.35	2.55	V
	Voltage detection level Vdet0_2 (1)	When Vcc falls	2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (1)	When Vcc falls	3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (2)	At the falling of Vcc from 5 V to (Vdet0 – 0.1) V	—	6	150	µs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. The voltage detection level must be selected with bits VDSEL0 and VDSEL1 in the OFS register.
2. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 4.10 Power-On Reset Circuit Characteristics (1)
(Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power VCC rise gradient		0	—	50,000	mV/msec

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to the **Voltage Detection Circuit** chapter of User's Manual: Hardware for details.
2. $t_{w(por)}$ indicates the duration the external power Vcc must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 4.3 Power-on Reset Circuit Characteristics

Table 4.11 High-Speed On-Chip Oscillator Circuit Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	Vcc = 1.8 V to 5.5 V, –20°C ≤ Topr ≤ 85°C (N version) –40°C ≤ Topr ≤ 85°C (D version)	—	40	—	MHz
	High-speed on-chip oscillator frequency when 01b or 10b is written to bits FRA25 and FRA24 in the FRA2 register (1)		—	36.864	—	MHz
	High-speed on-chip oscillator frequency when 10b is written to bits FRA25 and FRA24 in the FRA2 register		—	32	—	MHz
	High-speed on-chip oscillator frequency dependence on temperature and power supply voltage (2)		– 1.5	—	1.5	%
—	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	—	250	—	µs
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	—	500	—	µA

Notes:
1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.
2. This indicates the precision error for the oscillation frequency of the high-speed on-chip oscillator.

Table 4.15 DC Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V] (Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter	Conditions								Standard (4)			Unit
			Oscillation		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ.	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—		—	6.5	15	mA
			16 MHz	Off	Off	125 kHz	No division	—		—	5.3	12.5	mA
			10 MHz	Off	Off	125 kHz	No division	—		—	3.6	—	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	—		—	3.0	—	mA
			16 MHz	Off	Off	125 kHz	Divide-by-8	—		—	2.2	—	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	—		—	1.5	—	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz (3)	125 kHz	No division	—		—	7.0	15	mA
			Off	Off	20 MHz (3)	125 kHz	Divide-by-8	—		—	3.0	—	mA
			Off	Off	4 MHz (3)	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRC = 1		—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 SVC0 = 0		—	90	400	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	—	FMR27 = 1 SVC0 = 0		—	85	400	µA
			Off	32 kHz	Off	Off	—	FMSTP = 1 SVC0 = 0	Program operation on RAM Flash memory off	—	47	—	µA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	100	µA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	4	90	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	—	2.2	6.0	µA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	—	30	—	µA

Notes:
1. Vcc = 3.3 V to 5.5 V, single-chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Table 4.16 DC Characteristics (3) [2.7 V ≤ Vcc < 4.2 V]
(Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	Other than XOUT	Drive capacity is high	I_{OH} = –5 mA	Vcc – 0.5	—	Vcc	V
			Drive capacity is low	I_{OH} = –1 mA	Vcc – 0.5	—	Vcc	V
		XOUT		I_{OH} = –200 µA	1.0	—	Vcc	V
V_{OL}	Output low voltage	Other than XOUT	Drive capacity is high	I_{OL} = 5 mA	—	—	0.5	V
			Drive capacity is low	I_{OL} = 1 mA	—	—	0.5	V
		XOUT		I_{OL} = 200 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRJIO_0, TRCCLK_0, TRCTRG_0, TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0, CLK_0, CLK_1, RXD_0, RXD_1, $\overline{CTS2}$, SCL2, SDA2, CLK2, RXD2, $\underline{SCL\_0}$, SDA_0, SSI_0, $\overline{SCS\_0}$, SSCK_0, SSO_0			0.1	0.4	—	V
		$\overline{RESET}$	Vcc = 3.0 V		0.1	0.5	—	V
I_{IH}	Input high current		V_I = 3.0 V		—	—	1.0	µA
I_{IL}	Input low current		V_I = 0 V		—	—	–1.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Table 4.18 DC Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]
(Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	Other than XOUT	Drive capacity is high	I_{OH} = –2 mA	Vcc – 0.5	—	Vcc	V
			Drive capacity is low	I_{OH} = –1 mA	Vcc – 0.5	—	Vcc	V
		XOUT		I_{OH} = –200 µA	1.0	—	Vcc	V
V_{OL}	Output low voltage	Other than XOUT	Drive capacity is high	I_{OL} = 2 mA	—	—	0.5	V
			Drive capacity is low	I_{OL} = 1 mA	—	—	0.5	V
		XOUT		I_{OL} = 200 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRJIO_0, TRCCLK_0, TRCTRG_0, TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0, CLK_0, CLK_1, $\overline{RXD\_0}$, RXD_1,$\overline{CTS2}$, SCL2, SDA2, CLK2, RXD2, $\overline{SCL\_0}$, SDA_0,SSI_0, $\overline{SCS\_0}$, SSCK_0,SSO_0			0.05	0.2	—	V
		$\overline{RESET}$	V_{CC} = 2.2 V		0.05	0.2	—	V
I_{IH}	Input high current		V_I = 2.2 V		—	—	1.0	µA
I_{IL}	Input low current		V_I = 0 V		—	—	–1.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V		100	200	400	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

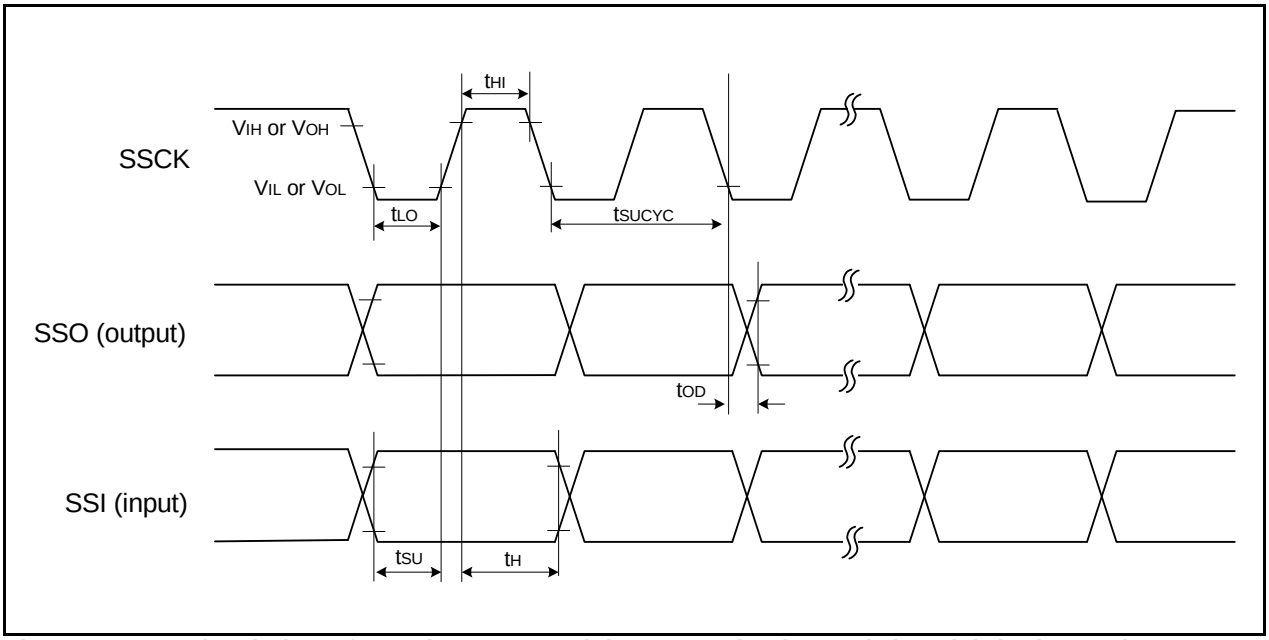


Figure 4.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 4.26 Timing Requirements of External Interrupt $\overline{INTi}$ (i = 0 to 4) and Key Input Interrupt $\overline{KIj}$ (j = 0 to 3)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIj}$ input high width	1000 (1)	—	380 (1)	—	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIj}$ input low width	1000 (2)	—	380 (2)	—	250 (2)	—	ns

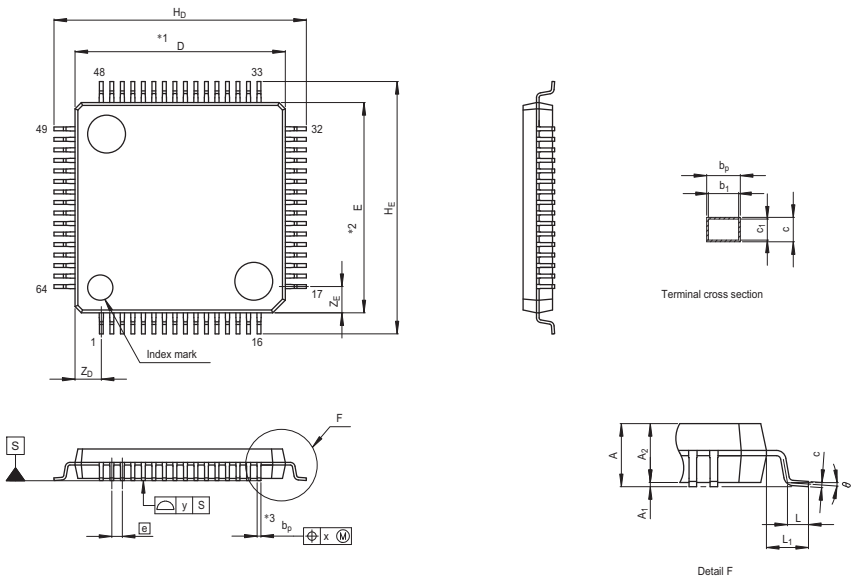
Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input high pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input low pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.

Figure 4.10 Input Timing of External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIj}$ (i = 0 to 4; j = 0 to 3)

Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

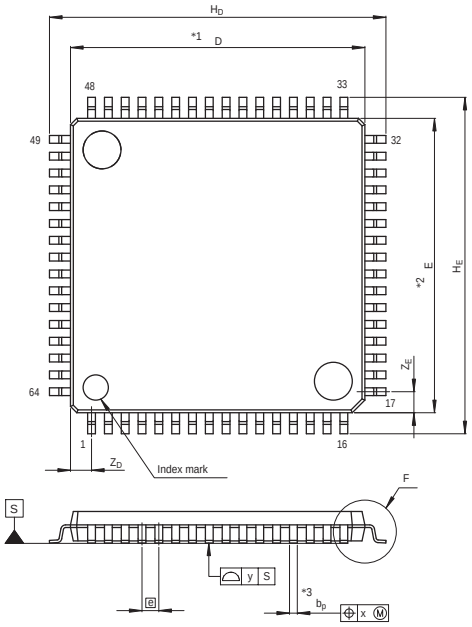
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g

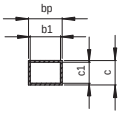


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

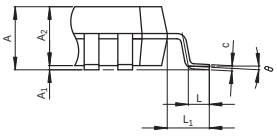
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.