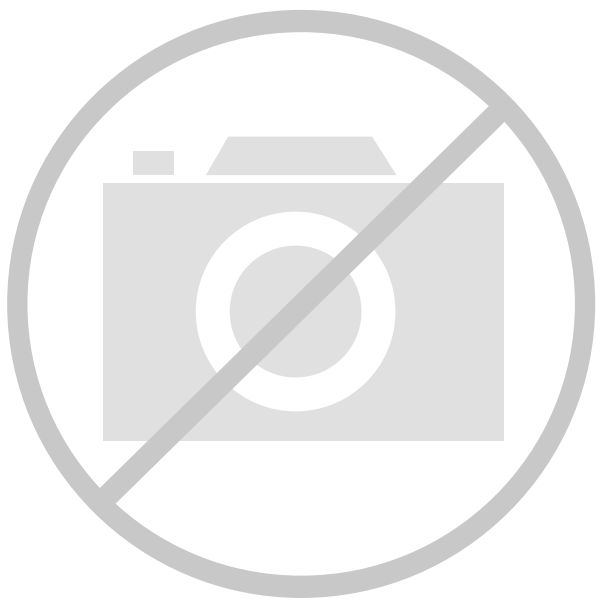




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2136csnfp-v0

Table 1.2 Specifications (2)

Item	Function	Description
Serial interface	UART0_0 and UART0_1	2 channels Clock synchronous serial I/O mode, clock asynchronous serial I/O mode
	UART2	1 channel Clock synchronous serial I/O mode, clock asynchronous serial I/O mode, I ² C mode (I ² C-bus), multiprocessor communication mode
Clock Synchronous serial interface	(SSU) SSU_0	1 channel (also used for the I ² C bus)
	(I ² C bus) I ² C_0	1 channel (also used for the SSU)
LIN module	HW-LIN_0	Hardware LIN 1 channel (timer RJ_0, UART0_0, or UART0_1 used)
A/D converter		Resolution: 10 bits × 12 channels, sample and hold function, sweep mode
Comparator B		2 circuits
Touch Sensor control unit (TSCU)		System CH × 4, electrostatic capacitive touch detection × 28
CRC calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash memory		• Program/erase voltage: VCC = 2.7 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • BGO (background operation) function (data flash)
Operating frequency/ Power supply voltage		CPU clock = 20 MHz (VCC = 2.7 V to 5.5 V) CPU clock = 5 MHz (VCC = 1.8 V to 5.5 V)
Current consumption		Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 4.0 μA (VCC = 3.0 V, wait mode f(XCIN) = 32 kHz) Typ. 2.2 μA (VCC = 3.0 V, stop mode)
Operating ambient temperature		-20°C to 85°C (N version) -40°C to 85°C (D version) ⁽¹⁾
Package		64-pin LQFP Package code: PLQP0064KB-A (previous code: 64P6Q-A) Package code: PLQP0064GA-A (previous code: 64P6U-A)

Note:

1. Specify the D version if it is to be used.

1.2 Product List

Table 1.3 lists product information. Figure 1.1 shows the Product Part Number Structure.

Table 1.3 Product List

Current of Dec 2011

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F21368SNFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	N version
R5F2136ASNFP	96 Kbytes		8 Kbytes	PLQP0064KB-A	
R5F2136CSNFP	128 Kbytes		10 Kbytes		
R5F21368SNFA	64 Kbytes		6 Kbytes	PLQP0064GA-A	D version
R5F2136ASNFA	96 Kbytes		8 Kbytes	PLQP0064KB-A	
R5F2136CSNFA	128 Kbytes		10 Kbytes		
R5F21368SDFP	64 Kbytes		6 Kbytes		
R5F2136ASDFP	96 Kbytes		8 Kbytes		
R5F2136CSDFP	128 Kbytes		10 Kbytes		
R5F21368SDFA	64 Kbytes		6 Kbytes	PLQP0064GA-A	
R5F2136ASDFA	96 Kbytes		8 Kbytes	PLQP0064GA-A	
R5F2136CSDFA	128 Kbytes		10 Kbytes		

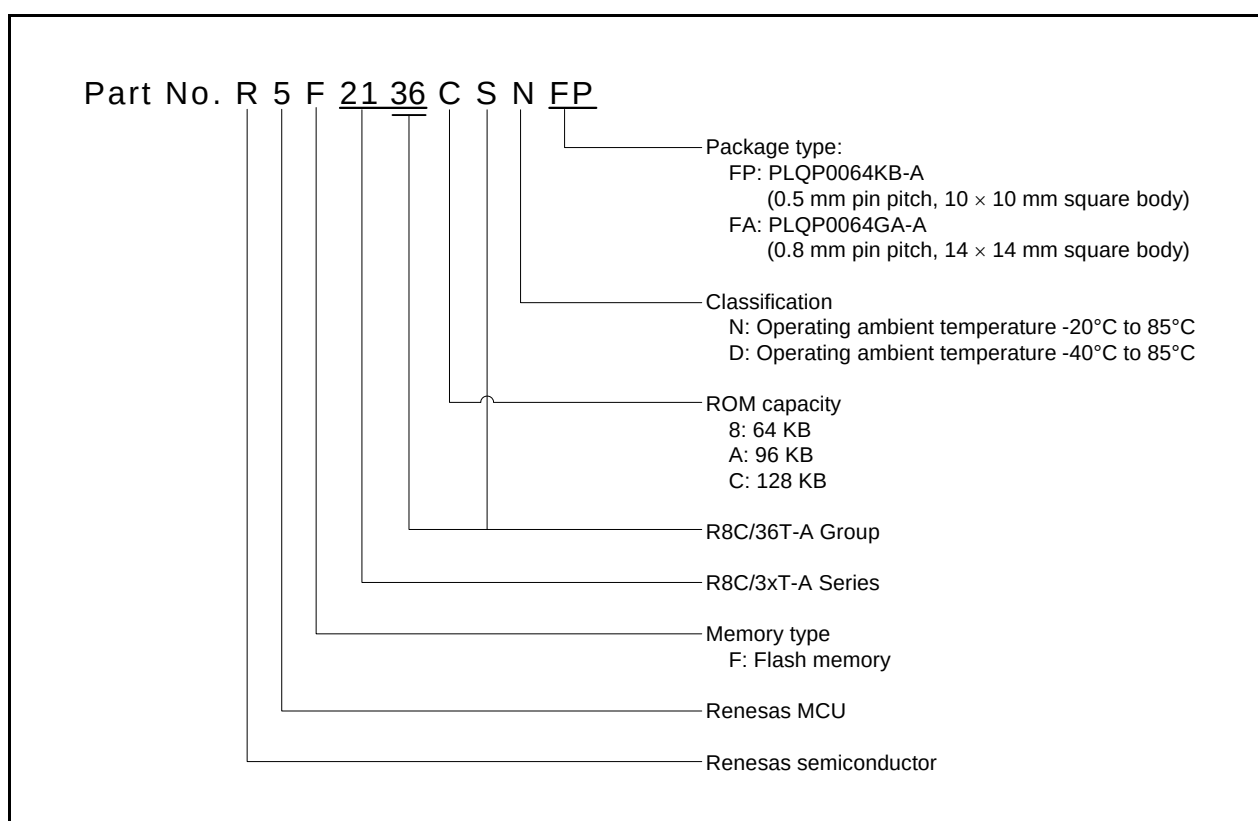


Figure 1.1 Product Part Number Structure

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Tables 1.4 to 1.6 list the Pin Name Information by Pin Number.

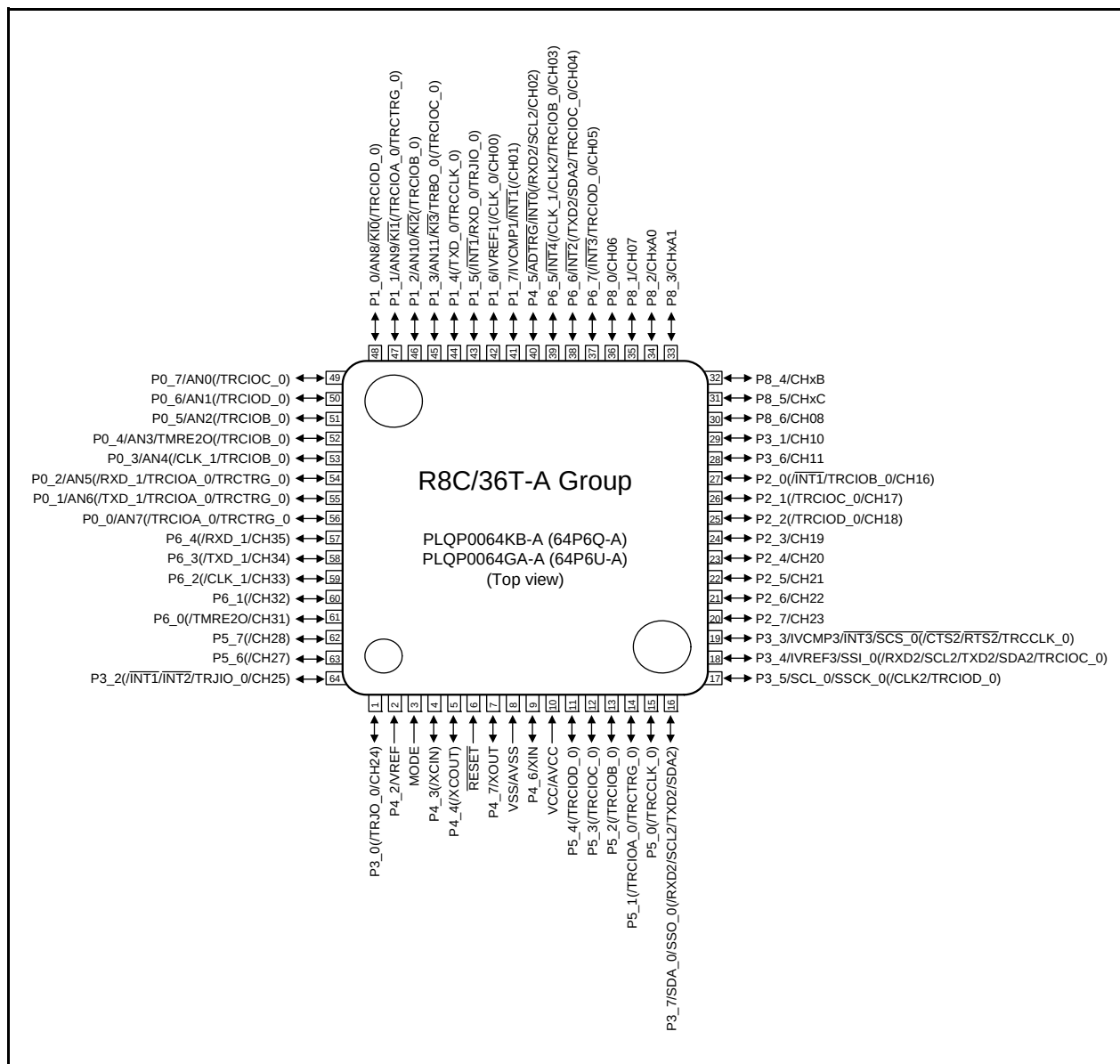


Figure 1.3 Pin Assignment (Top View)

Table 1.5 Pin Name Information by Pin Number (SSU/I²C, Timer RJ, and Timer RB2)

Port	Pin No.	SSU/I ² C						Timer RJ		Timer RB2
		SCL_0	SDA_0	SSI_0	SCS_0	SSCK_0	SSO_0	TRJO_0	TRJIO_0	TRBO_0
P0_0	56									
P0_1	55									
P0_2	54									
P0_3	53									
P0_4	52									
P0_5	51									
P0_6	50									
P0_7	49									
P1_0	48									
P1_1	47									
P1_2	46									
P1_3	45									TRBO_0
P1_4	44									
P1_5	43								TRJIO_0	
P1_6	42									
P1_7	41									
P2_0	27									
P2_1	26									
P2_2	25									
P2_3	24									
P2_4	23									
P2_5	22									
P2_6	21									
P2_7	20									
P3_0	1							TRJO_0		
P3_1	29									
P3_2	64								TRJIO_0	
P3_3	19				SCS_0					
P3_4	18			SSI_0						
P3_5	17	SCL_0				SSCK_0				
P3_6	28									
P3_7	16		SDA_0				SSO_0			
P4_2	2									
P4_3	4									
P4_4	5									
P4_5	40									
P4_6	9									
P4_7	7									
P5_0	15									
P5_1	14									
P5_2	13									
P5_3	12									
P5_4	11									
P5_6	63									
P5_7	62									
P6_0	61									
P6_1	60									
P6_2	59									
P6_3	58									
P6_4	57									
P6_5	39									
P6_6	38									
P6_7	37									
P8_0	36									
P8_1	35									
P8_2	34									
P8_3	33									
P8_4	32									
P8_5	31									
P8_6	30									

Table 1.6 Pin Name Information by Pin Number (Timer RC, Timer RE2, and Others)

Port	Pin No.	Timer RC						Timer RE2	Others		
		TRCCLK_0	TRCIOA_0	TRCIOB_0	TRCIOC_0	TRCIOD_0	TRCTRG_0	TMRE2O			
P0_0	56		TRCIOA_0				TRCTRG_0		AN7		
P0_1	55		TRCIOA_0				TRCTRG_0		AN6		
P0_2	54		TRCIOA_0				TRCTRG_0		AN5		
P0_3	53			TRCIOB_0					AN4		
P0_4	52			TRCIOB_0				TMRE2O	AN3		
P0_5	51			TRCIOB_0					AN2		
P0_6	50					TRCIOD_0			AN1		
P0_7	49				TRCIOC_0				AN0		
P1_0	48					TRCIOD_0			AN8	K10	
P1_1	47		TRCIOA_0				TRCTRG_0		AN9	K11	
P1_2	46			TRCIOB_0					AN10	K12	
P1_3	45				TRCIOC_0				AN11	K13	
P1_4	44	TRCCLK_0									
P1_5	43										
P1_6	42								IVREF1		CH00
P1_7	41								IVCMP1		CH01
P2_0	27			TRCIOB_0							CH16
P2_1	26				TRCIOC_0						CH17
P2_2	25					TRCIOD_0					CH18
P2_3	24										CH19
P2_4	23										CH20
P2_5	22										CH21
P2_6	21										CH22
P2_7	20										CH23
P3_0	1										CH24
P3_1	29										CH10
P3_2	64										CH25
P3_3	19	TRCCLK_0							IVCMP3		
P3_4	18				TRCIOC_0				IVREF3		
P3_5	17					TRCIOD_0					
P3_6	28										CH11
P3_7	16										
P4_2	2								VREF		
P4_3	4								XCIN		
P4_4	5								XCOU		
P4_5	40								ADTRG		CH02
P4_6	9								XIN		
P4_7	7								XOUT		
P5_0	15	TRCCLK_0									
P5_1	14		TRCIOA_0				TRCTRG_0				
P5_2	13			TRCIOB_0							
P5_3	12				TRCIOC_0						
P5_4	11					TRCIOD_0					
P5_6	63										CH27
P5_7	62										CH28
P6_0	61							TMRE2O			CH31
P6_1	60										CH32
P6_2	59										CH33
P6_3	58										CH34
P6_4	57										CH35
P6_5	39			TRCIOB_0							CH03
P6_6	38				TRCIOC_0						CH04
P6_7	37					TRCIOD_0					CH05
P8_0	36										CH06
P8_1	35										CH07
P8_2	34										CHxA0
P8_3	33										CHxA1
P8_4	32										CHxB
P8_5	31										CHxC
P8_6	30										CH08

1.5 Pin Functions

Tables 1.7 and 1.8 list Pin Functions.

Table 1.7 Pin Functions (1)

Item	Pin Name	I/O	Description
Power supply input	VCC, VSS	—	Apply 1.8 V through 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply input for the A/D converter. Connect a capacitor between pins AVCC and AVSS.
Reset input	RESET	I	Applying a low level to this pin resets the MCU.
MODE	MODE	I	Connect this pin to the VCC pin via a resistor.
XIN clock input	XIN	I	I/O for the XIN clock generation circuit.
XIN clock output	XOUT	I/O	Connect a ceramic resonator or a crystal oscillator between pins XIN and XOUT. ⁽¹⁾ To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XCIN clock input	XCIN	I	I/O for the XCIN clock generation circuit.
XCIN clock output	XCOUT	I/O	Connect a crystal oscillator between pins XCIN and XCOUT. ⁽¹⁾ To use an external clock, input it to the XCOUT pin and leave the XCIN pin open.
INT interrupt input	INT0 to INT4	I	INT interrupt input.
Key input interrupt	KI0 to KI3	I	Key input interrupt input.
Timer RJ_0	TRJIO_0	I/O	Input/output for timer RJ.
	TRJO_0	O	Output for timer RJ.
Timer RB2_0	TRBO_0	O	Output for timer RB2.
Timer RC_0	TRCLK_0	I	External clock input.
	TRCTR_0	I	External trigger input.
	TRCIOA_0, TRCIOB_0, TRCIOD_0	I/O	Input/output for timer RC.
Timer RE2	TMRE2O	O	Divided clock output.
Serial interface (UART0)	CLK_0, CLK_1	I/O	Transfer clock input/output.
	RXD_0, RXD_1	I	Serial data input.
	TXD_0, TXD_1	O	Serial data output.
Serial interface (UART2)	CTS2	I	Input for transmission control.
	RTS2	O	Output for reception control.
	SCL2	I/O	I ² C mode clock input/output.
	SDA2	I/O	I ² C mode data input/output.
	RXD2	I	Serial data input.
	TXD2	O	Serial data output.
	CLK2	I/O	Transfer clock input/output.
Synchronous serial communication unit (SSU_0)	SSI_0	I/O	Data input/output.
	SCS_0	I/O	Chip-select input/output.
	SSCK_0	I/O	Clock input/output.
	SSO_0	I/O	Data input/output.
I ² C bus (I ² C_0)	SCL_0	I/O	Clock input/output.
	SDA_0	I/O	Data input/output.
Reference voltage input	VREF	I	Reference voltage input for the A/D converter.

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

Table 1.8 Pin Functions (2)

Item	Pin Name	I/O	Description
A/D converter	AN0 to AN11	I	Analog input for the A/D converter.
	ADTRG	I	External trigger input for the A/D converter.
Comparator B	IVCMP1, IVCMP3	I	Analog voltage input for comparator B.
	IVREF1, IVREF3	I	Reference voltage input for comparator B.
Touch sensor control unit	CHxA0, CHxA1, CHxB, CHxC	I/O	Control pins for electrostatic capacitive touch detection.
	CH00 to CH08, CH10, CH11, CH16 to CH25, CH27, CH28, CH31 to CH35	I	Electrostatic capacitive touch detection pins.
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6_0 to P6_7, P8_0 to P8_6	I/O	8-bit CMOS input/output ports. Each port has an I/O select direction register, enabling switching input and output for each pin. For input ports, the presence or absence of a pull-up resistor can be selected by a program. All ports can be used as LED drive (high drive) ports.
Input port	P4_2	I	Input-only port.

3.2 Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 3.1 to 3.16 list the SFR Information. Table 3.17 lists the ID code Area, Option Function Select Area.

Table 3.1 SFR Information (1) (1)

Address	Symbol	Register Name	After Reset	Remarks
00000h				
00001h				
00002h				
00003h				
00004h	PM0	Processor Mode Register 0	00h	
00005h	PM1	Processor Mode Register 1	10000000b	
00006h				
00007h	PRCR	Protect Register	00h	
00008h	CM0	System Clock Control Register 0	00101000b	
00009h	CM1	System Clock Control Register 1	00100000b	
0000Ah	OCD	Oscillation Stop Detection Register	00h	
0000Bh	CM3	System Clock Control Register 3	00h	
0000Ch	CM4	System Clock Control Register 4	00000001b	
0000Dh				
0000Eh				
0000Fh				
00010h	CPSRF	Clock Prescaler Reset Flag	00h	
00011h				
00012h	FRA0	High-Speed On-Chip Oscillator Control Register 0	00h	
00013h				
00014h	FRA2	High-Speed On-Chip Oscillator Control Register 2	00h	
00015h				
00016h				
00017h				
00018h				
00019h				
0001Ah				
0001Bh				
0001Ch				
0001Dh				
0001Eh				
0001Fh				
00020h	RISR	Reset Interrupt Select Register	10000000b or 00000000b	(Note 2)
00021h	WDTR	Watchdog Timer Reset Register	FFh	
00022h	WDTs	Watchdog Timer Start Register	FFh	
00023h	WDTC	Watchdog Timer Control Register	01111111b	
00024h	CSPR	Count Source Protection Mode Register	10000000b or 00000000b	(Note 2)
00025h				
00026h				
00027h				
00028h	RSTFR	Reset Source Determination Register	00XXXXXXb	
00029h				
0002Ah				
0002Bh				
0002Ch	SVDC	STBY VDC Power Control Register	00h	
0002Dh				
0002Eh				
0002Fh				
00030h	CMPA	Voltage Monitor Circuit Control Register	00h	
00031h	VCAC	Voltage Monitor Circuit Edge Select Register	00h	
00032h	OCVREFCR	On-Chip Reference Voltage Control Register	00h	
00033h				
00034h	VCA2	Voltage Detection Register 2	00000000b or 00100000b	(Note 3)
00035h				
00036h	VD1LS	Voltage Detection 1 Level Select Register	00000111b	
00037h				
00038h	VW0C	Voltage Monitor 0 Circuit Control Register	1100XX10b or 1100XX11b	(Note 3)
00039h	VW1C	Voltage Monitor 1 Circuit Control Register	10001010b	

X: Undefined

Notes:

1. The blank areas are reserved. No access is allowed.
2. Depends on the CSPROINI bit in the OFS register.
3. Depends on the LVDASI bit in the OFS register.

Table 3.5 SFR Information (5) (1)

Address	Symbol	Register Name	After Reset	Remarks
000FAh				
000FBh				
000FCh				
000FDh				
000FEh				
000FFh				
00100h				
00101h				
00102h				
00103h				
00104h				
00105h				
00106h				
00107h				
00108h				
00109h				
0010Ah				
0010Bh				
0010Ch				
0010Dh				
0010Eh				
0010Fh				
00110h	TRJ_0	Timer RJ_0 Counter Register	FFFFh	
00111h				
00112h	TRJCR_0	Timer RJ_0 Control Register	00h	
00113h	TRJIOC_0	Timer RJ_0 I/O Control Register	00h	
00114h	TRJMR_0	Timer RJ_0 Mode Register	00h	
00115h	TRJISR_0	Timer RJ_0 Event Pin Select Register	00h	
00116h				
00117h				
00118h				
00119h				
0011Ah				
0011Bh				
0011Ch				
0011Dh				
0011Eh				
0011Fh				
00120h				
00121h				
00122h				
00123h				
00124h				
00125h				
00126h				
00127h				
00128h				
00129h				
0012Ah				
0012Bh				
0012Ch				
0012Dh				
0012Eh				
0012Fh				
00130h	TRBCR_0	Timer RB2_0 Control Register	00h	
00131h	TRBOCR_0	Timer RB2_0 One-Shot Control Register	00h	
00132h	TRBIOC_0	Timer RB2_0 I/O Control Register	00h	
00133h	TRBMR_0	Timer RB2_0 Mode Register	00h	
00134h	TRBPRES_0	Timer RB2_0 Prescaler Register	FFh	
00135h	TRBPR_0	Timer RB2_0 Primary Register	FFh	
00136h	TRBSC_0	Timer RB2_0 Secondary Register	FFh	
00137h	TRBIR_0	Timer RB2_0 Interrupt Request Register	00h	
00138h	TRCNT_0	Timer RC_0 Counter	0000h	
00139h				

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.8 SFR Information (8) (1)

Address	Symbol	Register Name	After Reset	Remarks
0023Ah	MSTCR2	Module Standby Control Register 2	00h	
0023Bh	MSTCR3	Module Standby Control Register 3	00h	
0023Ch	MSTCR4	Module Standby Control Register 4	00h	
0023Dh				
0023Eh				
0023Fh				
00240h				
00241h				
00242h				
00243h				
00244h				
00245h				
00246h				
00247h				
00248h				
00249h				
0024Ah				
0024Bh				
0024Ch				
0024Dh				
0024Eh				
0024Fh				
00250h				
00251h				
00252h	FST	Flash Memory Status Register	10000X00b	
00253h				
00254h	FMR0	Flash Memory Control Register 0	00h	
00255h	FMR1	Flash Memory Control Register 1	00h	
00256h	FMR2	Flash Memory Control Register 2	00h	
00257h				
00258h				
00259h				
0025Ah				
0025Bh				
0025Ch				
0025Dh				
0025Eh				
0025Fh				
00260h	AIADR0L	Address Match Interrupt Address 0L Register	XXXXh	
00261h				
00262h	AIADR0H	Address Match Interrupt Address 0H Register	0000XXXXb	
00263h	AIEN0	Address Match Interrupt Enable 0 Register	00h	
00264h	AIADR1L	Address Match Interrupt Address 1L Register	XXXXh	
00265h				
00266h	AIADR1H	Address Match Interrupt Address 1H Register	0000XXXXb	
00267h	AIEN1	Address Match Interrupt Enable 1 Register	00h	
00268h				
00269h				
0026Ah				
0026Bh				
0026Ch				
0026Dh				
0026Eh				
0026Fh				
00270h				
00271h				
00272h				
00273h				
00274h				
00275h				
00276h				
00277h				
00278h				
00279h				
0027Ah				
0027Bh				
0027Ch				
0027Dh				
0027Eh				
0027Fh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.15 SFR Information (15) ⁽¹⁾

Address	Symbol	Register Name	After Reset	Remarks
06C90h	DTCCR10	DTC Control Register 10	XXh	
06C91h	DTBLS10	DTC Block Size Register 10	XXh	
06C92h	DTCCT10	DTC Transfer Count Register 10	XXh	
06C93h	DTRLD10	DTC Transfer Count Reload Register 10	XXh	
06C94h	DTSAR10	DTC Source Address Register 10	XXXXh	
06C95h				
06C96h	DTDAR10	DTC Destination Address Register 10	XXXXh	
06C97h				
06C98h	DTCCR11	DTC Control Register 11	XXh	
06C99h	DTBLS11	DTC Block Size Register 11	XXh	
06CA0h	DTCCT11	DTC Transfer Count Register 11	XXh	
06C9Bh	DTRLD11	DTC Transfer Count Reload Register 11	XXh	
06C9Ch	DTSAR11	DTC Source Address Register 11	XXXXh	
06C9Dh				
06C9Eh	DTDAR11	DTC Destination Address Register 11	XXXXh	
06C9Fh				
06CA0h	DTCCR12	DTC Control Register 12	XXh	
06CA1h	DTBLS12	DTC Block Size Register 12	XXh	
06CA2h	DTCCT12	DTC Transfer Count Register 12	XXh	
06CA3h	DTRLD12	DTC Transfer Count Reload Register 12	XXh	
06CA4h	DTSAR12	DTC Source Address Register 12	XXXXh	
06CA5h				
06CA6h	DTDAR12	DTC Destination Address Register 12	XXXXh	
06CA7h				
06CA8h	DTCCR13	DTC Control Register 13	XXh	
06CA9h	DTBLS13	DTC Block Size Register 13	XXh	
06CAAh	DTCCT13	DTC Transfer Count Register 13	XXh	
06CABh	DTRLD13	DTC Transfer Count Reload Register 13	XXh	
06CACh	DTSAR13	DTC Source Address Register 13	XXXXh	
06CADh				
06CAEh	DTDAR13	DTC Destination Address Register 13	XXXXh	
06CAFh				
06CB0h	DTCCR14	DTC Control Register 14	XXh	
06CB1h	DTBLS14	DTC Block Size Register 14	XXh	
06CB2h	DTCCT14	DTC Transfer Count Register 14	XXh	
06CB3h	DTRLD14	DTC Transfer Count Reload Register 14	XXh	
06CB4h	DTSAR14	DTC Source Address Register 14	XXXXh	
06CB5h				
06CB6h	DTDAR14	DTC Destination Address Register 14	XXXXh	
06CB7h				
06CB8h	DTCCR15	DTC Control Register 15	XXh	
06CB9h	DTBLS15	DTC Block Size Register 15	XXh	
06CBAh	DTCCT15	DTC Transfer Count Register 15	XXh	
06CBBh	DTRLD15	DTC Transfer Count Reload Register 15	XXh	
06CBCh	DTSAR15	DTC Source Address Register 15	XXXXh	
06CBDh				
06CBEh	DTDAR15	DTC Destination Address Register 15	XXXXh	
06CBFh				
06CC0h	DTCCR16	DTC Control Register 16	XXh	
06CC1h	DTBLS16	DTC Block Size Register 16	XXh	
06CC2h	DTCCT16	DTC Transfer Count Register 16	XXh	
06CC3h	DTRLD16	DTC Transfer Count Reload Register 16	XXh	
06CC4h	DTSAR16	DTC Source Address Register 16	XXXXh	
06CC5h				
06CC6h	DTDAR16	DTC Destination Address Register 16	XXXXh	
06CC7h				
06CC8h	DTCCR17	DTC Control Register 17	XXh	
06CC9h	DTBLS17	DTC Block Size Register 17	XXh	
06CAAh	DTCCT17	DTC Transfer Count Register 17	XXh	
06CCBh	DTRLD17	DTC Transfer Count Reload Register 17	XXh	
06CCCh	DTSAR17	DTC Source Address Register 17	XXXXh	
06CCDh				
06CCEh	DTDAR17	DTC Destination Address Register 17	XXXXh	
06CCFh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.16 SFR Information (16) ⁽¹⁾

Address	Symbol	Register Name	After Reset	Remarks
06CD0h	DTCCR18	DTC Control Register 18	XXh	
06CD1h	DTBLS18	DTC Block Size Register 18	XXh	
06CD2h	DTCCT18	DTC Transfer Count Register 18	XXh	
06CD3h	DTRL18	DTC Transfer Count Reload Register 18	XXh	
06CD4h	DTSAR18	DTC Source Address Register 18	XXXXh	
06CD5h				
06CD6h	DTDAR18	DTC Destination Address Register 18	XXXXh	
06CD7h				
06CD8h	DTCCR19	DTC Control Register 19	XXh	
06CD9h	DTBLS19	DTC Block Size Register 19	XXh	
06CDAh	DTCCT19	DTC Transfer Count Register 19	XXh	
06CDBh	DTRL19	DTC Transfer Count Reload Register 19	XXh	
06CDC	DTSAR19	DTC Source Address Register 19	XXXXh	
06CDDh				
06CDEh	DTDAR19	DTC Destination Address Register 19	XXXXh	
06CDFh				
06CE0h	DTCCR20	DTC Control Register 20	XXh	
06CE1h	DTBLS20	DTC Block Size Register 20	XXh	
06CE2h	DTCCT20	DTC Transfer Count Register 20	XXh	
06CE3h	DTRL20	DTC Transfer Count Reload Register 20	XXh	
06CE4h	DTSAR20	DTC Source Address Register 20	XXXXh	
06CE5h				
06CE6h	DTDAR20	DTC Destination Address Register 20	XXXXh	
06CE7h				
06CE8h	DTCCR21	DTC Control Register 21	XXh	
06CE9h	DTBLS21	DTC Block Size Register 21	XXh	
06CEAh	DTCCT21	DTC Transfer Count Register 21	XXh	
06CEBh	DTRL21	DTC Transfer Count Reload Register 21	XXh	
06CECh	DTSAR21	DTC Source Address Register 21	XXXXh	
06CEDh				
06CEEh	DTDAR21	DTC Destination Address Register 21	XXXXh	
06CEFh				
06CF0h	DTCCR22	DTC Control Register 22	XXh	
06CF1h	DTBLS22	DTC Block Size Register 22	XXh	
06CF2h	DTCCT22	DTC Transfer Count Register 22	XXh	
06CF3h	DTRL22	DTC Transfer Count Reload Register 22	XXh	
06CF4h	DTSAR22	DTC Source Address Register 22	XXXXh	
06CF5h				
06CF6h	DTDAR22	DTC Destination Address Register 22	XXXXh	
06CF7h				
06CF8h	DTCCR23	DTC Control Register 23	XXh	
06CF9h	DTBLS23	DTC Block Size Register 23	XXh	
06CFAh	DTCCT23	DTC Transfer Count Register 23	XXh	
06CFBh	DTRL23	DTC Transfer Count Reload Register 23	XXh	
06CFCh	DTSAR23	DTC Source Address Register 23	XXXXh	
06CFDh				
06CFEh	DTDAR23	DTC Destination Address Register 23	XXXXh	
06CFFh				
06D00h to 06FFFh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.17 ID code Area, Option Function Select Area

Address	Symbol	Area Name	After Reset	Address size
⋮				
0FFDBh	OFS2	Option Function Select Register 2	(Note 1)	
⋮				
0FFDFh	ID1		(Note 2)	
⋮				
0FFE3h	ID2		(Note 2)	
⋮				
0FFEBh	ID3		(Note 2)	
⋮				
0FFEFh	ID4		(Note 2)	
⋮				
0FFF3h	ID5		(Note 2)	
⋮				
0FFF7h	ID6		(Note 2)	
⋮				
0FFFBh	ID7		(Note 2)	
⋮				
0FFFFh	OFS	Option Function Select Register	(Note 1)	

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the option function select area. Erasing the block including the option function select area sets the option function select area to FFh.
2. The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the ID code area. Erasing the block including the ID code area sets the ID code area to FFh.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V _{CC} /A _V _{CC} I _{CE} V _{CC}	Supply voltage		−0.3 to 6.5	V
V _I	Input voltage		−0.3 to V _{CC} + 0.3	V
V _O	Output voltage		−0.3 to V _{CC} + 0.3	V
P _d	Power dissipation	−40°C ≤ T _{opr} ≤ 85°C	500	mW
T _{opr}	Operating ambient temperature		−20 to 85 (N version)/ −40 to 85 (D version)	°C
T _{stg}	Storage temperature		−65 to 150	°C

4.3 Peripheral Function Characteristics

Table 4.3 A/D Converter Characteristics
($V_{CC}/AV_{CC} = V_{ref} = 2.2\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_{opr} = -20^{\circ}\text{C to }85^{\circ}\text{C}$ (N version)/
 $-40^{\circ}\text{C to }85^{\circ}\text{C}$ (D version), unless otherwise specified)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		Vref = AVcc		—	—	10	Bit
—	Absolute accuracy	10-bit mode	Vref = AVcc = 5.0 V	AN0 to AN11 input	—	—	±3	LSB
			Vref = AVcc = 3.3 V	AN0 to AN11 input	—	—	±5	LSB
			Vref = AVcc = 3.0 V	AN0 to AN11 input	—	—	±5	LSB
			Vref = AVcc = 2.2 V	AN0 to AN11 input	—	—	±5	LSB
		8-bit mode	Vref = AVcc = 5.0 V	AN0 to AN11 input	—	—	±2	LSB
			Vref = AVcc = 3.3 V	AN0 to AN11 input	—	—	±2	LSB
			Vref = AVcc = 3.0 V	AN0 to AN11 input	—	—	±2	LSB
			Vref = AVcc = 2.2 V	AN0 to AN11 input	—	—	±2	LSB
φAD	A/D conversion clock		4.0 V ≤ Vref = AVcc ≤ 5.5 V ⁽¹⁾		2	—	20	MHz
			3.2 V ≤ Vref = AVcc ≤ 5.5 V ⁽¹⁾		2	—	16	MHz
			2.7 V ≤ Vref = AVcc ≤ 5.5 V ⁽¹⁾		2	—	10	MHz
			2.2 V ≤ Vref = AVcc ≤ 5.5 V ⁽¹⁾		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
Ivref	Vref current		Vcc = 5 V, XIN = f1 = fAD = 20 MHz		—	45	—	μA
tconv	Conversion time	10-bit mode	Vref = AVcc = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
		8-bit mode	Vref = AVcc = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
tsAMP	Sampling time		φAD = 20 MHz		0.8	—	—	μs
Vref	Reference voltage				2.2	—	AVcc	V
VIA	Analog input voltage ⁽²⁾				0	—	Vref	V
OCVREF	On-chip reference voltage		2MHz ≤ φAD ≤ 4MHz		1.19	1.34	1.49	V

Notes:

1. If the CPU and the flash memory stop, the A/D conversion result will be undefined.
2. When the analog input voltage exceeds the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 4.4 Comparator B Characteristics
($V_{CC}/AV_{CC} = 2.2\text{ V to }5.5\text{ V}$, $T_{opr} = -20^{\circ}\text{C to }85^{\circ}\text{C}$ (N version)/ $-40^{\circ}\text{C to }85^{\circ}\text{C}$ (D version),
unless otherwise specified)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	$V_{CC} - 1.4$	V
V_I	IVCMP1, IVCMP3 input voltage		-0.3	—	$V_{CC} + 0.3$	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time (1)	$V_I = V_{ref} \pm 100\text{ mV}$	—	0.1	—	μs
I_{CMP}	Comparator operating current	$V_{CC} = 5.0\text{ V}$	—	17.5	—	μA

Note:

1. When the digital filter is not selected.

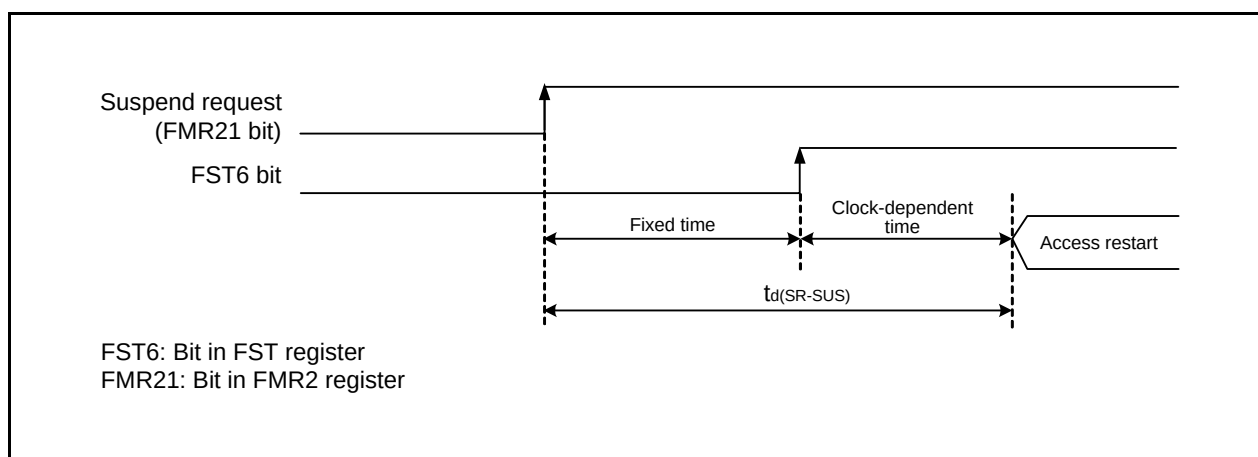


Figure 4.2 Time Delay from Suspend Request until Suspend

Table 4.7 Voltage Detection 0 Circuit Characteristics
**(Measurement conditions: $V_{CC} = 1.8\text{ V to }5.5\text{ V}$, $T_{opr} = -20^{\circ}\text{C to }85^{\circ}\text{C}$ (N version)/
 $-40^{\circ}\text{C to }85^{\circ}\text{C}$ (D version))**

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
Vdet0	Voltage detection level Vdet0_0 ⁽¹⁾	When Vcc falls	1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 ⁽¹⁾	When Vcc falls	2.15	2.35	2.55	V
	Voltage detection level Vdet0_2 ⁽¹⁾	When Vcc falls	2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 ⁽¹⁾	When Vcc falls	3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time ⁽²⁾	At the falling of Vcc from 5 V to (Vdet0 – 0.1) V	—	6	150	μs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	1.5	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

Notes:

1. The voltage detection level must be selected with bits VDSEL0 and VDSEL1 in the OFS register.
2. Time until the voltage monitor 0 reset is generated after the voltage passes Vdet0.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 4.8 Voltage Detection 1 Circuit Characteristics
(Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/
–40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
Vdet1	Voltage detection level Vdet1_0 ⁽¹⁾	When Vcc falls	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 ⁽¹⁾	When Vcc falls	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 ⁽¹⁾	When Vcc falls	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 ⁽¹⁾	When Vcc falls	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 ⁽¹⁾	When Vcc falls	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 ⁽¹⁾	When Vcc falls	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 ⁽¹⁾	When Vcc falls	2.80	3.10	3.40	V
	Voltage detection level Vdet1_7 ⁽¹⁾	When Vcc falls	2.95	3.25	3.55	V
	Voltage detection level Vdet1_8 ⁽¹⁾	When Vcc falls	3.10	3.40	3.70	V
	Voltage detection level Vdet1_9 ⁽¹⁾	When Vcc falls	3.25	3.55	3.85	V
	Voltage detection level Vdet1_A ⁽¹⁾	When Vcc falls	3.40	3.70	4.00	V
	Voltage detection level Vdet1_B ⁽¹⁾	When Vcc falls	3.55	3.85	4.15	V
	Voltage detection level Vdet1_C ⁽¹⁾	When Vcc falls	3.70	4.00	4.30	V
	Voltage detection level Vdet1_D ⁽¹⁾	When Vcc falls	3.85	4.15	4.45	V
	Voltage detection level Vdet1_E ⁽¹⁾	When Vcc falls	4.00	4.30	4.60	V
	Voltage detection level Vdet1_F ⁽¹⁾	When Vcc falls	4.15	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_6 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time ⁽²⁾	At the falling of Vcc from 5 V to (Vdet1 – 0.1) V	—	60	150	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

Notes:

1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 4.9 Voltage Detection 2 Circuit Characteristics
(Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/
–40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level Vdet2_0	When Vcc falls	3.70	4.00	4.30	V
—	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		—	0.1	—	μs
—	Voltage detection 2 circuit response time ⁽¹⁾	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	—	20	150	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽²⁾		—	—	100	μs

Notes:

1. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

**Table 4.17 DC Characteristics (4) [2.7 V ≤ Vcc < 3.3 V]
(Topr = −20°C to 85°C (N version)/−40°C to 85°C (D version), unless otherwise specified))**

Symbol	Parameter		Conditions							Standard (4)			Unit
			Oscillation		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ.	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	10 MHz	Off	Off	125 kHz	No division	—		—	3.5	10	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	—		—	1.5	7.5	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz (3)	125 kHz	No division	—		—	7.0	15	mA
			Off	Off	20 MHz (3)	125 kHz	Divide-by-8	—		—	3.0	—	mA
			Off	Off	10 MHz (3)	125 kHz	No division	—		—	4.0	—	mA
			Off	Off	10 MHz (3)	125 kHz	Divide-by-8	—		—	1.5	—	mA
			Off	Off	4 MHz (3)	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRC = 1		—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 SVC0 = 0		—	90	390	μA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 SVC0 = 0		—	80	400	μA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 SVC0 = 0	Program operation on RAM Flash memory off	—	40	—	μA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	90	μA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	4	80	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	3.5	—	μA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	—	2.2	6.0	μA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	—	30	—	μA

Notes:

1. Vcc = 2.7 V to 3.3 V, single-chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

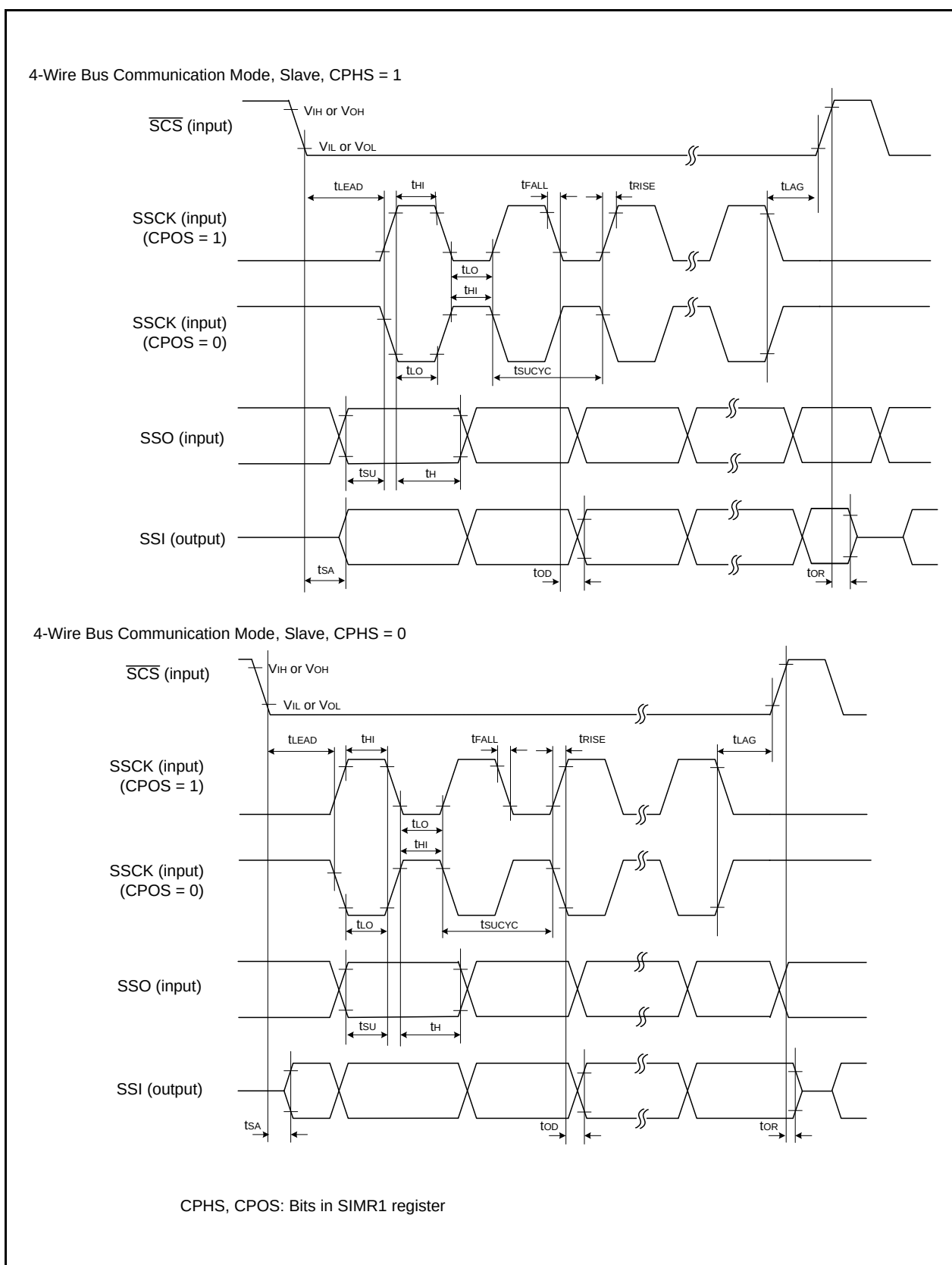


Figure 4.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

REVISION HISTORY	R8C/36T-A Group Datasheet
------------------	---------------------------

Rev.	Date	Description	
		Page	Summary
0.01	Feb 23, 2011	—	First Edition issued
1.00	Dec 09, 2011	All pages	"Preliminary", "Under development" deleted, "sensor control unit" → "touch sensor control unit"
		2, 3	Tables 1.1 and 1.2 revised
		6	Figure 1.3 "P3_10/CH10" → "P3_1/CH10"
		11	Table 1.8 "Touch sensor control unit" added
		13	2.1 revised
		16, 17, 19 to 22, 24 to 28	Tables 3.1, 3.2, 3.4 to 3.7, 3.9 to 3.13
		32	Table 3.17 revised, Note 2 added
		33 to 56	"4. Electrical Characteristics" added

All trademarks and registered trademarks are the property of their respective owners.