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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	CPU12
Core Size	16-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	83
Program Memory Size	4KB (4K x 8)
Program Memory Type	EEPROM
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc812a4cpve8

Chapter 18
Electrical Characteristics

Chapter 19
Mechanical Specifications

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0041	Loop Divider Register Low (LDVL) See page 113.	Read:	LDV7	LDV6	LDV5	LDV4	LDV3	LDV2	LDV1	LDV0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0042	Reference Divider Register High (RDVH) See page 114.	Read:	0	0	0	0	RDV11	RDV10	RDV9	RDV8
		Write:								
		Reset:	0	0	0	0	1	1	1	1
$0043	Reference Divider Register Low (RDVL) See page 114.	Read:	RDV7	RDV6	RDV5	RDV4	RDV3	RDV2	RDV1	RDV0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0044	Reserved		R	R	R	R	R	R	R	R
$0045	Reserved		R	R	R	R	R	R	R	R
$0046	Reserved		R	R	R	R	R	R	R	R
$0047	Clock Control Register (CLKCTL) See page 114.	Read:	LCKF	PLLON	PLLS	BCSC	BCSB	BCSA	MCSB	MCSA
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0048	Reserved		R	R	R	R	R	R	R	R
↓	↓									
$005F	Reserved		R	R	R	R	R	R	R	R
$0060	ATD Control Register 0 (ATDCTL0) See page 199.	Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0061	ATD Control Register 1 (ATDCTL1) See page 199.	Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0062	ATD Control Register 2 (ATDCTL2) See page 200.	Read:	ADPU	AFFC	AWAI	0	0	0	ASCIE	ASCIF
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0063	ATD Control Register 3 (ATDCTL3) See page 201.	Read:	0	0	0	0	0	0	FRZ1	FRZ0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0064	ATD Control Register 4 (ATDCTL4) See page 201.	Read:	0	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Write:								
		Reset:	0	0	0	0	0	0	0	1
$0065	ATD Control Register 5 (ATDCTL5) See page 202.	Read:	0	S8CM	SCAN	MULT	CD	CC	CB	CA
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Figure 2-1. Register Map (Sheet 6 of 14)

Chapter 4
Resets and Interrupts

4.1 Introduction

Resets and interrupts are exceptions. Each exception has a 16-bit vector that points to the memory location of the associated exception-handling routine. Vectors are stored in the upper 128 bytes of the standard 64-Kbyte address map.

The six highest vector addresses are used for resets and non-maskable interrupt sources. The remainder of the vectors are used for maskable interrupts, and all must be initialized to point to the address of the appropriate service routine.

4.2 Exception Priority

A hardware priority hierarchy determines which reset or interrupt is serviced first when simultaneous requests are made. Six sources are not maskable. The remaining sources are maskable and any one of them can be given priority over other maskable interrupts.

The priorities of the non-maskable sources are:

1. POR (power-on reset) or $\overline{\text{RESET}}$ pin
2. Clock monitor reset
3. COP (computer operating properly) watchdog reset
4. Unimplemented instruction trap
5. Software interrupt instruction (SWI)
6. $\overline{\text{XIRQ}}$ signal (if X bit in CCR = 0)

4.3 Maskable Interrupts

Maskable interrupt sources include on-chip peripheral systems and external interrupt service requests. Interrupts from these sources are recognized when the global interrupt mask bit (I) in the CCR is cleared. The default state of the I bit out of reset is 1, but it can be written at any time.

Interrupt sources are prioritized by default but any one maskable interrupt source may be assigned the highest priority by means of the HPRIO register. The relative priorities of the other sources remain the same.

An interrupt that is assigned highest priority is still subject to global masking by the I bit in the CCR or by any associated local bits. Interrupt vectors are not affected by priority assignment. HPRIO can only be written while the I bit is set (interrupts inhibited). Table 4-1 lists interrupt sources and vectors in default order of priority.

commands can be executed while the CPU is operating normally. Other BDM commands are firmware based and require the BDM firmware to be enabled and active for execution.

In special single-chip mode, BDM is enabled and active immediately out of reset. BDM is available in all other operating modes, but must be enabled before it can be activated. BDM should not be used in special peripheral mode because of potential bus conflicts.

Once enabled, background mode can be made active by a serial command sent via the BKGD pin or execution of a CPU12 BGND instruction. While background mode is active, the CPU can interpret special debugging commands, and read and write CPU registers, peripheral registers, and locations in memory.

While BDM is active, the CPU executes code located in a small on-chip ROM mapped to addresses $FF20 to $FFFF, and BDM control registers are accessible at addresses $FF00 to $FF06. The BDM ROM replaces the regular system vectors while BDM is active. While BDM is active, the user memory from $FF00 to $FFFF is not in the map except through serial BDM commands.

5.3 Internal Resource Mapping

The internal register block, RAM, and EEPROM have default locations within the 64-Kbyte standard address space but may be reassigned to other locations during program execution by setting bits in mapping registers INITRG, INITRM, and INITEE. During normal operating modes, these registers can be written once. It is advisable to explicitly establish these resource locations during the initialization phase of program execution, even if default values are chosen, to protect the registers from inadvertent modification later.

Writes to the mapping registers go into effect between the cycle that follows the write and the cycle after that. To assure that there are no unintended operations, a write to one of these registers should be followed with a NOP (no operation) instruction.

If conflicts occur when mapping resources, the register block takes precedence over the other resources; RAM or EEPROM addresses occupied by the register block are not available for storage. When active, BDM ROM takes precedence over other resources although a conflict between BDM ROM and register space is not possible. Table 5-2 shows resource mapping precedence.

Table 5-2. Mapping Precedence

Precedence	Resource
1	BDM ROM (if active)
2	Register space
3	RAM
4	EEPROM
5	External memory

All address space not used by internal resources is external memory by default.

The memory expansion module manages three memory overlay windows:

1. Program
2. Data
3. One extra page overlay

The sizes and locations of the program and data overlay windows are fixed. One of two locations can be selected for the extra page (EPAGE).

Chapter 7
EEPROM

7.1 Introduction

The MC68HC812A4 EEPROM (electrically erasable, programmable, read-only memory) serves as a 4096-byte nonvolatile memory which can be used for frequently accessed static data or as fast access program code. Operating system kernels and standard subroutines would benefit from this feature.

The MC68HC812A4 EEPROM is arranged in a 16-bit configuration. The EEPROM array may be read as either bytes, aligned words, or misaligned words. Access times are one bus cycle for byte and aligned word access and two bus cycles for misaligned word operations.

Programming is by byte or aligned word. Attempts to program or erase misaligned words will fail. Only the lower byte will be latched and programmed or erased. Programming and erasing of the user EEPROM can be done in all modes.

Each EEPROM byte or aligned word must be erased before programming. The EEPROM module supports byte, aligned word, row (32 bytes), or bulk erase, all using the internal charge pump. Bulk erasure of odd and even rows is also possible in test modes; the erased state is $FF. The EEPROM module has hardware interlocks which protect stored data from corruption by accidentally enabling the program/erase voltage. Programming voltage is derived from the internal V_{DD} supply with an internal charge pump. The EEPROM has a minimum program/erase life of 10,000 cycles over the complete operating temperature range.

7.2 EEPROM Programmer's Model

The EEPROM module consists of two separately addressable sections. The first is a 4-byte memory mapped control register block used for control, testing and configuration of the EEPROM array. The second section is the EEPROM array itself.

At reset, the 4-byte register section starts at address $00F0 and the EEPROM array is located from addresses $1000 to $1FFF (see Figure 7-1). For information on remapping the register block and EEPROM address space, refer to Chapter 5 Operating Modes and Resource Mapping.

Read/write access to the memory array section can be enabled or disabled by the EEON control bit in the INITEE register. This feature allows the access of memory mapped resources that have lower priority than the EEPROM memory array. EEPROM control registers can be accessed and EEPROM locations may be programmed or erased regardless of the state of EEON.

Using the normal EEPROG control, it is possible to continue program/erase operations during wait. For lowest power consumption during wait, stop program/erase by turning off EEPGM.

If the stop mode is entered during programming or erasing, program/erase voltage is automatically turned off and the RC clock (if enabled) is stopped. However, the EEPGM control bit remains set. When stop mode is terminated, the program/erase voltage automatically turns back on if EEPGM is set.

At low bus frequencies, the RC clock must be turned on for program/erase.

Table 7-2. Erase Selection

Byte	Row	Block Size
0	0	Bulk erase entire EEPROM array
0	1	Row erase 32 bytes
1	0	Byte or aligned word erase
1	1	Byte or aligned word erase

ERASE — Erase Control Bit

1 = EEPROM configuration for erasure
0 = EEPROM configuration for programming
Write anytime, if EEPGM = 0
This bit configures the EEPROM for erasure or programming.

EELAT — EEPROM Latch Control Bit

1 = EEPROM address and data bus latches set up for programming or erasing
0 = EEPROM set up for normal reads
Write: Anytime, if EEPGM = 0

NOTE

When EELAT is set, the entire EEPROM is unavailable for reads; therefore, no program residing in the EEPROM can be executed while attempting to program unused EEPROM space. Care should be taken that no references to the EEPROM are used while programming. Interrupts should be turned off if the vectors are in the EEPROM. Timing and any serial communications must be done with polling during the programming process.

BYTE, ROW, ERASE, and EELAT bits can be written simultaneously or in any sequence.

EEPGM — Program and Erase Enable Bit

1 = Applies program/erase voltage to EEPROM
0 = Disables program/erase voltage to EEPROM
The EEPGM bit can be set only after EELAT has been set. When EELAT and EEPGM are set simultaneously, EEPGM remains clear but EELAT is set.

The BULKP, BYTE, ROW, ERASE, and EELAT bits cannot be changed when EEPGM is set. To complete a program or erase, two successive writes to clear EEPGM and EELAT bits are required before reading the programmed data. A write to an EEPROM location has no effect when EEPGM is set. Latched address and data cannot be modified during program or erase.

A program or erase operation should follow this sequence:

1. Write BYTE, ROW, and ERASE to the desired value; write EELAT = 1.
2. Write a byte or an aligned word to an EEPROM address.
3. Write EEPGM = 1.
4. Wait for programming (t_{PROG}) or erase (t_{Erase}) delay time.
5. Write EEPGM = 0.
6. Write EELAT = 0.

By jumping from step 5 to step 2, it is possible to program/erase more bytes or words without intermediate EEPROM reads.

The external E-clock may be the stretched E-clock, the E-clock, or no clock depending on the selection of control bits ESTR and IVIS in the MODE register and NECLK in the PEAR register.

8.4 Memory Expansion Registers

This section describes the memory expansion registers.

8.4.1 Port F Data Register

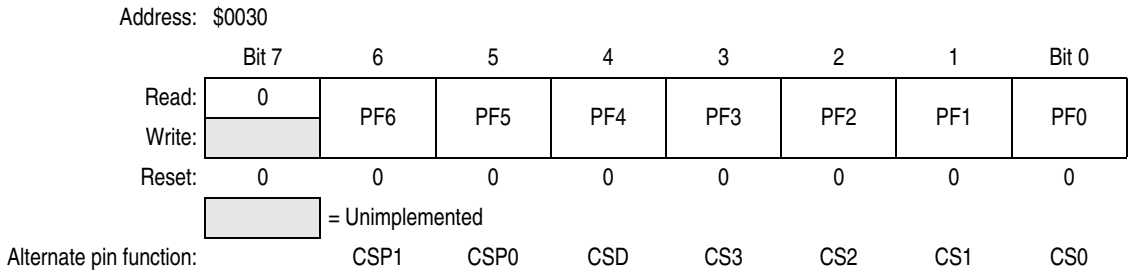


Figure 8-7. Port F Data Register (PORTF)

Read: Anytime
Write: Anytime

Seven port F pins are associated with chip-selects. Any pin not used as a chip-select can be used as general-purpose I/O. All pins are pulled up when inputs (if pullups are enabled). Enabling a chip-select overrides the associated data direction bit and port data bit.

8.4.2 Port G Data Register

Figure 8-8. Port G Data Register (PORTG)

Read: Anytime
Write: Anytime

Six port G pins are associated with memory expansion. Any pin not used for memory expansion can be used as general-purpose I/O. All pins are pulled up when inputs (if pullups are enabled). Enabling a memory expansion address with the memory expansion assignment register overrides the associated data direction bit and port data bit.

9.2.2 Port D Data Direction Register

Address: $0007

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	0	0	0	0	0	0	0	0

Figure 9-2. Port D Data Direction Register (DDRD)

Read: Anytime
Write: Anytime

This register is not in the map in wide expanded modes or in special expanded narrow mode with MODE register bit EMD set.

Data direction register D is associated with port D and designates each pin as an input or output.

DDRD7–DDRD0 — Data Direction Port D Bits

1 = Associated pin is an output.
0 = Associated pin is an input.

9.2.3 Port D Key Wakeup Interrupt Enable Register

Address: $0020

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	0	0	0	0	0	0	0	0

Figure 9-3. Port D Key Wakeup Interrupt Enable Register (KWIED)

Read: Anytime
Write: Anytime

This register is not in the map in wide expanded modes and in special expanded narrow mode with MODE register bit EMD set.

KWIED7–KWIED0 — Key Wakeup Port D Interrupt Enable Bits

1 = Interrupt for the associated bit is enabled.
0 = Interrupt for the associated bit is disabled.

9.2.14 Port J Pullup/Pulldown Select Register

Address: $002D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PUPSJ7	PUPSJ6	PUPSJ5	PUPSJ4	PUPSJ3	PUPSJ2	PUPSJ1	PUPSJ0
Reset:	0	0	0	0	0	0	0	0

Figure 9-14. Port J Pullup/Pulldown Select Register (PUPSJ)

Read: Anytime
Write: Anytime

Each bit in the register corresponds to a port J pin. Each bit selects a pullup or pulldown device for the associated port J pin. The pullup or pulldown is active only if enabled by the PULEJ register.

PUPSJ should be initialized before enabling the pullups/pulldowns (PUPEJ).

PUPSJ7–PUPSJ0 — Key Wakeup Port J Pullup/Pulldown Select Bits

1 = Pullup is selected for the associated port J pin.
0 = Pulldown is selected for the associated port J pin.

9.2.15 Port J Pullup/Pulldown Enable Register

Address: $002E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PULEJ7	PULEJ6	PULEJ5	PULEJ4	PULEJ3	PULEJ2	PULEJ1	PULEJ0
Reset:	0	0	0	0	0	0	0	0

Figure 9-15. Port J Pullup/Pulldown Enable Register (PULEJ)

Read: Anytime
Write: Anytime

Each bit in the register corresponds to a port J pin. If a pin is configured as an input, each bit enables an active pullup or pulldown device. PUPSJ selects whether a pullup or a pulldown is the active device.

PULEJ7–PULEJ0 — Key Wakeup Port J Pullup/Pulldown Enable Bits

1 = Selected pullup/pulldown device for the associated port J pin is enabled if it is an input.
0 = Associated port J pin has no pullup/pulldown device.

12.4.4.2 Gated Time Accumulation Mode

Setting the PAMOD bit configures the PA for gated time accumulation operation. An active level on the PAI pin enables a divided-by-64 clock to drive the PA. The PA edge bit, PEDGE, selects low levels or high levels to enable the divided-by-64 clock.

The trailing edge of the active level at the PAI pin sets the PA input flag, PAIF. The PA input interrupt enable bit, PAI, enables the PAIF flag to generate interrupt requests.

NOTE

The PAI input and timer channel 7 use the same pin. To use the PAI input, disconnect it from the output logic by clearing the channel 7 output mode and output level bits, OM7 and OL7. Also clear the channel 7 output compare mask bit, OC7M7.

The PA counter registers, TIMPACNTH/L reflect the number of pulses from the divided-by-64 clock since the last reset.

NOTE

The timer prescaler generates the divided-by-64 clock. If the timer is not active, there is no divided-by-64 clock.

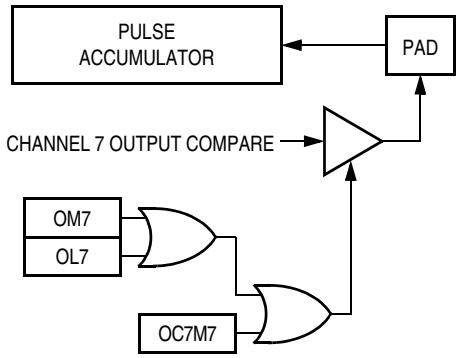


Figure 12-3. Channel 7 Output Compare/Pulse Accumulator Logic

13.3 SPI Features

Serial preipheral interface (SPI) fetures include:

- Full-duplex operation
- Master mode and slave mode
- Programmable slave-select output option
- Programmable bidirectional data pin option
- Interrupt-driven operation with two flags:
  - Transmission complete
  - Mode fault
- Read data buffer
- Serial clock with programmable polarity and phase
- Reduced drive control for lower power consumption
- Programmable open-drain output option

For additional information, refer to Chapter 15 Serial Peripheral Interface (SPI)

13.4 MSI Block Diagram

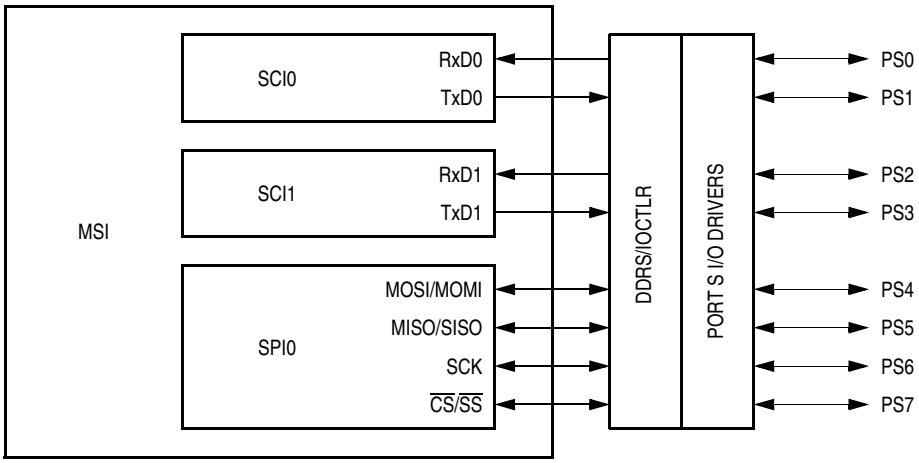


Figure 13-1. Multiple Serial Interface Block Diagram

register can accept new data from the internal data bus. If the transmit interrupt enable bit, TIE, in SCI control register 2 (SCCR2) is also set, the TDRE flag generates an SCI interrupt request.

When the transmit shift register is not transmitting a frame, the TXD pin goes to the idle condition, logic 1. If at any time software clears the TE bit in SCI control register 2 (SCCR2), the transmitter and receiver relinquish control of the port I/O pins.

If software clears TE while a transmission is in progress (TC = 0), the frame in the transmit shift register continues to shift out. Then the TXD pin reverts to being a general-purpose I/O pin even if there is data pending in the SCI data register. To avoid accidentally cutting off the last frame in a message, always wait for TDRE to go high after the last frame before clearing TE.

To separate messages with preambles with minimum idle line time, use this sequence between messages:

1. Write the last byte of the first message to SCDRH/L.
2. Wait for the TDRE flag to go high, indicating the transfer of the last frame to the transmit shift register.
3. Queue a preamble by clearing and then setting the TE bit.
4. Write the first byte of the second message to SCDRH/L.

When the SCI relinquishes the TXD pin, the PORTS and DDRS registers control the TXD pin.

To force TXD high when turning off the transmitter, set bit 1 of the port S register (PORTS) and bit 1 of the port S data direction register (DDRS). The TXD pin goes high as soon as the SCI relinquishes it.

14.5.3.3 Break Characters

Writing a logic 1 to the send break bit, SBK, in SCI control register 2 (SCCR2) loads the transmit shift register with a break character. A break character contains all logic 0s and has no start, stop, or parity bit. Break character length depends on the M bit in SCI control register 1 (SCCR1). As long as SBK is at logic 1, transmitter logic continuously loads break characters into the transmit shift register. After software clears the SBK bit, the shift register finishes transmitting the last break character and then transmits at least one logic 1. The automatic logic 1 at the end of a break character guarantees the recognition of the start bit of the next frame.

The SCI recognizes a break character when a start bit is followed by eight or nine logic 0 data bits and a logic 0 where the stop bit should be. Receiving a break character has these effects on SCI registers:

- Sets the framing error flag, FE
- Sets the receive data register full flag, RDRF
- Clears the SCI data registers, SCDRH/L
- May set the overrun flag, OR, noise flag, NF, parity error flag, PE, or the receiver active flag, RAF (see 14.6.4 SCI Status Register 1)

14.5.3.4 Idle Characters

An idle character contains all logic 1s and has no start, stop, or parity bit. Idle character length depends on the M bit in SCI control register 1 (SCCR1). The preamble is a synchronizing idle character that begins the first transmission initiated after writing the TE bit from 0 to 1.

If the TE bit is cleared during a transmission, the TXD pin becomes idle after completion of the transmission in progress. Clearing and then setting the TE bit during a transmission queues an idle character to be sent after the frame currently being transmitted.

Figure 14-10 shows the effect of noise early in the start bit time. Although this noise does not affect proper synchronization with the start bit time, it does set the noise flag.

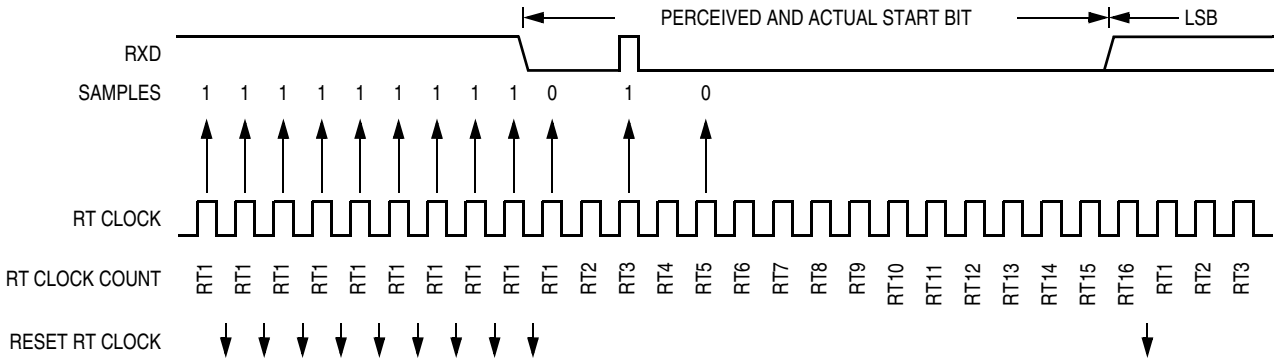


Figure 14-10. Start Bit Search Example 4

Figure 14-11 shows a burst of noise near the beginning of the start bit that resets the RT clock. The sample after the reset is low but is not preceded by three high samples that would qualify as a falling edge. Depending on the timing of the start bit search and on the data, the frame may be missed entirely or it may set the framing error flag.

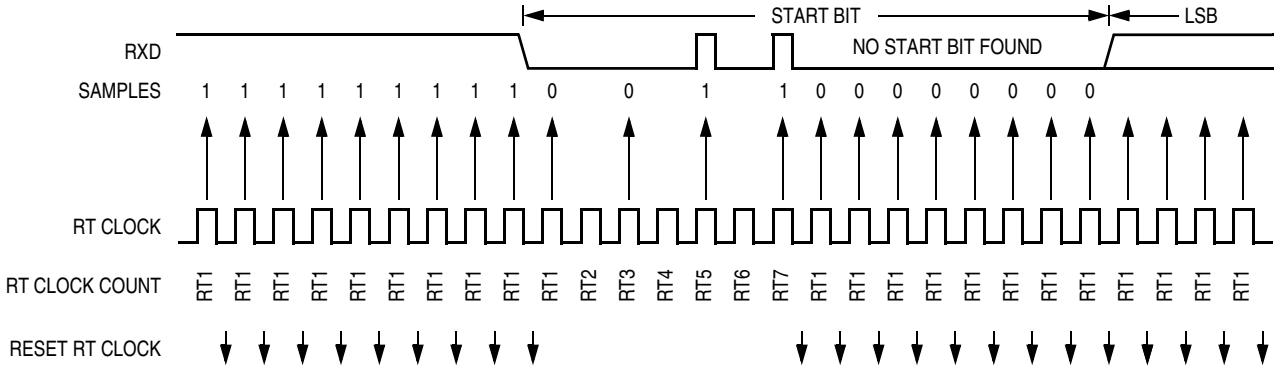


Figure 14-11. Start Bit Search Example 5

In Figure 14-12 a noise burst makes the majority of data samples RT8, RT9, and RT10 high. This sets the noise flag but does not reset the RT clock. In start bits only, the RT8, RT9, and RT10 data samples are ignored.

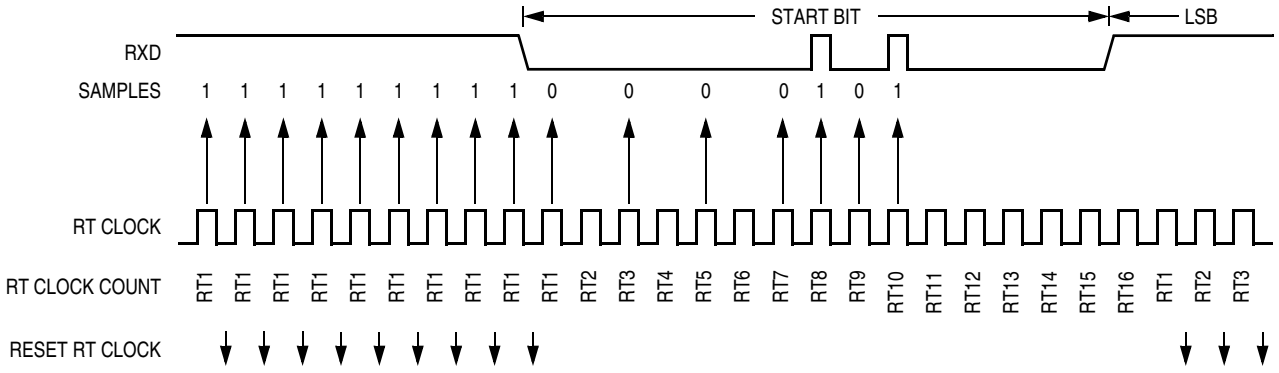


Figure 14-12. Start Bit Search Example 6

16.7.3 Stop Mode

The ATD is inactive in stop mode for reduced power consumption. The STOP instruction aborts any conversion sequence in progress.

16.8 Interrupt Sources

Table 16-5. ATD Interrupt Sources

Interrupt Source	Flag	Local Enable	CCR Mask	Vector Address
Conversion sequence complete	ASCIF	ASCIE	I bit	$FFD2, $FFD3

NOTE

The ASCIF flag is set only when a conversion sequence is completed and ASCIE = 1 or interrupts on the analog-to-digital converter (ATD) module are enabled.

16.9 General-Purpose Ports

Port AD is an input-only port. When the ATD is enabled, port AD is the analog input port for the ATD. Setting the ATD power-up bit, ADPU, in ATD control register 2 enables the ATD.

Port AD is available for general-purpose input when the ATD is disabled. Clearing the ADPU bit disables the ATD.

16.10 Port AD Data Register

Address: $006F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PAD7	PAD6	PAD5	PAD4	PAD3	PAD2	PAD1	PAD0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 16-14. Port AD Data Input Register (PORTAD)

Read: Anytime; reads return logic levels on the PAD pins
Write: Has no meaning or effect

PAD7–PAD0 — Port AD Data Input Bits

17.4.2 BDM Status Register

Address: $FF01

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ENBDM	EDMACT	ENTAG	SDV	TRACE	0	0	0
Reset:	0	0	0	0	0	0	0	0
Single-chip peripheral:	1	0	0	0	0	0	0	0

Figure 17-6. BDM Status Register (STATUS)

This register can be read or written by BDM commands or firmware.

ENBDM — Enable BDM Bit (permit active background debug mode)

1 = BDM can be made active to allow firmware commands.
0 = BDM cannot be made active (hardware commands still allowed).

BDMACT — Background Mode Active Status Bit

1 = BDM active and waiting for serial commands
0 = BDM not active

ENTAG — Instruction Tagging Enable Bit

Set by the TAGGO instruction and cleared when BDM is entered.

1 = Tagging active (BDM cannot process serial commands while tagging is active.)
0 = Tagging not enabled or BDM active

SDV — Shifter Data Valid Bit

Shows that valid data is in the serial interface shift register. Used by firmware-based instructions.

1 = Valid data
0 = No valid data

TRACE — Asserted by the TRACE1 Instruction

17.4.3 BDM Shift Register

Address: $FF02

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	S15	S14	S13	S12	S11	S10	S9	S8
Reset:	0	0	0	0	0	0	0	0

Address: $FF03

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	S7	S6	S5	S4	S3	S2	S1	S0
Reset:	0	0	0	0	0	0	0	0

Figure 17-7. BDM Shift Register (SHIFTER)

This 16-bit register contains data being received or transmitted via the serial interface.

Chapter 18
Electrical Characteristics

18.1 Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

NOTE

This device is not guaranteed to operate properly at the maximum ratings. Refer to 18.4 DC Electrical Characteristics for guaranteed operating conditions.

Rating	Symbol	Value	Unit
Supply voltage	V_{DD} V_{DDA} V_{DDX}	–0.3 to +6.5	V
Input voltage	V_{In}	–0.3 to +6.5	V
Maximum current per pin excluding V_{DD} and V_{SS}	I_{In}	± 25	mA
Storage temperature	T_{STG}	–55 to +150	°C
V_{DD} differential voltage	V_{DD}–V_{DDX}	6.5	V

NOTE

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{In} and V_{Out} be constrained to the range $V_{SS} \le (V_{In}$ or $V_{Out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}).

18.9 ATD AC Operating Characteristics

Characteristic[1]	Symbol	Min	Max	Unit
ATD operating clock frequency	f_{ATDCLK}	0.5	2.0	MHz
Conversion time per channel 0.5 MHz ≤ f_{ATDCLK} ≤ 2 MHz 18 ATD clocks 32 ATD clocks	t_{CONV}	 8.0 15.0	 32.0 60.0	µs
Stop recovery time V_{DDA} = 5.0 V	t_{SR}	—	50	µs

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, ATD clock = 2 MHz, unless otherwise noted

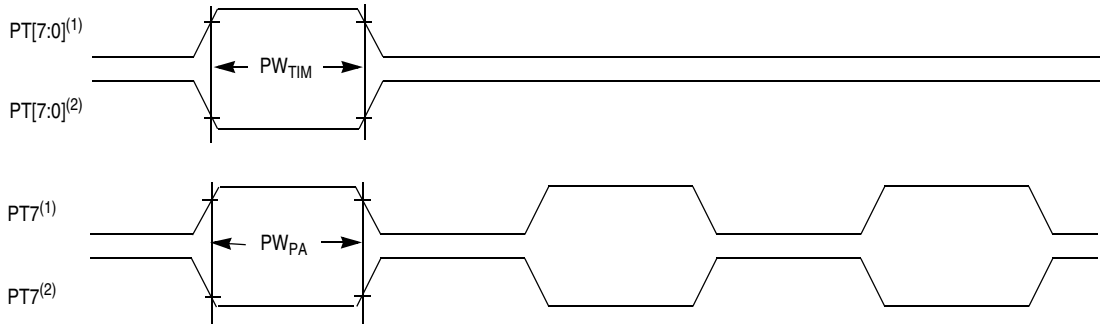
18.10 EEPROM Characteristics

Characteristic[1]	Symbol	Min	Typical	Max	Unit
Minimum programming clock frequency[2]	f_{PROG}	4.0	—	—	MHz
Programming time	t_{PROG}	10.0	—	10.5	ms
Clock recovery time following STOP, to continue programming	t_{CRSTOP}	—	—	t_{PROG}+ 1	ms
Erase time	t_{Erase}	10.0	—	10.5	ms
Write/erase endurance	—	10,000	30,000[3]	—	Cycles
Data retention	—	10	—	—	Years

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted
2. RC oscillator must be enabled if programming is desired and $f_{SYS} < f_{PROG}$.
3. If average T_H is below 85°C

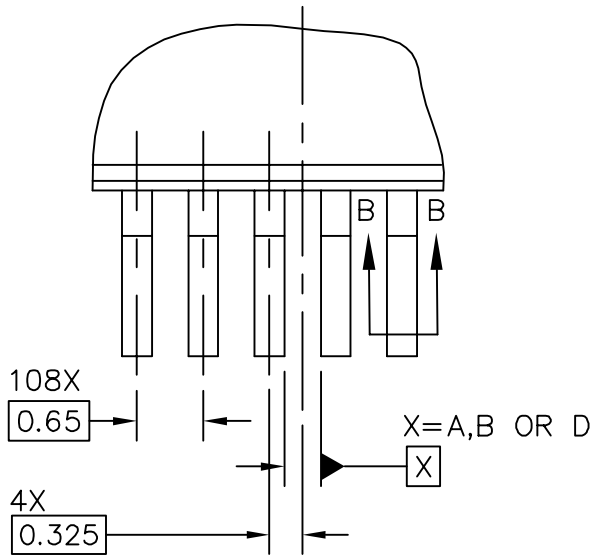
18.11 Control Timing

Characteristic	Symbol	8.0 MHz		Unit
		Min	Max	
Frequency of operation	f_o	dc	8.0	MHz
E-clock period	t_{cyc}	125	—	ns
Crystal frequency	f_{XTAL}	—	16.0	MHz
External oscillator frequency	2 f_o	dc	16.0	MHz
Processor control setup time $t_{PCSU} = t_{cyc}/2 + 30$	t_{PCSU}	82	—	ns
Reset input pulse width To guarantee external reset vector Minimum input time (can be pre-empted by internal reset)	PW_{RSTL}	32 2	— —	t_{cyc}
Mode programming setup time	t_{MPS}	4	—	t_{cyc}
Mode programming hold time	t_{MPH}	10	—	ns
Interrupt pulse width, $\overline{IRQ}$, edge-sensitive mode, KWU $PW_{IRQ} = 2\ t_{cyc} + 20$	PW_{IRQ}	270	—	ns
Wait recovery startup time	t_{WRS}	—	4	t_{cyc}
Timer pulse width, input capture pulse accumulator input $PW_{TIM} = 2\ t_{cyc} + 20$	PW_{TIM}	270	—	ns

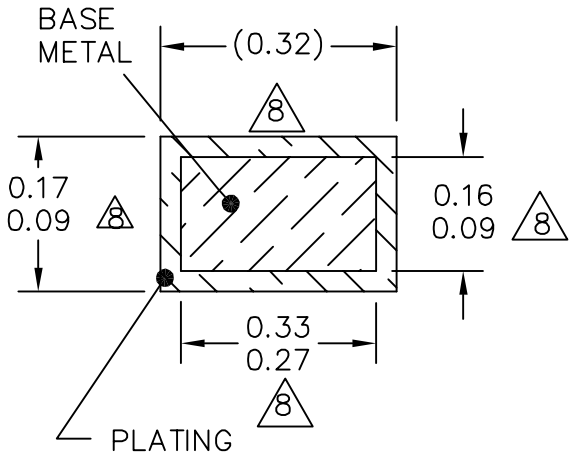


Notes:
1. Rising edge-sensitive input
2. Falling edge-sensitive input

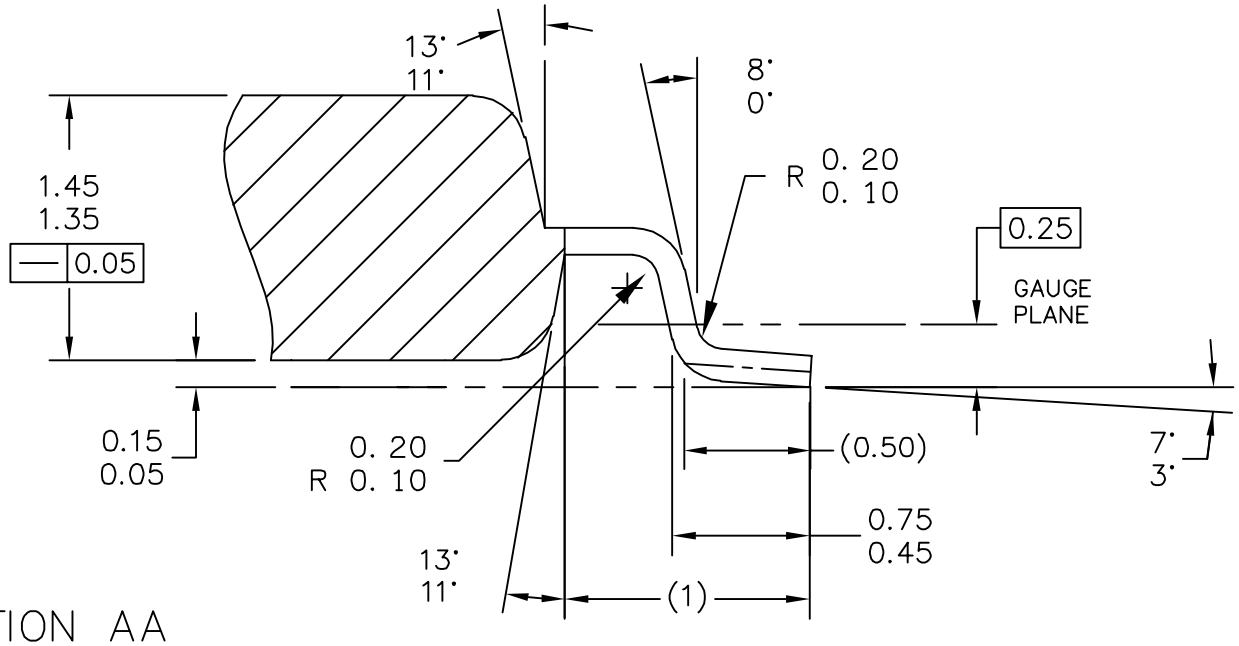
Figure 18-1. Timer Inputs



VIEW Y



SECTION B–B



SECTION AA

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASS23330W	REV: E
112LD LQFP 20 X 20 X 1.4 0.65 PITCH	CASE NUMBER: 987–02	25 MAY 2005
	STANDARD: JEDEC MS–026 BFA	