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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CPU12
Core Size	16-Bit
Speed	5MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	83
Program Memory Size	4KB (4K x 8)
Program Memory Type	EEPROM
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=xc68c812a4pve5

Revision History

Date	Revision Level	Description	Page Number(s)
August, 2001 (Continued)	4	**12.11.3 Data Direction Register for Timer Port** — Repetitive information removed. See **12.11.2 Timer Port Data Direction Register**	209
		18.12 Control Timing — Minimum values added for PW_{IRQ} and PW_{TIM}	329
		18.14 Non-Multiplexed Expansion Bus Timing — Table heading changed to reflect minimum and maximum values at 8 MHz	334
September, 2001	5	**Table 12-3. Prescaler Selection** — Added value column and updated prescale factors	197
		18.11 EEPROM Characteristics — Corrected minimum and maximum values for programming and erase times	328
August, 2002	6	**Figure 1-3. Expanded Wide Mode SRAM Expansion Schematic** — On sheet 1 of this schematic removed reference to resistor R2	40
		Figure 1-4. Expanded Narrow Mode SRAM Expansion Schematic — On sheet 1 of this schematic removed reference to resistor R2	42
		4.6.2 External Reset — Corrected reference to eight E-clock cycles to nine E-clock cycles	77
May, 2006	7	Updated to meet Freescale identity guidelines.	Throughout
		1.3 Ordering Information — Updated Table 1-1. Ordering Information and added Figure 1-1. Device Numbering System.	18
		Figure 1-4. Expanded Wide Mode SRAM Expansion Schematic (Sheet 1 of 3) — Updated sheet 1 and corrected title for sheets 2 and 3.	24
		Figure 1-5. Expanded Narrow Mode SRAM Expansion Schematic (Sheet 1 of 3) — Updated sheet 1 and corrected title for sheets 2 and 3.	26
		Figure 3-9. Condition Code Register (CCR) — Corrected reset state for bit 7.	46
		Table 4-1. Interrupt Vector Map — Corrected reference to clock monitor reset.	50
		4.5 Resets — Reworked paragraph for clarity.	52
		Figure 5-1. Mode Register (MODE) — Changed reset state designator from Peripheral to Special peripheral.	58
		Figure 10-3. Clock Function Register Map — Removed reference to Special Reset for the COP Control Register.	102
		Figure 10-9. COP Control Register (COPCTL) — Corrected reset states.	107
		12.4.1 Prescaler — Corrected number of prescaler divides.	122
		Figure 12-17. Timer Mask 2 Register (TMSK2) — Corrected reset state for bit 4.	131
		Table 16-5. ATD Interrupt Sources — Corrected table title.	207
		18.2 Functional Operating Range — Corrected operating temperature range entries.	222
		18.10 EEPROM Characteristics — Corrected minimum value for minimum programming clock frequency.	226
		18.11 Control Timing — Corrected maximum value for frequency of operation.	227
		18.12 Peripheral Port Timing — Corrected table heading.	231
		19.2 Package Dimensions — Replaced package dimension drawing with the latest available.	237

List of Chapters

Chapter 16
Analog-to-Digital Converter (ATD)

Chapter 17
Development Support

Chapter 1
General Description

1.1 Introduction

The MC68HC812A4 microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripheral modules connected by an intermodule bus. Modules include:

- 16-bit central processor unit (CPU12)
- Lite integration module (LIM)
- Two asynchronous serial communications interfaces (SCI0 and SCI1)
- Serial peripheral interface (SPI)
- Timer and pulse accumulator module
- 8-bit analog-to-digital converter (ATD)
- 1-Kbyte random-access memory (RAM)
- 4-Kbyte electrically erasable, programmable read-only memory (EEPROM)
- Memory expansion logic with chip selects, key wakeup ports, and a phase-locked loop (PLL)

1.2 Features

Features of the MC68HC812A4 include:

- Low-power, high-speed M68HC12 CPU
- Power-saving stop and wait modes
- Memory:
  - 1024-byte RAM
  - 4096-byte EEPROM
  - On-chip memory mapping allows expansion to more than 5-Mbyte address space
- Single-wire background debug mode
- Non-multiplexed address and data buses
- Seven programmable chip-selects with clock stretching (expanded modes)
- 8-channel, enhanced 16-bit timer with programmable prescaler:
  - All channels configurable as input capture or output compare
  - Flexible choice of clock source
- 16-bit pulse accumulator
- Real-time interrupt circuit
- Computer operating properly (COP) watchdog
- Clock monitor
- Phase-locked loop (PLL)

1.4 Block Diagram

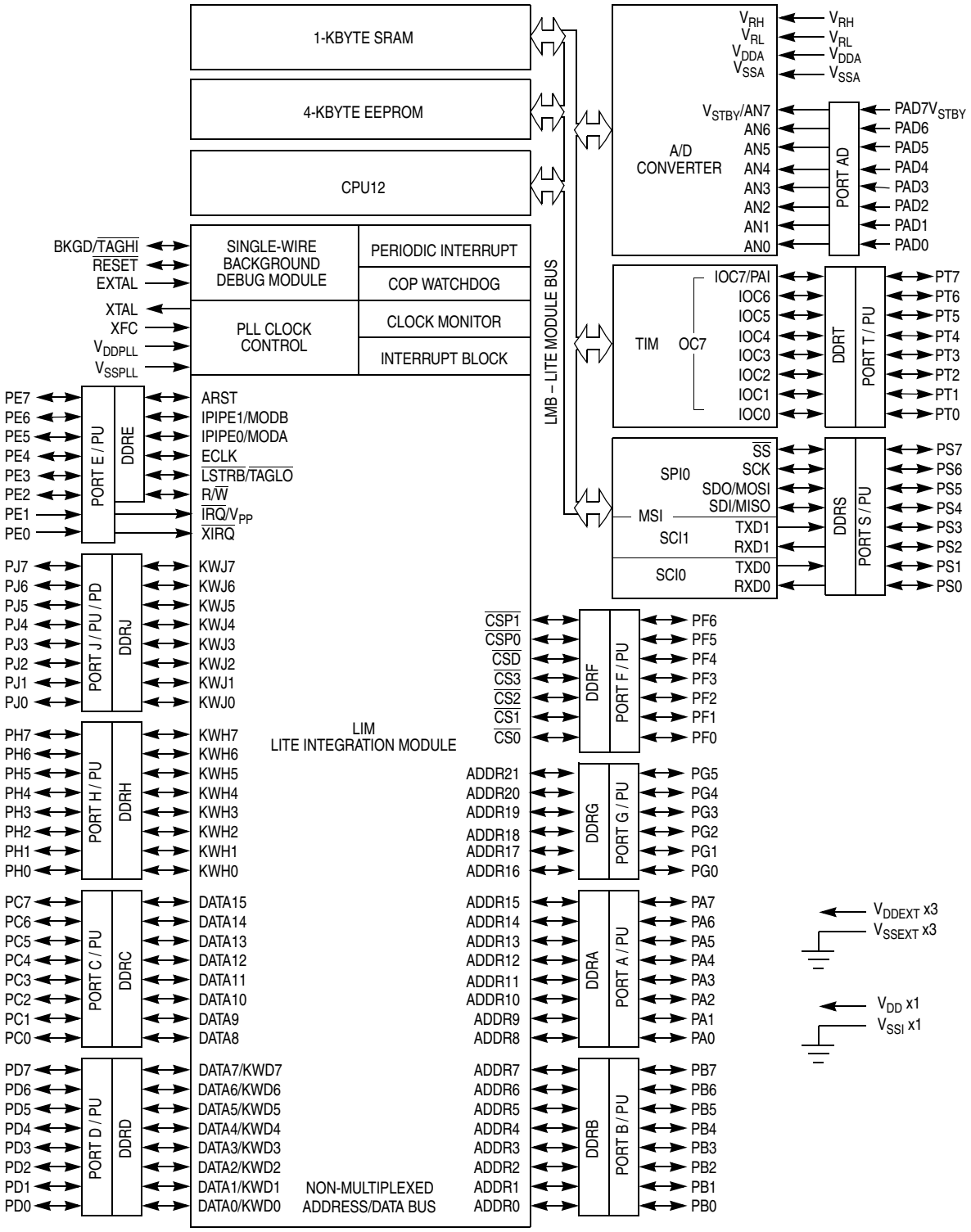


Figure 1-2. Block Diagram

1.5 Signal Descriptions

NOTE

A line over a signal name indicates an active low signal. For example, RESET is active high and $\overline{RESET}$ is active low.

The MC68HC812A4 is available in a 112-lead low-profile quad flat pack (LQFP). The pin assignments are shown in Figure 1-3. Most pins perform two or more functions, as described in Table 1-2. Individual ports are cross referenced in Table 1-3 and Table 1-4.

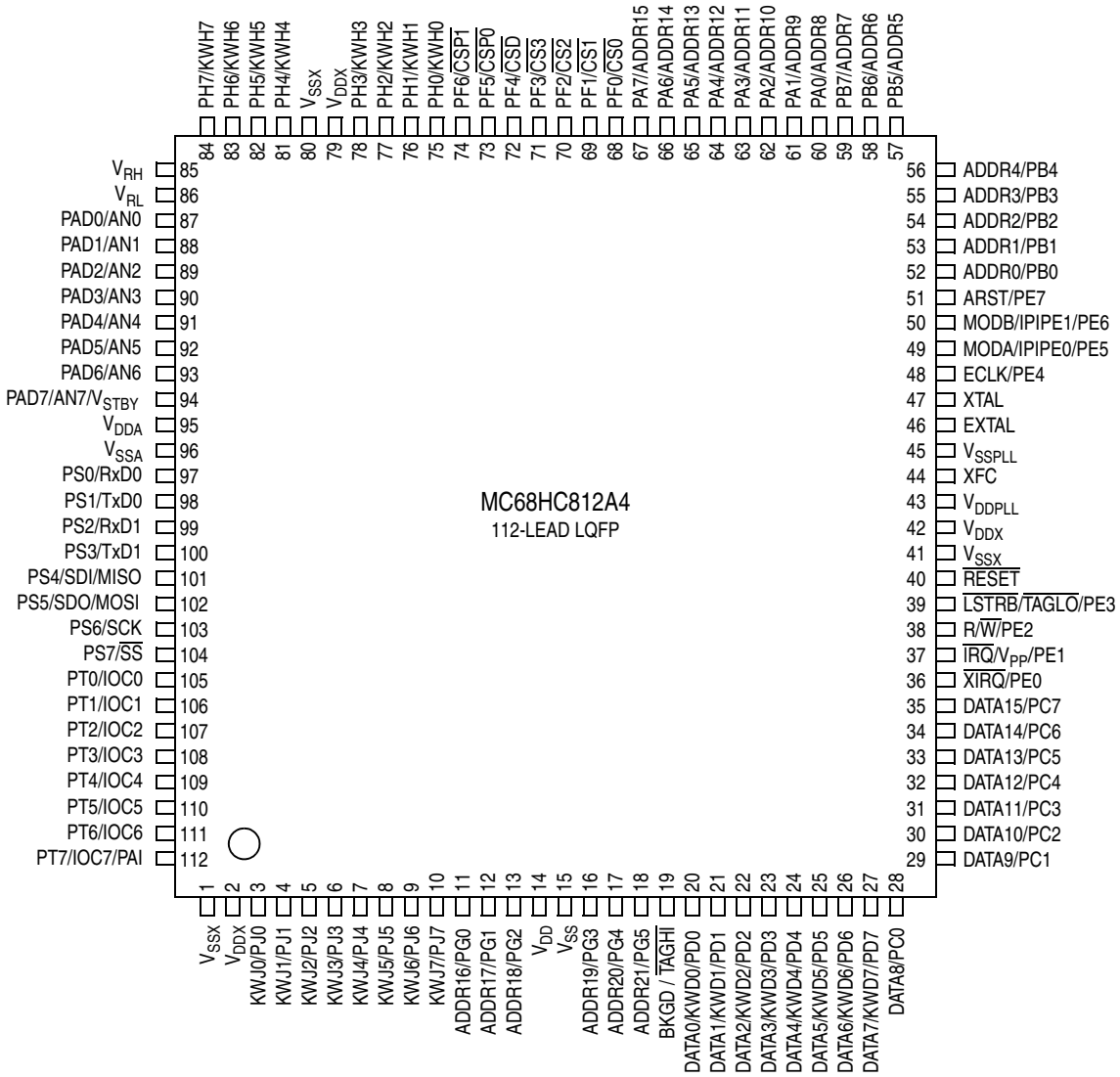


Figure 1-3. Pin Assignments

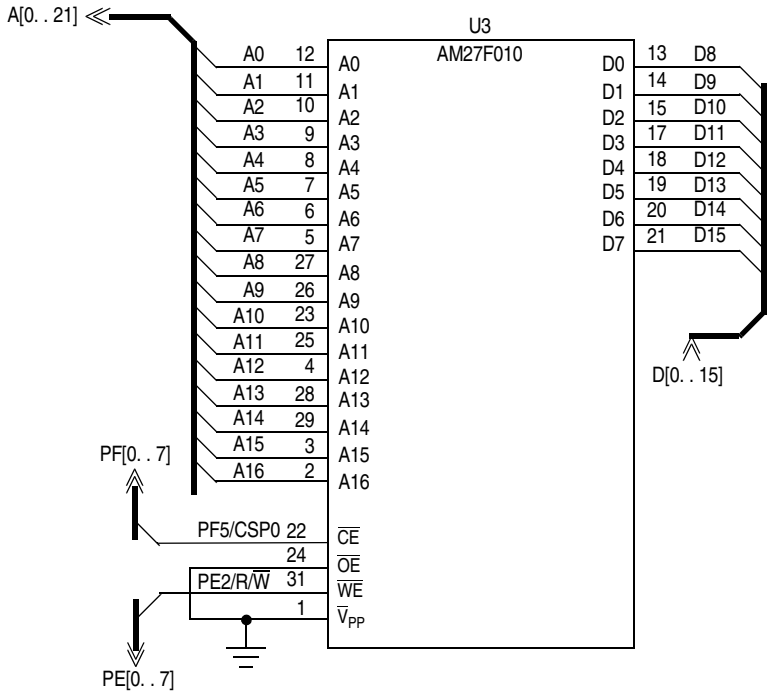


Figure 1-5. Expanded Narrow Mode SRAM Expansion Schematic (Sheet 2 of 3)

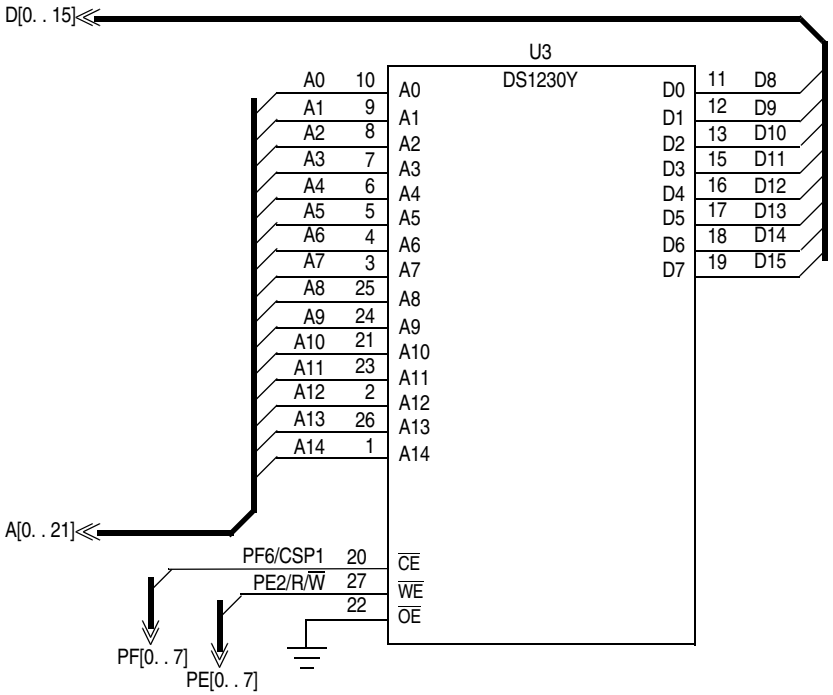


Figure 1-5. Expanded Narrow Mode SRAM Expansion Schematic (Sheet 3 of 3)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0086	Timer System Control Register (TSCR) See page 127.	Read:	TEN	TSWAI	TSBCK	TFFCA	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0087	Reserved		R	R	R	R	R	R	R	R
$0088	Timer Control Register 1 (TCTL1) See page 129.	Read:	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0089	Timer Control Register 2 (TCTL2) See page 129.	Read:	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$008A	Timer Control Register 3 (TCTL3) See page 130.	Read:	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$008B	Timer Control Register 4 (TCTL4) See page 130.	Read:	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$008C	Timer Mask Register 1 (TMSK1) See page 130.	Read:	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$008D	Timer Mask Register 2 (TMSK2) See page 131.	Read:	TOI	0	PUPT	RDPT	TCRE	PR2	PR1	PR0
		Write:								
		Reset:	0	0	1	1	0	0	0	0
$008E	Timer Flag Register 1 (TFLG1) See page 132.	Read:	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$008F	Timer Flag Register 2 (TFLG2) See page 132.	Read:	TOF	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0090	Timer Channel 0 Register High (TC0H) See page 133.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0091	Timer Channel 0 Register Low (TC0L) See page 133.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0092	Timer Channel 1 Register High (TC1H) See page 133.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Figure 2-1. Register Map (Sheet 9 of 14)

4.6 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known startup states, as follows.

4.6.1 Operating Mode and Memory Map

The states of the BGND, MODA, and MODB pins during reset determine the operating mode and default memory mapping. The SMODN, MODA, and MODB bits in the MODE register reflect the status of the mode-select inputs at the rising edge of reset. Operating mode and default maps can subsequently be changed according to strictly defined rules.

4.6.2 Clock and Watchdog Control Logic

Reset enables the COP watchdog with the CR2–CR0 bits set for the longest timeout period. The clock monitor is disabled. The RTIF flag is cleared and automatic hardware interrupts are masked. The rate control bits are cleared, and must be initialized before the RTI system is used. The DLY control bit is set to specify an oscillator startup delay upon recovery from stop mode.

4.6.3 Interrupts

Reset initializes the HPRIO register with the value $F2, causing the $\overline{\text{IRQ}}$ pin to have the highest I bit interrupt priority. The $\overline{\text{IRQ}}$ pin is configured for level-sensitive operation (for wired-OR systems). However, the I and X bits in the CCR are set, masking $\overline{\text{IRQ}}$ and $\overline{\text{XIRQ}}$ interrupt requests.

4.6.4 Parallel I/O

If the MCU comes out of reset in an expanded mode, port A and port B are the address bus. Port C and port D are the data bus. In narrow mode, port C alone is the data bus. Port E pins are normally used to control the external bus. The PEAR register affects port E pin operation.

If the MCU comes out of reset in a single-chip mode, all ports are configured as general-purpose, high-impedance inputs except in normal narrow expanded mode (NNE). In NNE, PE3 is configured as an output driven high.

In expanded modes, PF5 is an active chip-select.

4.6.5 Central Processor Unit

After reset, the CPU fetches a vector from the appropriate address and begins executing instructions. The stack pointer and other CPU registers are indeterminate immediately after reset. The CCR X and I interrupt mask bits are set to mask any interrupt requests. The S bit is also set to inhibit the STOP instruction.

4.6.6 Memory

After reset, the internal register block is located at $0000–$01FF and RAM is at $0800–$0BFF. EEPROM is located at $1000–$1FFF in expanded modes and at $F000–$FFFF in single-chip modes.

4.6.7 Other Resources

The timer, serial communications interface (SCI), serial peripheral interface (SPI), and analog-to-digital converter (ATD) are off after reset.

5.4.5 Miscellaneous Mapping Control Register

Additional mapping controls are available that can be used in conjunction with memory expansion and chip selects.

To use memory expansion, the part must be operated in one of the expanded modes. Sections of the standard 64-Kbyte memory map have memory expansion windows which allow more than 64 Kbytes to be addressed externally. Memory expansion consists of three memory expansion windows and six address lines in addition to the existing standard 16 address lines. The memory expansion function reuses as many as six of the standard 16 address lines. Usage of chip selects identifies the source of the internal address.

All of the memory expansion windows have a fixed size and two of them have a fixed address location. The third has two selectable address locations.

Address: $0013

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EWDIR	NDRC	0	0	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

Figure 5-5. Miscellaneous Mapping Control Register (MISC)

Read: Anytime
Write: Once in normal modes; anytime in special modes

EWDIR — Extra Window Positioned in Direct Space Bit

This bit is only valid in expanded modes. If the EWEN bit in the WINDEF register is cleared, then this bit has no meaning or effect.

1 = If EWEN is set, then a 1 in this bit places the EPAGE at $0000–$03FF.
0 = If EWEN is set, then a 0 in this bit places the EPAGE at $0400–$07FF.

NDRC — Narrow Data Bus for Register Chip-Select Space Bit

This function requires at least one of the chip selects CS3–CS0 to be enabled. It effects the external 512-byte memory space.

1 = Makes the register-following chip-selects (2, 1, 0, and sometimes 3) active space (512-byte block) act the same as an 8-bit only external data bus. Data only goes through port C externally. This allows 8-bit and 16-bit external memory devices to be mixed in a system.
0 = Makes the register-following chip-select active space act as a full 16-bit data bus. In the narrow (8-bit) mode, NDRC has no effect.

Port D and its associated data direction register may be removed from the on-chip map when port D is needed for 16-bit data transfers. If the MCU is in an expanded wide mode, port C and port D are used for 16-bit data and the associated port and data direction registers become external accesses. When the MCU is in expanded narrow mode, the external data bus is normally 8 bits. To allow full-speed operation while allowing visibility of internal 16-bit accesses, a 16-bit-wide data path is required. The emulate port D (EMD) control bit in the MODE register may be set to allow such 16-bit transfers. In this case of narrow special expanded mode and the EMD bit set, port D and data direction D registers are removed from the on-chip memory map and become external accesses so port D may be rebuilt externally.

In any expanded mode, port E pins may be needed for bus control (for instance, ECLK and R/$\overline{W}$). To regain the single-chip functions of port E, the emulate port E (EME) control bit in the MODE register may be set. In this special case of expanded mode and EME set, PORTE and DDRE registers are removed from the on-chip memory map and become external accesses so port E may be rebuilt externally.

6.3.1 Port A Data Register

Address: $0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Reset:	0	0	0	0	0	0	0	0
Expanded and peripheral:	ADDR15	ADDR14	ADDR13	ADDR12	ADDR11	ADDR10	ADDR9	ADDR8

Figure 6-1. Port A Data Register (PORTA)

Read: Anytime, if register is in the map
Write: Anytime, if register is in the map

Bits PA7–PA0 are associated with addresses ADDR15–ADDR8 respectively. When this port is not used for external addresses such as in single-chip mode, these pins can be used as general-purpose I/O. DDRA determines the primary direction of each pin. This register is not in the on-chip map in expanded and peripheral modes.

6.3.2 Port A Data Direction Register

Address: $0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Reset:	0	0	0	0	0	0	0	0

Figure 6-2. Port A Data Direction Register (DDRA)

Read: Anytime, if register is in the map
Write: Anytime, if register is in the map

This register determines the primary direction for each port A pin when functioning as a general-purpose I/O port. DDRA is not in the on-chip map in expanded and peripheral modes.

1 = Associated pin is an output.
0 = Associated pin is a high-impedance input.

TSWAI — Timer Stop in Wait Mode Bit

TSWAI disables the timer and PA in wait mode.

1 = Timer and PA disabled in wait mode
0 = Timer and PA enabled in wait mode

NOTE

If timer and PA interrupt requests are needed to bring the MCU out of wait mode, clear TSWAI before executing the WAIT instruction.

TSBCK — Timer Stop in Background Mode Bit

TSBCK stops the timer during background mode.

1 = Timer disabled in background mode
0 = Timer enabled in background mode

NOTE

Setting TSBCK does not stop the PA when it is in event counter mode.

TFFCA — Timer Fast Flag Clear-All Bit

When TFFCA is set:

- An input capture read or a write to an output compare channel clears the corresponding channel flag, CnF.
- Any access of the timer counter registers, TCNTH/L, clears the TOF flag.
- Any access of the PA counter registers, PACNTH/L, clears both the PAOVF and PAIF flags in the PAFLG register.

When TFFCA is clear, writing logic 1s to the flags clears them.

1 = Fast flag clearing
0 = Normal flag clearing

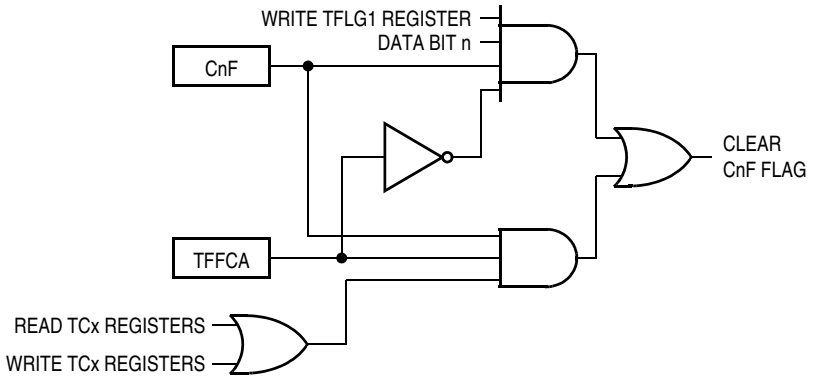


Figure 12-11. Fast Clear Flag Logic

Table 12-3. Prescaler Selection (Continued)

Value	PR[2:1:0]	Prescaler Divisor
5	101	32
6	110	32
7	111	32

NOTE

The newly selected prescale divisor does not take effect until the next synchronized edge when all prescale counter stages equal 0.

12.5.11 Timer Flag Register 1

Address: $008E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
Reset:	0	0	0	0	0	0	0	0

Figure 12-18. Timer Flag Register 1 (TFLG1)

Read: Anytime
Write: Anytime; writing 1 clears flag; writing 0 has no effect

C7F–C0F — Channel Flags

These flags are set when an input capture or output compare occurs on the corresponding channel. Clear a channel flag by writing a 1 to it.

NOTE

When the fast flag clear-all bit, TFFCA, is set, an input capture read or an output compare write clears the corresponding channel flag. TFFCA is in the timer system control register (TSCR).

12.5.12 Timer Flag Register 2

Address: $008F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-19. Timer Flag Register 2 (TFLG2)

Read: Anytime
Write: Anytime; writing 1 clears flag; writing 0 has no effect

register can accept new data from the internal data bus. If the transmit interrupt enable bit, TIE, in SCI control register 2 (SCCR2) is also set, the TDRE flag generates an SCI interrupt request.

When the transmit shift register is not transmitting a frame, the TXD pin goes to the idle condition, logic 1. If at any time software clears the TE bit in SCI control register 2 (SCCR2), the transmitter and receiver relinquish control of the port I/O pins.

If software clears TE while a transmission is in progress (TC = 0), the frame in the transmit shift register continues to shift out. Then the TXD pin reverts to being a general-purpose I/O pin even if there is data pending in the SCI data register. To avoid accidentally cutting off the last frame in a message, always wait for TDRE to go high after the last frame before clearing TE.

To separate messages with preambles with minimum idle line time, use this sequence between messages:

1. Write the last byte of the first message to SCDRH/L.
2. Wait for the TDRE flag to go high, indicating the transfer of the last frame to the transmit shift register.
3. Queue a preamble by clearing and then setting the TE bit.
4. Write the first byte of the second message to SCDRH/L.

When the SCI relinquishes the TXD pin, the PORTS and DDRS registers control the TXD pin.

To force TXD high when turning off the transmitter, set bit 1 of the port S register (PORTS) and bit 1 of the port S data direction register (DDRS). The TXD pin goes high as soon as the SCI relinquishes it.

14.5.3.3 Break Characters

Writing a logic 1 to the send break bit, SBK, in SCI control register 2 (SCCR2) loads the transmit shift register with a break character. A break character contains all logic 0s and has no start, stop, or parity bit. Break character length depends on the M bit in SCI control register 1 (SCCR1). As long as SBK is at logic 1, transmitter logic continuously loads break characters into the transmit shift register. After software clears the SBK bit, the shift register finishes transmitting the last break character and then transmits at least one logic 1. The automatic logic 1 at the end of a break character guarantees the recognition of the start bit of the next frame.

The SCI recognizes a break character when a start bit is followed by eight or nine logic 0 data bits and a logic 0 where the stop bit should be. Receiving a break character has these effects on SCI registers:

- Sets the framing error flag, FE
- Sets the receive data register full flag, RDRF
- Clears the SCI data registers, SCDRH/L
- May set the overrun flag, OR, noise flag, NF, parity error flag, PE, or the receiver active flag, RAF (see 14.6.4 SCI Status Register 1)

14.5.3.4 Idle Characters

An idle character contains all logic 1s and has no start, stop, or parity bit. Idle character length depends on the M bit in SCI control register 1 (SCCR1). The preamble is a synchronizing idle character that begins the first transmission initiated after writing the TE bit from 0 to 1.

If the TE bit is cleared during a transmission, the TXD pin becomes idle after completion of the transmission in progress. Clearing and then setting the TE bit during a transmission queues an idle character to be sent after the frame currently being transmitted.

15.9 Interrupt Sources

Table 15-4. SPI Interrupt Sources

Interrupt Source	Flag	Local Enable	CCR Mask	Vector Address
Transmission complete	SPIF	SPIE	I bit	$FFD8, $FFD9
Mode fault	MODF			

15.10 General-Purpose I/O Ports

Port S shares its pins with the multiple serial interface (MSI). In all modes, port S pins PS7–PS0 are available for either general-purpose I/O or for SCI and SPI functions. See Chapter 13 Multiple Serial Interface (MSI).

15.11 Synchronous Character Transmission Using the SPI

This program is intended to communicate with the HC11 on the UDLP1 board. It utilizes the SPI to transmit synchronously characters in a string to be displayed on the LCD display. The program must configure the SPI as a master, and non-interrupt driven. The slave peripheral is chip-selected with the $\overline{SS}$ line at low voltage level. Between 8 bit transfers the $\overline{SS}$ line is held high. Also the clock idles low and takes data on the rising clock edges. The serial clock is set not to exceed 100 kHz baud rate.

15.11.1 Equipment

For this exercise, use the M68HC812A4EVB emulation board.

15.11.2 Code Listing

NOTE

A comment line is delimited by a semicolon. If there is no code before comment, a semicolon (;) must be placed in the first column to avoid assembly errors.

```
INCLUDE 'EQUATES.ASM'      ;Equates for all registers

; User Variables

; Bit Equates

; ---------------------------------------------------------------------
;           MAIN PROGRAM
; ---------------------------------------------------------------------
        ORG    $7000            ; 16K On-Board RAM, User code data area,
;                               ; start main program at $7000
MAIN:
        BSR    INIT             ; Subroutine to initialize SPI registers
        BSR    TRANSMIT         ; Subroutine to start transmission
FINISH:
        BRA    FINIS            ; Finished transmitting all DATA
```

16.6.9 ATD Result Registers

Address: ADR0H: $0070
ADR1H: $0072
ADR2H: $0074
ADR3H: $0076
ADR4H: $0078
ADR5H: $007A
ADR6H: $007C
ADR7H: $007E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	ADRxH7	ADRxH6	ADRxH5	ADRxH4	ADRxH3	ADRxH2	ADRxH1	ADRxH0
Write:								
Reset:	Indeterminate							

= Unimplemented

Figure 16-13. ATD Result Registers (ADR0H–ADR7H)

Read: Anytime
Write: Has no meaning or effect

ADRxH7–ADRxH0 — ATD Conversion Result Bits

These bits contain the left justified, unsigned result from the ATD conversion. The channel from which this result was obtained depends on the conversion mode selected. These registers are always read-only in normal mode.

16.7 Low-Power Options

This section describes the three low-power modes:

- Run mode
- Wait mode
- Stop mode

16.7.1 Run Mode

Clearing the ATD power-up bit, ADPU, in ATD control register 2 (ATDCTL2) reduces power consumption in run mode. ATD registers are still accessible, but the clock to the ATD is disabled and ATD analog circuits are powered down.

16.7.2 Wait Mode

ATD operation in wait mode depends on the state of the ATD stop in wait bit, AWAI, in ATD control register 2 (ATDCTL2).

- If AWAI is clear, the ATD operates normally when the CPU is in wait mode
- If AWAI is set, the ATD clock is disabled and conversion continues unless ASWAI bit in ATDCTL2 register is set.

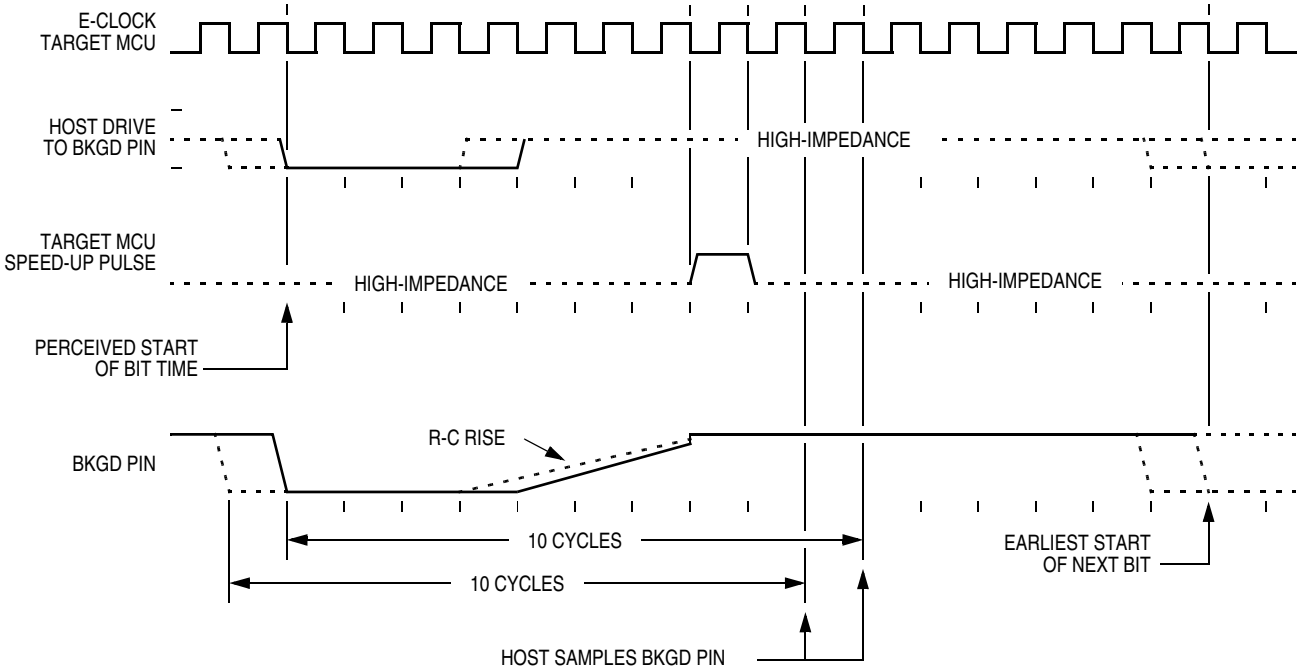


Figure 17-2. BDM Target-to-Host Serial Bit Timing (Logic 1)

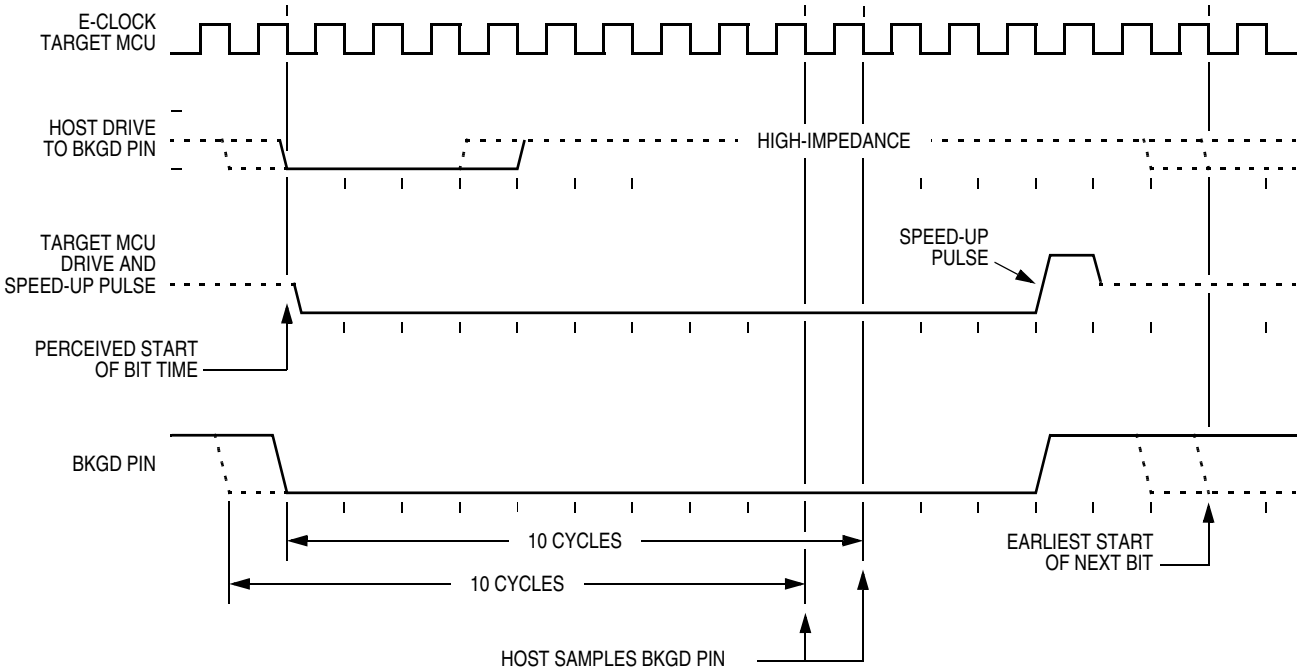


Figure 17-3. BDM Target-to-Host Serial Bit Timing (Logic 0)

Chapter 18
Electrical Characteristics

18.1 Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

NOTE

This device is not guaranteed to operate properly at the maximum ratings. Refer to 18.4 DC Electrical Characteristics for guaranteed operating conditions.

Rating	Symbol	Value	Unit
Supply voltage	V_{DD} V_{DDA} V_{DDX}	–0.3 to +6.5	V
Input voltage	V_{In}	–0.3 to +6.5	V
Maximum current per pin excluding V_{DD} and V_{SS}	I_{In}	± 25	mA
Storage temperature	T_{STG}	–55 to +150	°C
V_{DD} differential voltage	V_{DD}–V_{DDX}	6.5	V

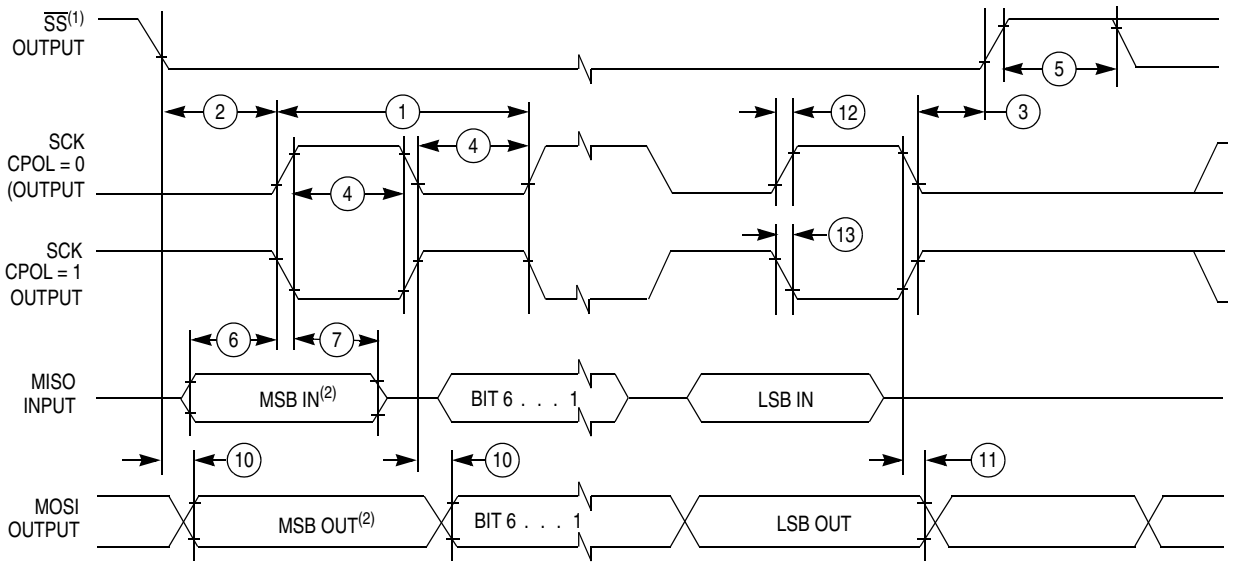
NOTE

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{In} and V_{Out} be constrained to the range $V_{SS} \le (V_{In}$ or $V_{Out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}).

18.14 SPI Timing

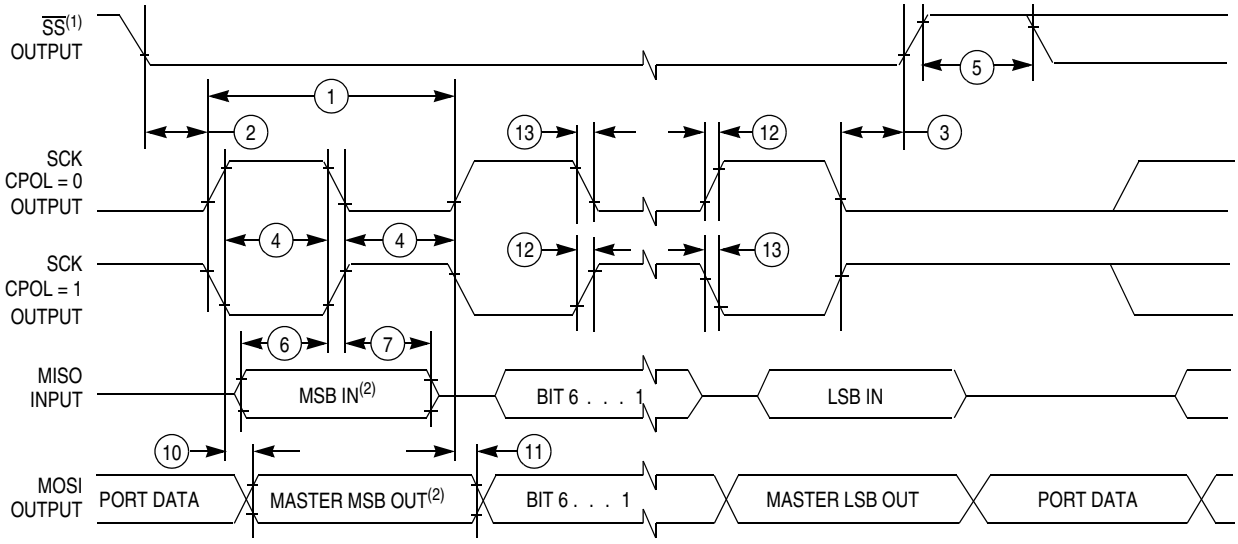
Num	Function(1), (2)	Symbol	Min	Max	Unit
	Operating frequency Master Slave	f_{op}	 dc dc	 1/2 1/2	E-clock frequency
1	SCK period Master Slave	t_{sck}	 2 2	 256 —	t_{cyc}
2	Enable lead time Master Slave	t_{Lead}	 1/2 1	 — —	 t_{sck} t_{cyc}
3	Enable lag time Master Slave	t_{Lag}	 1/2 1	 — —	 t_{sck} t_{cyc}
4	Clock (SCK) high or low time Master Slave	t_{wsck}	 t_{cyc} – 60 t_{cyc} – 30	 128 t_{cyc} —	ns
5	Sequential transfer delay Master Slave	t_{td}	 1/2 1	 — —	 t_{sck} t_{cyc}
6	Data setup time (inputs) Master Slave	t_{su}	 30 30	 — —	ns
7	Data hold time (inputs) Master Slave	t_{hi}	 0 30	 — —	ns
8	Slave access time	t_a	—	1	t_{cyc}
9	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
10	Data valid (after SCK edge) Master Slave	t_v	 — —	 50 50	ns
11	Data hold time (outputs) Master Slave	t_{ho}	 0 0	 — —	ns
12	Rise time Input Output	 t_{ri} t_{ro}	 — —	 t_{cyc} – 30 30	 ns ns
13	Fall time Input Output	 t_{fi} t_{fo}	 — —	 t_{cyc} – 30 30	 ns ns

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, 200 pF load on all SPI pins
2. All ac timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels, unless otherwise noted.



Notes:
1. SS output mode (DDS7 = 1, SSOE = 1)
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB

A) SPI Master Timing (CPHA = 0)



Notes:
1. SS output mode (DDS7 = 1, SSOE = 1)
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB

B) SPI Master Timing (CPHA = 1)

Figure 18-9. SPI Timing Diagram (Sheet 1 of 2)