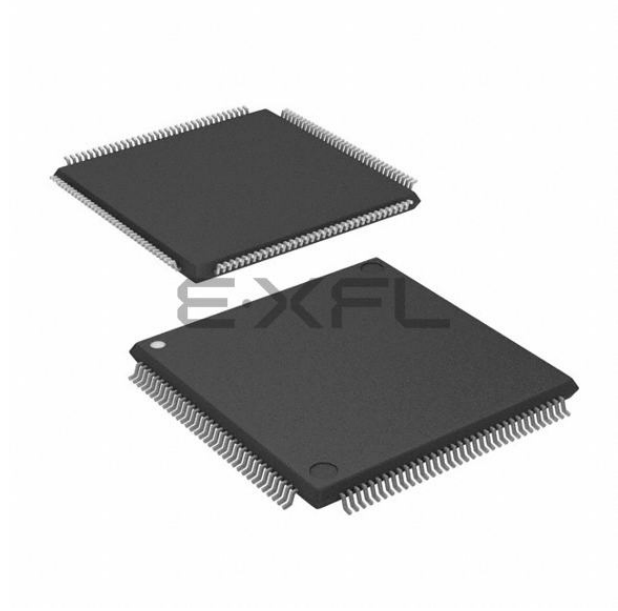

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	-
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 10K Logic Modules
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s010s-tq144

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Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 25.0

Name change from native SerDes interface to native EPCS SerDes interface in the High-Speed Serial Interfaces, page 25 was updated in revision 25.0.

1.2 Revision 24.0

Following was a summary of changes made in revision 24.0:

- Updated Table 1, page 9 for Automotive grade 2 (SAR 80232).
- Added a note on Automotive grade 2 in the I/Os Per Package, page 10 (SAR 80232)
- Added Automotive grade 2 information in the SmartFusion2 Ordering Information, page 14 (SAR 80232)

1.3 Revision 23.0

Updated Table 1, page 9 with more footnotes. (SAR 66079, SAR 77444, and SAR 73335).

1.4 Revision 22.0

Following was a summary of changes made in revision 22.0:

- Updated Table 1, page 9 (SAR 71992).
- Updated Marking Specification Details, page 16 (SAR 71992).
- Updated Low Power, page 21 (SAR 71992).
- Updated Table 11, page 27 (SAR 71992).

1.5 Revision 21.0

Following was a summary of changes made in revision 21.0:

- Updated Table 3, page 10
- Added Table 6, page 13, Table 7, page 15, Table 8, page 15
- Updated Marking Specification Details, page 16
- Updated Table 11, page 27

1.6 Revision 20.0

Following was a summary of changes made in revision 20.0:

- Updated Table 1, page 9, Table 3, page 10, Table 4, page 11, Table 5, page 12, and Table 10, page 20
- Updated SmartFusion2 Ordering Information, page 14
- Updated Marking Specification Details, page 16
- Updated Table 9, page 19, Table , page 20
- Updated SmartFusion2 Development Tools, page 26

1.7 Revision 19.0

Following was a summary of changes made in revision 19.0:

- Updated Table 1, page 9, Table 3, page 10, Table 4, page 11, Table 5, page 12, and Table 10, page 20
- Removed all instances of and references to M2S100. VQ144 is replaced with TQ144 (SAR 62858).
- Updated SmartFusion2 Ordering Information, page 14
- Updated Table 9, page 19 and Table 10, page 20

- Updated Table 11, page 27

1.8 Revision 18.0

Following was a summary of changes made in revision 18.0:

- Ordering information added to Table 2, page 10 and Table 3, page 10 for the M2S090(T) device in the FCS/FCSG325 package.
- Trademark changed to the Register mark for ARM Cortex-M3.

1.9 Revision 17.0

Updated Device Packages 005-VF256 and 150-FCS536 in Table 2, page 10 and Table 5, page 12.

1.10 Revision 16.0

Updated Table 3, page 10, Table 4, page 11, and Table 5, page 12.

1.11 Revision 15.0

Following was a summary of changes made in revision 15.0:

- Table 1, page 9 to Table 10, page 20 and SmartFusion2 Ordering Information, page 14 were updated with Military device data.
- Table 10, page 20 and the Marking Specification Details, page 16 were added.

1.12 Revision 14.0

Following was a summary of changes made in revision 14.0:

- Tables 3-6 were combined into Table 4, page 11.
- Fabric Interface Controller features were added to Table 1, page 9.
- Packages VQ144 and FCV484 were added to Table 2, page 10 and Table 4, page 11.

1.13 Revision 13.0

Following was a summary of changes made in revision 13.0:

- Data Security Feature sections and Device Status table were removed.
- Figure 1, page 8 was updated.

1.14 Revision 12.0

Following was a summary of changes made in revision 12.0:

- Packages FCS325 and VF256 were added to Table 2, page 10.
- SmartFusion2 Ordering Information, page 14 was updated.
- Typo fixed on Figure 1, page 8.

1.15 Revision 11.0

Following was a summary of changes made in revision 11.0:

- LSRAM x32/36 widths added. In Table 1, page 9, notes are added referring to updates in Table 3, page 10 –Table 5, page 12 and Table 6.
- SmartFusion2 Ordering Information, page 14 was updated. Part Numbers (tables 7 and 8) were removed. SmartFusion2 Device Status, page 16 was updated.
- M2S090-FG676 and M2S005-VF400 package pinouts finalized.

1.16 Revision 10.0

M2S005-FG484 package pinout I/O count finalized. Typos were corrected.

- The phrase, with 16-bit PIPE interface (Gen1/Gen2), was removed from the PCIe bullet in the High-Speed Serial Interfaces, page 25 (SAR 43851).
- In Table 1, page 9, PCIe Endpoint x4 was corrected to PCIe Endpoint ×1, ×2, ×4 (SAR 43851).
- The number of I/Os for M2S025 in the FG484 package was corrected from 267 to 289 in Table 2, page 10 and Table 3, page 10 (SAR 42618).
- The Y security designator was removed from SmartFusion2 Ordering Information (SAR 42231).
- The SGMII PHY Interface, page 24 was revised to change from allocating one of the high-speed serial channels to SGMII and by implementing custom logic in the fabric to allocating one of the high-speed serial channels to and utilizing the CoreTBI soft IP block (SAR 43851).
- The PCI Express, page 25 was corrected to state the SmartFusion2 family has up to four high-speed serial interface blocks rather than two. The following bullets were removed (SAR 43851):
  - Intel's PIPE interface (8-bit/16-bit) to interface between the PHY MAC and PHY (SerDes)
  - Fully compliant PHY PCS sub-layer (125/250 MHz)
- Support for SDRAM memories was removed from the High-Speed Memory Interfaces: DDRx Memory Controllers , page 25 (SAR 42594). The text was corrected to state there are up to three, rather than two, DDR subsystems (SAR 43851).
- The MDDR Subsystem, page 26 was revised to explain that support for 3.3 V Single Data Rate DRAMs (SDRAM) can be obtained by using the SMC_FIC interface (SAR 42594).
- The FDDR Subsystem, page 26 was revised to remove the statement that the APB configuration bus can be mastered by the MSS directly (SAR 42594).
- The SmartFusion2 Development Tools, page 26chapter was revised to indicate that Libero SoC includes SoftConsole (GNU/Eclipse) (SAR 41972).

1.23 Revision 3.0

Following was a summary of changes made in revision 3.0:

- Figure 1, page 8 was updated.
- Table 7, page 15 was added.

1.24 Revision 2.0

Information was updated based on ongoing development of specifications.

1.25 Revision 1.0

Information was reorganized and updated based on ongoing development of specifications.

2.1.7 High-Speed Serial Interfaces

- Up to 16 SerDes lanes, each supporting
  - XGXS/XAUI extension (to implement a 10 Gbps (XGMII) Ethernet PHY interface)
  - Native EPCS SerDes interface facilitates implementation of serial rapidIO (SRIO) in fabric or an SGMII interface to the Ethernet MAC in MSS
- PCI express (PCIe) endpoint controller
  - ×1, ×2, and ×4 lane PCI express core
  - Up to 2 Kbytes maximum payload size
  - 64-Bit/32-Bit AXI and 64-Bit/32-Bit AHB master and slave interfaces to the application layer

2.1.8 High-Speed Memory Interfaces

- Up to 2 high-speed DDRx memory controllers
  - MSS DDR (MDDR) and fabric DDR (FDDR) controllers
  - Supports LPDDR/DDR2/DDR3
  - Maximum 333 MHz DDR clock rate
  - SECDED enable/disable feature
  - Supports various DRAM bus width modes, ×8, ×9, ×16, ×18, ×32, ×36
  - Supports command reordering to optimize memory efficiency
  - Supports data reordering, returning critical word first for each command
- SDRAM support through the SMC_FIC and additional soft SDRAM memory controller

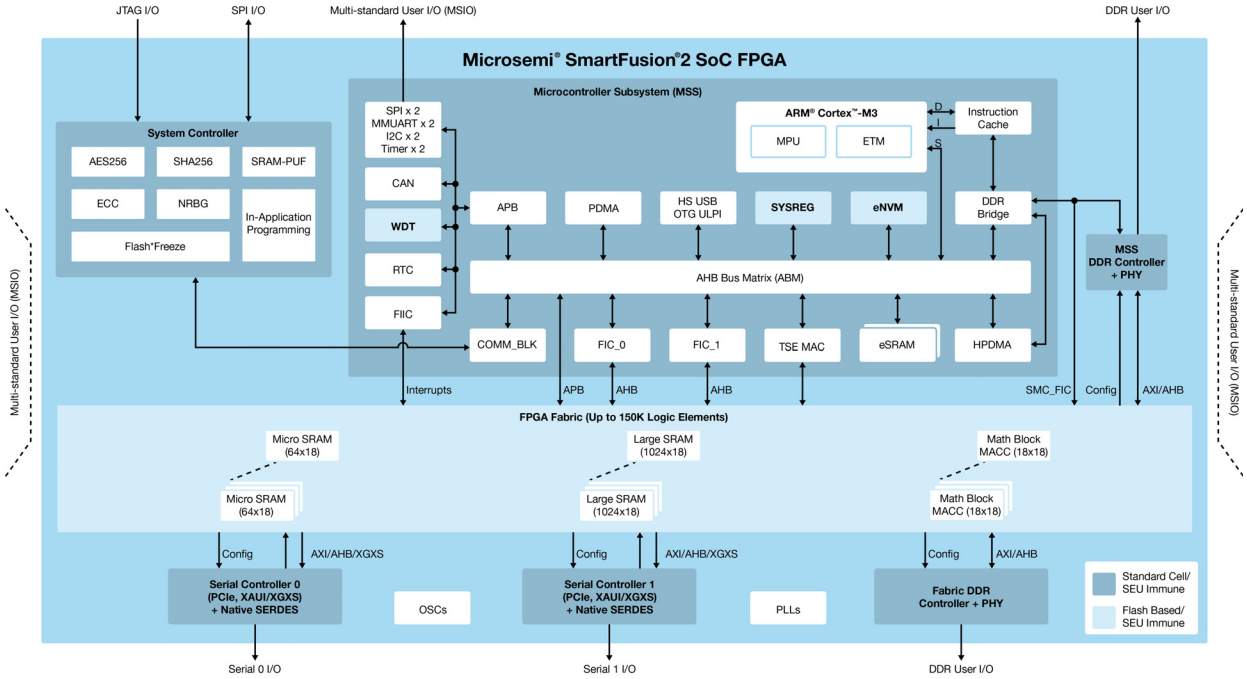
2.1.9 Operating Voltage and I/Os

- 1.2 V core voltage
- Multi-standard user I/Os (MSIO/MSIOD)
  - LVTTL/LVCMOS 3.3 V (MSIO Only)
  - LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V
  - DDR (SSTL2_1, SSTL2_2)
  - LVDS, MLVDS, Mini-LVDS, RSDS differential standards
  - PCI
  - LVPECL (receiver only)
- DDR I/Os (DDRIO)
  - DDR2, DDR3, LPDDR, SSTL2, SSTL18, HSTL
  - LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V
- Market leading number of user I/Os with 5G SerDes

2.2 SmartFusion2 SoC FPGA Block Diagram

The following figure shows the various available blocks in SmartFusion2 such as MSS, system controller, FPGA fabric LEs, and user I/Os.

Figure 1 • **SmartFusion2 Block Diagram**



The following table lists features and devices that are supported in the SmartFusion2 SoC FPGA family.

Table 1 • **SmartFusion2 SoC FPGA Product Family [1, 2]**

Peripherals	Features	M2S005 (S)	M2S010 (S/T/TS)	M2S025 (T/TS)	M2S050 (T/TS)	M2S060 (T/TS)	M2S090 (T/TS)	M2S150 (T/TS)
Logic/DSP	Maximum Logic Elements (4 LUT + DFF)[3]	6,060	12,084	27,696	56,340	56,520	86,184	146,124
	Mathblocks (18 × 18)	11	22	34	72	72	84	240
	Fabric Interface Controllers	1	1	1	2	1	1	2
	PLLs and CCCs	2	2	6	6	6	6	8
	Data Security	AES256, SHA256, and RNG	AES256, SHA256, and RNG	AES256, SHA256, and RNG	AES256, SHA256, and RNG	AES256, SHA256, RNG, ECC, and PUF	AES256, SHA256, RNG, ECC, and PUF	AES256, SHA256, RNG, ECC, and PUF
MSS	Cortex-M3 + Instruction Cache	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	eNVM (K Bytes)	128	256	256	256	256	512	512
	eSRAM (K Bytes)	64	64	64	64	64	64	64
	eSRAM (K Bytes) Non SECDED	80	80	80	80	80	80	80
	CAN, 10/100/1000 Ethernet, HS USB	1 each	1 each	1 each	1 each	1 each	1 each	1 each
	Multi-Mode UART, SPI, I^2C, Timer	2 each	2 each	2 each	2 each	2 each	2 each	2 each
Fabric Memory	LSRAM 18 K Blocks	10	21	31	69	69	109	236
	uSRAM 1 K Blocks	11	22	34	72	72	112	240
	Total RAM (K bits)	191	400	592	1314	1314	2074	4488
High Speed	DDR Controllers (Count x Width)	1 × 18	1 × 18	1 × 18	2 × 36	1 × 18	1 × 18	2 × 36
	SerDes Lanes (T)	0	4	4	8	4	4	16
	PCIe End Points	0	1	1	2	2	2	4
User I/Os	MSIO (3.3 V)	119	123	157	139	271	309	292
	MSIOD (2.5 V)	28	40	40	62	40	40	106
	DDRIO (2.5 V)	66	70	70	176	76	76	176
	Total User I/Os	209	233	267	377	387	425	574
Grades	Commercial (C), Industrial (I), Military (M), and Automotive (T2)	C, I, T2	C, I, M, T2	C, I, M, T2	C, I, M, T2	C, I, M, T2	C, I, M, T2	C, I, M

1. *Feature availability is package dependent.*
2. *Data security features are only available in S and TS devices.*

3. *Total logic may vary based on utilization of DSP and memories in the design. See UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide for details.*

2.3 I/Os Per Package

The following tables list the package options and I/Os per package.

Table 2 • **Package Options**

Packages[1]	Pitch (mm)	Length × Width (mm)
FCS(G)325[2]	0.5	11 × 11
VF(G)256[1, 3]	0.8	14 × 14
FCS(G)536[1]	0.5	16 × 16
VF(G)400[1, 2]	0.8	17 × 17
FCV(G)484[1, 2]	0.8	19 × 19
TQ(G)144[1, 4]	0.5	20 × 20
FG(G)484[1]	1.0	23 × 23
FG(G)676[1, 2]	1.0	27 × 27
FG(G)896[1]	1.0	31 × 31
FC(G)1152[1]	1.0	35 × 35

1. All the packages mentioned above are available with lead and lead free.
2. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.
3. Automotive T2 grade devices are only available in the VF(G)256, VF(G)400, FG(G)484, and FG(G)676 packages.
4. The TQ(G)144 package will be available in T2 grade by end of February, 2017.

Table 3 • **I/Os per Package**

Packages		M2S005 (S)	M2S010 (S/T/TS)[1,2]	M2S025 (T/TS)[1]	M2S050 (T/TS)[1]	M2S060 (T/TS)[1]	M2S090 (T/TS)[1, 3, 4]	M2S150 (T/TS)[5]
FCS(G)325	I/Os			180	200	200	180	
	Lanes			2	2	2	4	
VF(G)256	I/Os	161	138	138				
	Lanes		2	2				
FCS(G)536	I/Os							293
	Lanes							4
VF(G)400	I/Os	171	195	207	207	207		
	Lanes		4	4	4	4		
FCV(G)484	I/Os							248
	Lanes							4
TQ(G)144	I/Os	84	84					
	Lanes							
FG(G)484	I/Os	209	233	267	267	267	267	
	Lanes		4	4	4	4	4	
FG(G)676	I/Os					387	425	
	Lanes					4	4	

Table 3 • **I/Os per Package *(continued)***

Packages		M2S005 (S)	M2S010 (S/T/TS)[1,2]	M2S025 (T/TS)[1]	M2S050 (T/TS)[1]	M2S060 (T/TS)[1]	M2S090 (T/TS)[1, 3, 4]	M2S150 (T/TS)[5]
FG(G)896	I/Os				377			
	Lanes				8			
FC(G)1152	I/Os							574
	Lanes							16

1. Military temperature 010/025/050/060/090 are only available in the FG(G)484 package.
2. M2S010S device is only available in TQ(G)144 package.
3. 090 FCSG325 is 11 × 13.5 package dimension.
4. The M2S090 (T/TS) device in the FCS(G)325 package is available with an ordering code of XZ48. The XZ48 ordering code pre-configures the device for Auto Update mode. Minimum Order quantities apply, contact your local Microsemi sales office for details.
5. Military temperature 150 devices are only available in the FC(G)1152 package.

Note: Shaded cells indicate that the device packages have vertical migration capability.

The following table lists the package details along with the supported devices and their features.

Table 4 • **Features per Device/Package Combination**

		Features										
Package	Devices	MDDR	FDDR	Crystal Oscillators	5G SerDes Lanes[1]	PCIe Endpoints	ULPI	UTMI	MSIO (3.3 V max)[2]	MSIOD (2.5 V max)[3]	DDRIO (2.5 V max)	Total User I/Os
TQ(G)144[4]	M2S005 (S)			2			1	1	52	9	23	84
	M2S010 (S)			2			1	1	50	11	23	84
VF(G)256[4]	M2S005 (S)			2			1	1	119	12	30	161
	M2S010 (T/TS)	×18[5]		2	2	1	1	1	66	8	64	138
	M2S025 (T/TS)	×18[5]		2	2	1	1	1	66	8	64	138
FCS(G)325[4]	M2S025 (T/TS)	×18[5]		2	2	1	1	1	94	22	64	180
	M2S050 (T/TS)	×18[6]		1	2	1	0	1	90	22	88	200
	M2S060 (T/TS)	×18[5]		2	2	2	1	1	114	22	64	200
	M2S090 (T/TS)	×18[5]		2	4	2	1	1	104	12	64	180
VF(G)400[4]	M2S005 (S)	×18[5]		2			1	1	79	28	64	171
	M2S010 (T/TS)	×18[5]		2	4	1	1	1	99	32	64	195
	M2S025 (T/TS)	×18[5]		2	4	1	1	1	111	32	64	207
	M2S050 (T/TS)	×18[6]		1	4	1	0	1	87	32	88	207
	M2S060 (T/TS)	×18[5]		2	4	2	1	1	111	32	64	207
FCV(G)484[4]	M2S150 (T/TS)	×18[5]	×18[5]	2	4	4[7]	1	1	91	34	123	273
FG(G)484[4]	M2S005 (S)	×18[5]		2			1	1	115	28	66	209
	M2S010 (T/TS)	×18[5]		2	4	1	1	1	123	40	70	233
	M2S025 (T/TS)	×18[5]		2	4	1	1	1	157	40	70	267
	M2S050 (T/TS)	×18[6]		1	4	1	0	1	105	40	122	267
	M2S060 (T/TS)	×18[5]		2	4	2	1	1	157	40	70	267
	M2S090 (T/TS)	×18[5]		2	4	2	1	1	157	40	70	267

Table 4 • **Features per Device/Package Combination *(continued)***

		Features										
Package	**Devices**	**MDDR**	**FDDR**	**Crystal Oscillators**	**5G SerDes Lanes[1]**	**PCIe Endpoints**	**ULPI**	**UTMI**	**MSIO (3.3 V max)[2]**	**MSIOD (2.5 V max)[3]**	**DDRIO (2.5 V max)**	**Total User I/Os**
FCS(G)536[4]	M2S150 (T/TS)	×18[5]	×18[5]	2	4	4[7]	1	1	151	16	126	293
FG(G)676[4]	M2S060 (T/TS)	×18[5]		2	4	2	1	1	271	40	76	387
	M2S090 (T/TS)	×18[5]		2	4	2	1	1	309	40	76	425
FG(G)896 [4, 8]	M2S050 (T/TS)	×36[9]	×36[9]	1	8	2	1	1	139	62	176	377
FC(G)1152[4]	M2S150 (T/TS)	×36[10]	×36[10]	2	16	4	1	1	292	106	176	574

1. *Maximum SerDes rate for Military temperature devices is 3.125 Gbps.*
2. *Number of differential MSIO is Number of MSIOs/2 for even and (Number of MSIOs-1)/2 for odd MSIO supports LVDS 3.3/2.5 standard.*
3. *Number of differential MSIOD is Number of MSIODs/2 for even and (Number of MSIODs-1)/2 for odd MSIOD supports only LVDS 2.5 standard.*
4. *All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.*
5. *DDR supports ×18, ×16, ×9, and ×8 modes.*
6. *DDR supports ×18 and ×16 modes.*
7. *4 PCIe Gen1/Gen2 endpoints ×1 lane configuration.*
8. *DDR3 is non-compliant. Call technical support for details.*
9. *DDR supports ×36, ×32, ×18, and ×16 modes.*
10. *DDR supports ×36, ×32, ×18, ×16, ×9, and ×8 modes.*

The following table lists the available programming interfaces.

Table 5 • **Available Programming Interfaces**

Package	**Devices**	**JTAG**	**SPI_0**	**Flash_GOLDEN_N**	**System Controller SPI Port**
TQ(G)144[1]	M2S005 (S)	Yes	Yes	No	No
	M2S010 (S)	Yes	Yes	No	No
VF(G)256[1]	M2S005 (S)	Yes	Yes	Yes	Yes
	M2S010 (T/TS)	Yes	Yes	Yes	No
	M2S025 (T/TS)	Yes	Yes	Yes	No
FCS(G)325[1]	M2S025 (T/TS)	Yes	Yes	No	No
	M2S050 (T/TS)	Yes	Yes	No	No
	M2S060 (T/TS)	Yes	Yes	No	No
	M2S090 (T/TS)	Yes	Yes	No	No
VF(G)400[1]	M2S005 (S)	Yes	Yes	Yes	Yes
	M2S010 (T/TS)	Yes	Yes	Yes	Yes
	M2S025 (T/TS)	Yes	Yes	Yes	Yes
	M2S050 (T/TS)	Yes	Yes	Yes	Yes
	M2S060 (T/TS)	Yes	Yes	Yes	Yes
FCV(G)484[1]	M2S150 (T/TS)	Yes	Yes	Yes	Yes

Table 5 • **Available Programming Interfaces *(continued)***

Package	Devices	JTAG	SPI_0	Flash_GOLDEN_N	System Controller SPI Port
FG(G)484[1]	M2S005 (S)	Yes	Yes	Yes	Yes
	M2S010 (T/TS)	Yes	Yes	Yes	Yes
	M2S025 (T/TS)	Yes	Yes	Yes	Yes
	M2S050 (T/TS)	Yes	Yes	Yes	Yes
	M2S060 (T/TS)	Yes	Yes	Yes	Yes
	M2S090 (T/TS)	Yes	Yes	Yes	Yes
FCS(G)536[1]	M2S150 (T/TS)	Yes	Yes	Yes	Yes
FG(G)676[1]	M2S060 (T/TS)	Yes	Yes	Yes	Yes
	M2S090 (T/TS)	Yes	Yes	Yes	Yes
FG(G)896[1]	M2S050 (T/TS)	Yes	No	Yes	Yes
FC(G)1152[1]	M2S150 (T/TS)	Yes	Yes	Yes	Yes

1. *All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.*

The following table lists the programming modes that are required for chip resources.

Table 6 • **Chip Resources Needed for Programming Modes**

Programming Mode	JTAG	SPI_0	Flash_GOLDEN_N	System Controller SPI Port
External FlashPro4/5	Yes	No	No	No
External uP – JTAG slave	Yes	No	No	No
External uP – SPI Slave	No	No	No	Yes
Auto Programming	No	Yes	Yes	No
2-Step IAP	No	Yes	No	No
Programming Recovery	No	Yes	No	No

2.6 SmartFusion2 Commercial and Industrial Temperature Grade Devices

The following table lists SmartFusion2 devices and device ranges that are supported without data security.

Table 7 • **SmartFusion2 Devices without Data Security (All Speed Grades, C, and I Temperature)[1]**

M2S	FCS(G)325	VF(G)256	FCS(G)536	VF(G)400	FCV(G)484	TQ(G)144	FG(G)484	FG(G)676	FG(G)896	FC(G)1152
005										
010		T		T			T			
025	T	T		T			T			
050	T			T			T		T	
060	T			T			T	T		
090	T						T	T		
150			T		T					T

1. *All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.*

Note: T indicates that the devices are available with Transceiver. Example ordering code: M2S025T-FCSG325

Note: Shaded cells indicate that the devices are available without Transceiver. Example ordering code: M2S025-FCSG325

The following table lists SmartFusion2 devices and device ranges that are supported with data security.

Table 8 • **SmartFusion2 Data Security S Devices (All Speed Grades, C, and I Temperature)[1]**

M2S	FCS(G)325	VF(G)256	FCS(G)536	VF(G)400	FCV(G)484	TQ(G)144	FG(G)484	FG(G)676	FG(G)896	FC(G)1152
005		S		S		S	S			
010		TS		TS		S	TS			
025	TS	TS		TS			TS			
050	TS			TS			TS		TS	
060	TS			TS			TS	TS		
090	TS						TS	TS		
150			TS		TS					TS

1. All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

Note: S indicates that the devices are available with Data Security.
Example ordering code: M2S005S-VFG400.

Note: TS indicates that the devices are available with Transceiver and Data Security.
Example ordering code: M2S025TS-FCSG325.

2.6.1 SmartFusion2 Military Temperature Grade Devices

Following are the SmartFusion2 military temperature grade devices:

- M2S010 (T/TS)-1FG(G)484M
- M2S025 (T/TS)-1FG(G)484M
- M2S050 (T/TS)-1FG(G)484M
- M2S060 (T/TS)-1FG(G)484M
- M2S090 (T/TS)-1FG(G)484M
- M2S150 (T/TS)-1FC(G)1152M

Note: Gold Wire bonds are available for the FG484 package by appending X399 to the part number when ordering, for example: M2S090 (T/TS)-1FG484MX399.

Note: All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

2.7 SmartFusion2 Device Status

See *DS0128: IGLOO2 and SmartFusion2 Datasheet* for device status.

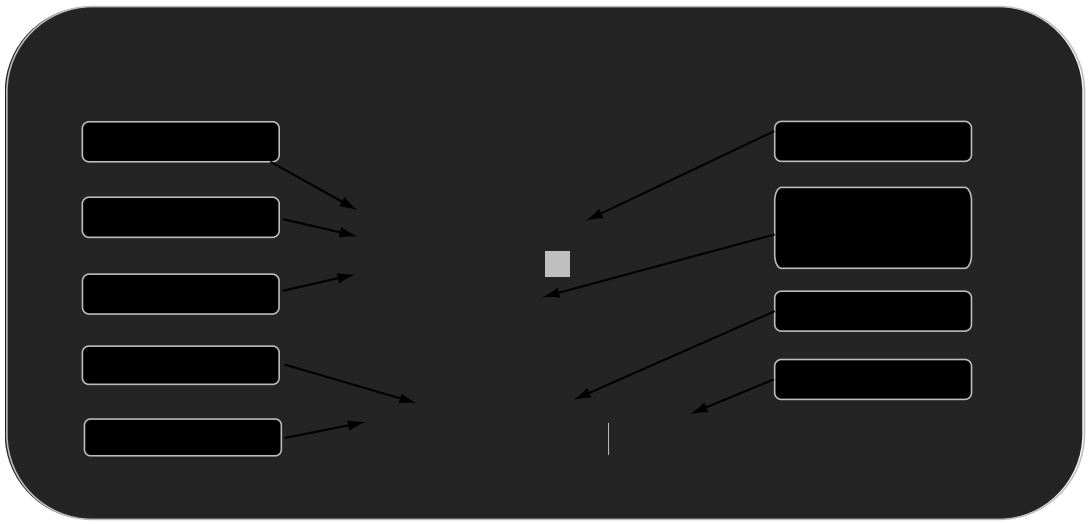
2.8 SmartFusion2 Datasheet and Pin Descriptions

The datasheet and pin descriptions are published separately:

- *DS0128: IGLOO2 and SmartFusion2 Datasheet*
- *DS0134: SmartFusion2 and IGLOO2 Automotive Grade 2 Datasheet*
- *PB0136: Automotive Grade 2 SmartFusion2 SoC FPGAs Product Brief*
- *DS0115: SmartFusion2 Pin Descriptions Datasheet*

2.9 Marking Specification Details

Microsemi normally topside marks the full ordering part number on each device. The following figure provides the details for each character code present on Microsemi's SmartFusion2 SoC FPGA devices.



3 SmartFusion2 Device Family Overview

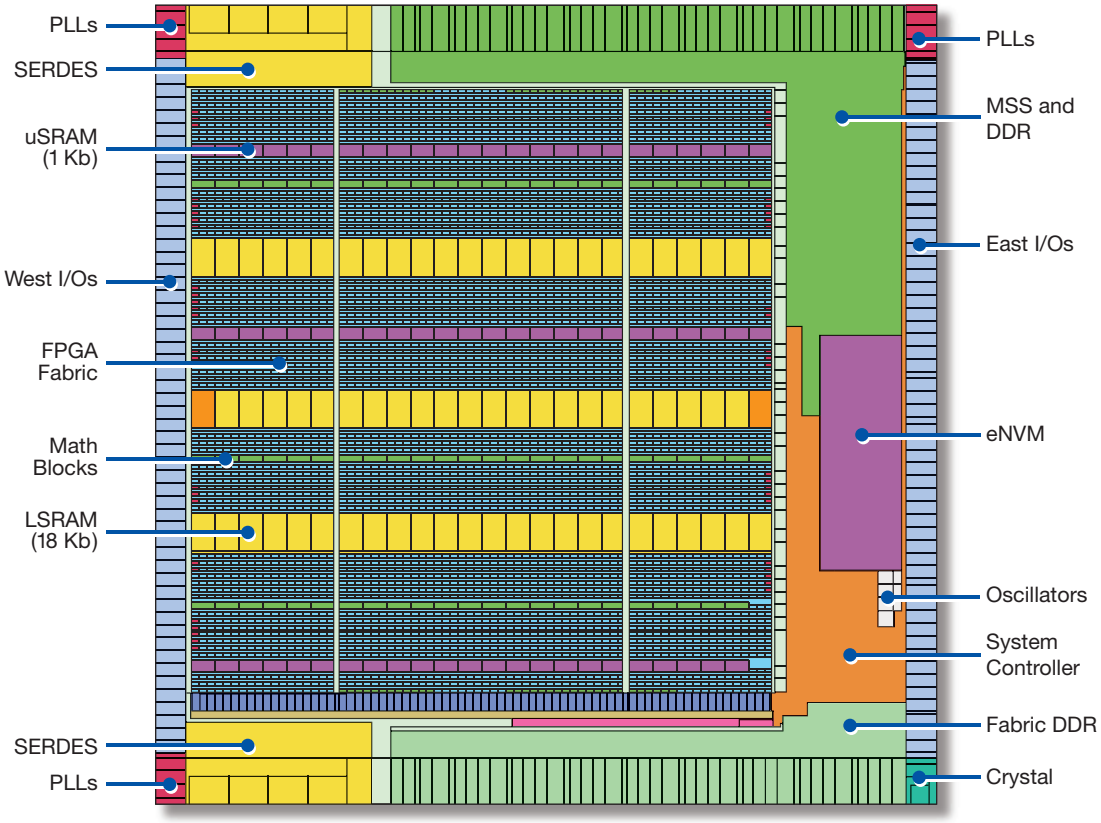
Microsemi's SmartFusion2 SoC FPGAs integrate the fourth generation flash-based FPGA fabric, an ARM Cortex-M3 processor, and high-performance communication interfaces on a single chip. The SmartFusion2 FPGA is the industry's lowest power, the most secure, and has the highest reliability of any programmable logic solution.

SmartFusion2 FPGAs offer up to 3.6X the gate density, up to 2X the performance of previous flash-based FPGA families, and include multiple memory blocks and multiply accumulate blocks for DSP processing. The 166 MHz ARM Cortex-M3 processor is enhanced with ETM and 8 Kbyte instruction cache, and additional peripherals including CAN, Gigabit Ethernet, and high-speed USB. High-speed serial interfaces enable PCIe, XAUI/XGXS plus native SerDes communication while DDR2/DDR3 memory controllers provide high-speed memory interfaces.

3.1 SmartFusion2 Chip Layout

The following figure shows the SmartFusion2 chip layout and its various parts highlighted.

Figure 3 • **SmartFusion2 Chip Layout**



3.2 Reliability

SmartFusion2 flash-based fabric has zero FIT configuration rate due to its SEU immunity, which is critical in reliability applications. The flash fabric also has the advantage that no external configuration memory is required, making the device instant-on; it retains configuration when powered off. To complement this unique FPGA capability, SmartFusion2 devices add reliability to many other aspects of the device. Single error correct double error detect (SECDED) protection is implemented on the Cortex-M3 embedded scratch pad memory, Ethernet, CAN, and USB buffers, and is optional on the DDR memory controllers. This means that if a one-bit error is detected, the error is corrected automatically. If errors of more than

one bit are detected, they are not corrected. SECDED error signals are brought to the FPGA fabric to allow the user to monitor the status of these protected internal memories. Other areas of the architecture are implemented with latches, which are more resistant to SEUs. Therefore, no correction is needed in DDR bridges (MSS, MDDR, and FDDR), instruction cache and MMUART, SPI, and PCIe FIFOs.

3.3 Highest Security Devices

Building further on the intrinsic security benefits of flash nonvolatile memory technology, the SmartFusion2 family incorporates essentially all the legacy security features that made the original SmartFusion®, Fusion®, IGLOO®, and ProASIC®3 third-generation flash FPGAs and cSoCs the gold standard for secure devices in the PLD industry. In addition, the fourth-generation flash-based SmartFusion2 SoC FPGAs add many unique design, data security features, and use models new to the PLD industry.

3.3.1 Design Security vs. Data Security

When classifying the security attributes of programmable logic devices (PLDs), a useful distinction is made between design security and data security.

3.3.2 Design Security

Design security protects the intent of the owner of the design such as keeping the design and associated bitstream keys confidential, preventing design changes (for example, insertion of Trojan Horses), and controlling the number of copies made throughout the device life cycle. Design security may also be known as intellectual property (IP) protection. It is one aspect of anti-tamper (AT) protection. Design security applies to the device from initial production, includes any updates such as in-the-field upgrades, and can include decommissioning of the device at the end of its life, if desired. Good design security is a prerequisite for good data security.

The following are the main design security features supported.

Table 9 • **Design Security Features**

Features (all devices)	M2S005, M2S010, M2S025, and M2S050	M2S060, M2S090, and M2S150
Software memory protection unit (MPU)	●	●
FlashLock® passcode security (256-bit)	●	●
Flexible security settings using flash lock-bits	●	●
Encrypted/authenticated design key loading	●	●
Symmetric key design security (256-bit)	●	●
Design key verification protocol	●	●
Encrypted/authenticated configuration loading	●	●
Certificate-of-conformance (C-of-C)	●	●
Back-tracking prevention (also known as, versioning)	●	●
Device certificate(s) (anti-counterfeiting)	●	●
Support for configuration variations	●	●
Fabric NVM and eNVM integrity tests	●	●
Information services (S/N, Cert., USERCODE, and others)	●	●

Table 10 • **Data Security Features *(continued)***

Features (S devices)	M2S005S, M2S010S, M2S010TS, M2S025TS, and M2S050TS	M2S060TS, M2S090TS, and M2S150TS
SRAM-PUF key importance and enrollment service		•
SRAM-PUF key regeneration service		•

3.4 Low Power

Microsemi's flash-based FPGA fabric results in extremely low-power design implementation with static power as low as 7.5 mW for 6,060 LE devices. Flash*Freeze (F*F) technology provides an ultra-low power static mode (Flash*Freeze mode) for SmartFusion2 devices with power less than 11 mW for the largest device that contains146,124 LEs. Flash*Freeze mode entry retains all the SRAM and register information, and the exit from Flash*Freeze mode achieves rapid recovery to active mode.

3.5 High-Performance FPGA Fabric

Built on 65 nm process technology, the SmartFusion2 FPGA fabric is composed of four building blocks such as the logic module, the large SRAM, the micro SRAM, and the mathblock. The logic module is the basic logic element and has advanced features:

- A fully permutable 4-input LUT optimized for lowest power
- A dedicated carry chain based on carry look-ahead technique
- A separate flip-flop which can be used independently from the LUT

The 4-input LUT can be configured either to implement any 4-input combinatorial function or to implement an arithmetic function where the LUT output is XORed with carry input to generate the sum output.

3.5.1 Dual-Port Large SRAM

Large SRAM (LSRAM) (RAM1Kx18) is targeted for storing large memory for use with various operations. Each LSRAM block can store up to 18,432 bits. Each RAM1Kx18 block contains two independent data ports such as Port A and Port B. LSRAM is synchronous for both read and write operations. Operations are triggered on the rising edge of the clock. The data output ports of the LSRAM have pipeline registers which have control signals that are independent of the SRAM's control signals.

3.5.2 Three-Port Micro SRAM

µSRAM(RAM64x18) is the second type of SRAM, which is embedded in the fabric of SmartFusion2 devices. RAM64x18 uSRAM is a 3-port SRAM; Port A and Port B are used as read ports and Port C is used as write port. The two read ports are independent of each other and can perform read operations in both synchronous and asynchronous modes. The write port is always synchronous. The uSRAM block is approximately 1 KB (1,152 bits) in size. These uSRAM blocks are primarily targeted for building embedded FIFOs to be used by any embedded fabric masters.

3.5.3 Mathblocks for DSP Applications

The fundamental building block in any digital signal processing algorithm is the MACC function. SmartFusion2 FPGAs implement a custom 18 x 18 MACC block for efficient implementation of complex DSP algorithms such as finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast fourier transform (FFT) for filtering and image processing applications.

Each mathblock has the following capabilities:

- Supports 18 x 18 signed multiplications natively (A[17:0] x B[17:0])
- Supports dot product; the multiplier computes:
  - (A[8:0] x B[17:9] + A[17:9] x B[8:0]) x 2^9
- Built-in addition, subtraction, and accumulation units to combine multiplication results efficiently

3.6.6 Fabric Interface Controller

The fabric interface controller (FIC) block provides two separate interfaces between the MSS and the FPGA fabric such as the MSS master (MM) and fabric master (FM). Each of these interfaces can be configured to operate as AHB-Lite or APB3. Depending on device density, there are up to two FIC blocks (FIC_0 and FIC_1) present in the MSS.

3.6.7 Embedded SRAM

The MSS contains two blocks of 32 KB embedded SRAM (eSRAM), giving a total of 64 KB. Having the eSRAM arranged as two separate blocks allows the user to take advantage of the Harvard architecture of the Cortex-M3 processor. For example, code could be located in one eSRAM, while data, such as the stack, could be located in the other.

The eSRAM is designed for SECDED protection. When SECDED is disabled, the SRAM usually used to store SECDED data may be reused as an extra 16 KB of eSRAM.

3.6.8 Embedded NVM

The MSS contains up to 512 KB of embedded NVM (eNVM) (64 bits wide). Accesses to the eNVM from the Cortex-M3 processor are cacheable.

3.6.9 DMA Engines

Two DMA engines are present in the MSS such as high-performance DMA and peripheral DMA.

3.6.9.1 High-Performance DMA

The high-performance DMA (HPDMA) engine provides efficient memory to memory data transfers between an external DDR memory and internal eSRAM. This engine has two separate AHB-Lite interfaces—one to the MDDR bridge and the other to the AHB bus matrix. All transfers by the HPDMA are full word transfers.

3.6.9.2 Peripheral DMA

The peripheral DMA engine (PDMA) is tuned for offloading byte-intensive operations, involving MSS peripherals, to and from the internal eSRAMs. Data transfers can also be targeted to user logic/RAM in the FPGA fabric.

3.6.10 APB Configuration Bus

Each SmartFusion2 device has an APB configuration bus that allow the user to initialize the SerDes ASIC blocks, the fabric DDR memory controller, and user instantiated peripherals in the FPGA fabric.

3.6.11 Peripherals

A large number of communications and general purpose peripherals are implemented in the MSS.

3.6.11.1 USB Controller

The MSS contains a high speed USB 2.0 on-the-go (OTG) controller with the following features:

- Operates either as the function controller of a high-speed / full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions.
- Complies with the USB 2.0 standard for high-speed functions and with the *On-The-Go* supplement to the USB 2.0 specification.
- Supports OTG communications with one or more high-speed, full-speed, or low-speed devices.

3.6.11.2 Triple Speed Ethernet MAC

The triple speed Ethernet (TSE) MAC supports IEEE 802.3 10/100/1000 Mbps Ethernet operation. The following PHY interfaces are directly supported by the MAC:

- GMII
- MII
- TBI

3.7 Clock Sources: On-Chip Oscillators, PLLs, and CCCs

SmartFusion2 devices have two on-chip RC oscillators—a 1 MHz RC oscillator and a 50 MHz RC oscillator—and up to two main crystal oscillators (32 kHz–20 MHz). These are available to the user for generating clocks to the on-chip resources and the logic built on the FPGA fabric array. The second crystal oscillator available on the SmartFusion2 devices is dedicated for RTC clocking. These oscillators (except the RTC crystal oscillator) can be used in conjunction with the integrated user phase-locked loops (PLLs) and fabric clock conditioning circuits (FAB_CCC) to generate clocks of varying frequency and phase. In addition to being available to the user, these oscillators are also used by the system controller, power-on reset circuitry, MSS during Flash*Freeze mode, and the RTC.

SmartFusion2 devices have up to eight fabric CCC (FAB_CCC) blocks and a dedicated PLL associated with each CCC to provide flexible clocking to the FPGA fabric portion of the device. The user has the freedom to use any of the eight PLLs and CCCs to generate the fabric clocks and the internal MSS clock from the base fabric clock (CLK_BASE). There is also a dedicated CCC block for the MSS (MSS_CCC) and an associated PLL (MPLL) for MSS clocking and de-skewing the CLK_BASE clock. The fabric alignment clock controller (FACC), part of the MSS CCC, is responsible for generating various aligned clocks required by the MSS for correct operation of the MSS blocks and synchronous communication with the user logic in the FPGA fabric.

3.8 High-Speed Serial Interfaces

3.8.1 SerDes Interface

SmartFusion2 has up to four 5 Gbps SerDes transceivers, each supporting the following:

- Four SerDes lanes
- The native EPCS SerDes interface facilitates implementation of SRIO in fabric or an SGMII interface for the Ethernet MAC in MSS. In EPCS mode, the SerDes runs at a maximum rate of 3.2 Gbps.

3.8.2 PCI Express

PCI express (PCIe) is a high speed, packet-based, point-to-point, low pin count, and serial interconnect bus. The SmartFusion2 family has two hard high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block and following are the main features supported:

- Supports ×1, ×2, and ×4 lane configuration
- Endpoint configuration only
- PCI Express Base Specification Revision 2.0
- 2.5 and 5.0 Gbps compliant
- Embedded receive (2 KB), transmit (1 KB) and retry (1 KB) buffer dual-port RAM implementation
- Up to 2 Kbytes maximum payload size
- 64-bit AXI or 32-bit AHB-Lite Master and Slave interface to the application layer
- 32-bit APB interface to access configuration and status registers of PCIe system
- Up to 3 × 64 bit base address registers
- 1 virtual channel (VC)

3.8.3 XAUI/XGXS Extension

The XAUI/XGXS extension allows the user to implement a 10 Gbps (XGMII) Ethernet PHY interface by connecting the Ethernet MAC fabric interface through an appropriate soft IP block in the fabric.

3.9 High-Speed Memory Interfaces: DDRx Memory Controllers

There are up to three DDR subsystems, MDDR (MSS DDR), and FDDR (fabric DDR) present in SmartFusion2 devices. Each subsystem consists of a DDR controller, PHY, and a wrapper. The MDDR has an interface from the MSS and fabric, and FDDR provides an interface from the fabric.

3.10.3 IP Cores

SmartFusion2 SoC FPGAs contain an ARM Cortex-M3 processor and multiple peripherals hardcoded into the device. In addition to these, Microsemi offers many soft peripherals that can be placed in the FPGA fabric of the device. These include Core429, Core1553, CoreJESD204BRX/TX, CoreFRI, CoreFFT, and many other DirectCores. See *IP Cores* for more information.