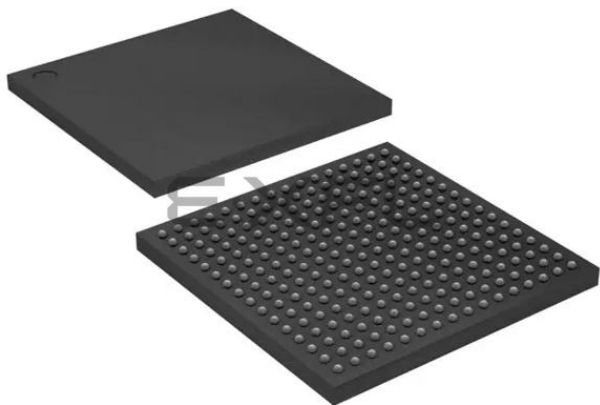




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	6.2 ns
Voltage Supply - Internal	1.71V ~ 1.89V
Number of Logic Elements/Blocks	1270
Number of Macrocells	980
Number of Gates	-
Number of I/O	211
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5m1270zf256a5n

Recommended Operating Conditions

Table 3–2 lists recommended operating conditions for the MAX V device family.

Table 3–2. Recommended Operating Conditions for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT} (1)	1.8-V supply voltage for internal logic and in-system programming (ISP)	MAX V devices	1.71	1.89	V
V_{CCIO} (1)	Supply voltage for I/O buffers, 3.3-V operation	—	3.00	3.60	V
	Supply voltage for I/O buffers, 2.5-V operation	—	2.375	2.625	V
	Supply voltage for I/O buffers, 1.8-V operation	—	1.71	1.89	V
	Supply voltage for I/O buffers, 1.5-V operation	—	1.425	1.575	V
	Supply voltage for I/O buffers, 1.2-V operation	—	1.14	1.26	V
V_I	Input voltage	(2), (3), (4)	–0.5	4.0	V
V_O	Output voltage	—	0	V_{CCIO}	V
T_J	Operating junction temperature	Commercial range	0	85	°C
		Industrial range	–40	100	°C
		Extended range (5)	–40	125	°C

Notes to Table 3–2:

- (1) MAX V device ISP and/or user flash memory (UFM) programming using JTAG or logic array is not guaranteed outside the recommended operating conditions (for example, if brown-out occurs in the system during a potential write/program sequence to the UFM, Altera recommends that you read back the UFM contents and verify it against the intended write data).
- (2) The minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) During transitions, the inputs may overshoot to the voltages shown below based on the input duty cycle. The DC case is equivalent to 100% duty cycle. For more information about 5.0-V tolerance, refer to the *Using MAX V Devices in Multi-Voltage Systems* chapter.

V_{IN}	Max. Duty Cycle
4.0 V	100% (DC)
4.1 V	90%
4.2 V	50%
4.3 V	30%
4.4 V	17%
4.5 V	10%
- (4) All pins, including the clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (5) For the extended temperature range of 100 to 125°C, MAX V UFM programming (erase/write) is only supported using the JTAG interface. UFM programming using the logic array interface is not guaranteed in this range.

Programming/Erase Specifications

Table 3–3 lists the programming/erase specifications for the MAX V device family.

Table 3–3. Programming/Erase Specifications for MAX V Devices

Parameter	Block	Minimum	Typical	Maximum	Unit
Erase and reprogram cycles	UFM	—	—	1000 (1)	Cycles
	Configuration flash memory (CFM)	—	—	100	Cycles

Note to Table 3–3:

(1) This value applies to the commercial grade devices. For the industrial grade devices, the value is 100 cycles.

DC Electrical Characteristics

Table 3–4 lists DC electrical characteristics for the MAX V device family.

Table 3–4. DC Electrical Characteristics for MAX V Devices (Note 1) (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIO}$ max to 0 V (2)	–10	—	10	μA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIO}$ max to 0 V (2)	–10	—	10	μA
$I_{CCSTANDBY}$	V_{CCINT} supply current (standby) (3)	5M40Z, 5M80Z, 5M160Z, and 5M240Z (Commercial grade) (4), (5)	—	25	90	μA
		5M240Z (Commercial grade) (6)	—	27	96	μA
		5M40Z, 5M80Z, 5M160Z, and 5M240Z (Industrial grade) (5), (7)	—	25	139	μA
		5M240Z (Industrial grade) (6)	—	27	152	μA
		5M570Z (Commercial grade) (4)	—	27	96	μA
		5M570Z (Industrial grade) (7)	—	27	152	μA
		5M1270Z and 5M2210Z	—	2	—	mA
$V_{SCHMITT}$ (8)	Hysteresis for Schmitt trigger input (9)	$V_{CCIO} = 3.3$ V	—	400	—	mV
		$V_{CCIO} = 2.5$ V	—	190	—	mV
$I_{CCPOWERUP}$	V_{CCINT} supply current during power-up (10)	MAX V devices	—	—	40	mA
R_{PULLUP}	Value of I/O pin pull-up resistor during user mode and ISP	$V_{CCIO} = 3.3$ V (11)	5	—	25	$k\Omega$
		$V_{CCIO} = 2.5$ V (11)	10	—	40	$k\Omega$
		$V_{CCIO} = 1.8$ V (11)	25	—	60	$k\Omega$
		$V_{CCIO} = 1.5$ V (11)	45	—	95	$k\Omega$
		$V_{CCIO} = 1.2$ V (11)	80	—	130	$k\Omega$

Table 3-4. DC Electrical Characteristics for MAX V Devices (Note 1) (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{PULLUP}	I/O pin pull-up resistor current when I/O is unprogrammed	—	—	—	300	μA
C_{IO}	Input capacitance for user I/O pin	—	—	—	8	pF
C_{GCLK}	Input capacitance for dual-purpose GCLK/user I/O pin	—	—	—	8	pF

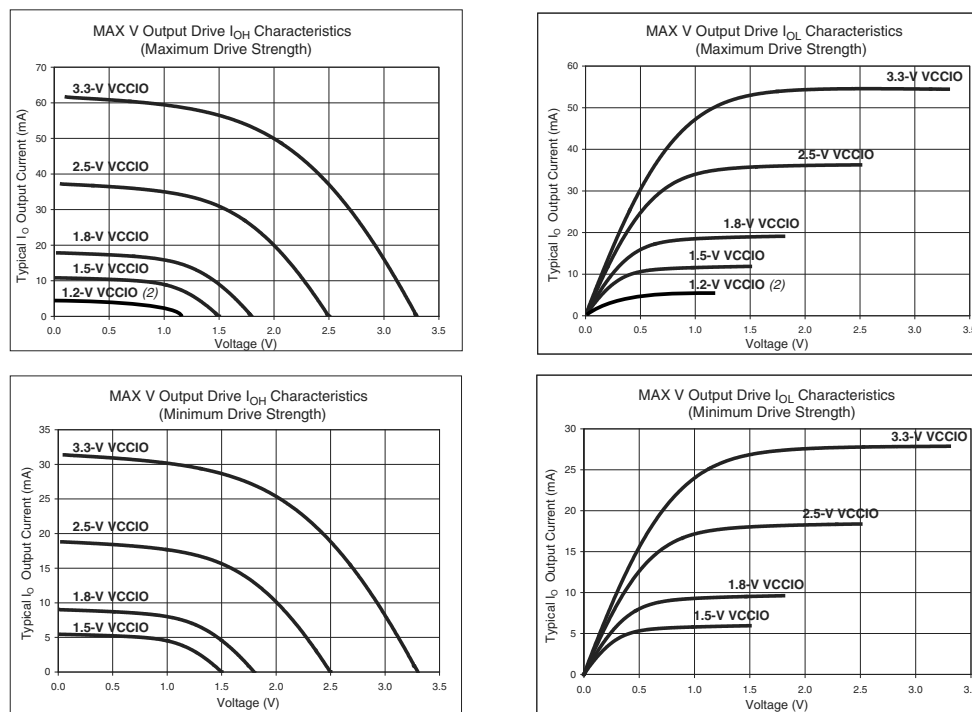
Notes to Table 3-4:

- (1) Typical values are for $T_A = 25^\circ C$, $V_{CCINT} = 1.8 V$ and $V_{CCIO} = 1.2, 1.5, 1.8, 2.5$, or $3.3 V$.
- (2) This value is specified for normal device operation. The value may vary during power-up. This applies to all V_{CCIO} settings (3.3, 2.5, 1.8, 1.5, and 1.2 V).
- (3) $V_I =$ ground, no load, and no toggling inputs.
- (4) Commercial temperature ranges from $0^\circ C$ to $85^\circ C$ with the maximum current at $85^\circ C$.
- (5) Not applicable to the T144 package of the 5M240Z device.
- (6) Only applicable to the T144 package of the 5M240Z device.
- (7) Industrial temperature ranges from $-40^\circ C$ to $100^\circ C$ with the maximum current at $100^\circ C$.
- (8) This value applies to commercial and industrial range devices. For extended temperature range devices, the $V_{SCHMITT}$ typical value is 300 mV for $V_{CCIO} = 3.3 V$ and 120 mV for $V_{CCIO} = 2.5 V$.
- (9) The TCK input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.
- (10) This is a peak current value with a maximum duration of t_{CONFIG} time.
- (11) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO} .

Output Drive Characteristics

Figure 3–1 shows the typical drive strength characteristics of MAX V devices.

Figure 3–1. Output Drive Characteristics of MAX V Devices (Note 1)



Notes to Figure 3–1:

- (1) The DC output current per pin is subject to the absolute maximum rating of Table 3–1 on page 3–1.
- (2) 1.2-V V_{CCIO} is only applicable to the maximum drive strength.

I/O Standard Specifications

Table 3–5 through Table 3–13 on page 3–8 list the I/O standard specifications for the MAX V device family.

Table 3–5. 3.3-V LVTTTL Specifications for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.5	0.8	V
V_{OH}	High-level output voltage	$I_{OH} = -4 \text{ mA}$ (1)	2.4	—	V
V_{OL}	Low-level output voltage	$I_{OL} = 4 \text{ mA}$ (1)	—	0.45	V

Note to Table 3–5:

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

Table 3–9. 1.5-V I/O Specifications for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.425	1.575	V
V_{IH}	High-level input voltage	—	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$ (2)	V
V_{IL}	Low-level input voltage	—	–0.3	$0.35 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$IOH = -2 \text{ mA}$ (1)	$0.75 \times V_{CCIO}$	—	V
V_{OL}	Low-level output voltage	$IOL = 2 \text{ mA}$ (1)	—	$0.25 \times V_{CCIO}$	V

Notes to Table 3–9:

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.
- (2) This maximum V_{IH} reflects the JEDEC specification. The MAX V input buffer can tolerate a V_{IH} maximum of 4.0, as specified by the V_I parameter in Table 3–2 on page 3–2.

Table 3–10. 1.2-V I/O Specifications for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.14	1.26	V
V_{IH}	High-level input voltage	—	$0.8 \times V_{CCIO}$	$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage	—	–0.3	$0.25 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$IOH = -2 \text{ mA}$ (1)	$0.75 \times V_{CCIO}$	—	V
V_{OL}	Low-level output voltage	$IOL = 2 \text{ mA}$ (1)	—	$0.25 \times V_{CCIO}$	V

Note to Table 3–10:

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

Table 3–11. 3.3-V PCI Specifications for MAX V Devices (Note 1)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	—	$0.5 \times V_{CCIO}$	—	$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage	—	–0.5	—	$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$IOH = -500 \text{ }\mu\text{A}$	$0.9 \times V_{CCIO}$	—	—	V
V_{OL}	Low-level output voltage	$IOL = 1.5 \text{ mA}$	—	—	$0.1 \times V_{CCIO}$	V

Note to Table 3–11:

- (1) 3.3-V PCI I/O standard is only supported in Bank 3 of the 5M1270Z and 5M2210Z devices.

Table 3–12. LVDS Specifications for MAX V Devices (Note 1)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	2.375	2.5	2.625	V
V_{OD}	Differential output voltage swing	—	247	—	600	mV
V_{OS}	Output offset voltage	—	1.125	1.25	1.375	V

Note to Table 3–12:

- (1) Supports emulated LVDS output using a three-resistor network (LVDS_E_3R).

Power Consumption

You can use the Altera® PowerPlay Early Power Estimator and PowerPlay Power Analyzer to estimate the device power.

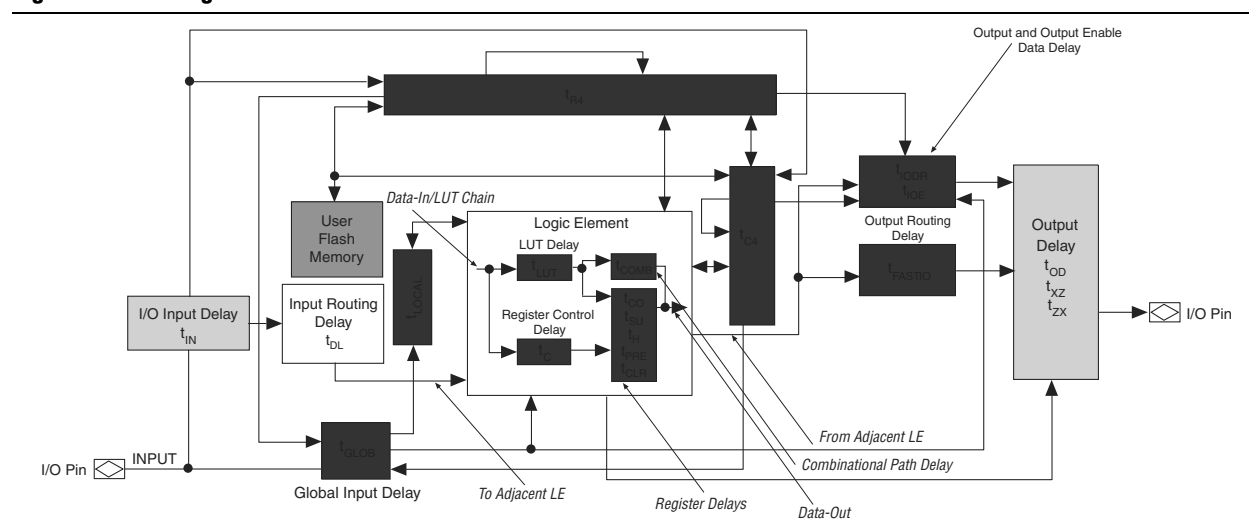
- For more information about these power analysis tools, refer to the *PowerPlay Early Power Estimator for Altera CPLDs User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Timing Model and Specifications

MAX V devices timing can be analyzed with the Altera Quartus® II software, a variety of industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 3-2.

MAX V devices have predictable internal delays that allow you to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 3-2. Timing Model for MAX V Devices



You can derive the timing characteristics of any signal path from the timing model and parameters of a particular device. You can calculate external timing parameters, which represent pin-to-pin timing delays, as the sum of the internal parameters.

- For more information, refer to AN629: *Understanding Timing in Altera CPLDs*.

Preliminary and Final Timing

This section describes the performance, internal, external, and UFM timing specifications. All specifications are representative of the worst-case supply voltage and junction temperature conditions.

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 3-16 lists the status of the MAX V device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under the worst-case voltage and junction temperature conditions.

Table 3-16. Timing Model Status for MAX V Devices

Device	Final
5M40Z	✓
5M80Z	✓
5M160Z	✓
5M240Z	✓
5M570Z	✓
5M1270Z	✓
5M2210Z	✓

Performance

Table 3-17 lists the MAX V device performance for some common designs. All performance values were obtained with the Quartus II software compilation of megafunctions.

Table 3-17. Device Performance for MAX V Devices (Part 1 of 2)

Resource Used	Design Size and Function	Resources Used			Performance				Unit
					5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z		5M1270Z/ 5M2210Z		
		Mode	LEs	UFM Blocks	C4	C5, I5	C4	C5, I5	
LE	16-bit counter (1)	—	16	0	184.1	118.3	247.5	201.1	MHz
	64-bit counter (1)	—	64	0	83.2	80.5	154.8	125.8	MHz
	16-to-1 multiplexer	—	11	0	17.4	20.4	8.0	9.3	ns
	32-to-1 multiplexer	—	24	0	12.5	25.3	9.0	11.4	ns
	16-bit XOR function	—	5	0	9.0	16.1	6.6	8.2	ns
	16-bit decoder with single address line	—	5	0	9.2	16.1	6.6	8.2	ns

Table 3–18. LE Internal Timing Microparameters for MAX V Devices (Part 2 of 2)

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{CLKHL}	Minimum clock high or low time	253	—	339	—	216	—	266	—	ps
t _C	Register control delay	—	1,356	—	1,741	—	1,114	—	1,372	ps

Table 3–19. IOE Internal Timing Microparameters for MAX V Devices

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{FASTIO}	Data output delay from adjacent LE to I/O block	—	170	—	428	—	207	—	254	ps
t _{IN}	I/O input pad and buffer delay	—	907	—	986	—	920	—	1,132	ps
t _{GLOB} (1)	I/O input pad and buffer delay used as global signal pin	—	2,261	—	3,322	—	1,974	—	2,430	ps
t _{IOE}	Internally generated output enable delay	—	530	—	1,410	—	374	—	460	ps
t _{DL}	Input routing delay	—	318	—	509	—	291	—	358	ps
t _{OD} (2)	Output delay buffer and pad delay	—	1,319	—	1,543	—	1,383	—	1,702	ps
t _{XZ} (3)	Output buffer disable delay	—	1,045	—	1,276	—	982	—	1,209	ps
t _{ZX} (4)	Output buffer enable delay	—	1,160	—	1,353	—	1,303	—	1,604	ps

Notes to Table 3–19:

- (1) Delay numbers for t_{GLOB} differ for each device density and speed grade. The delay numbers for t_{GLOB} , shown in Table 3–19, are based on a 5M240Z device target.
- (2) For more information about delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3–34 on page 3–24 and Table 3–35 on page 3–25.
- (3) For more information about t_{XZ} delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3–22 on page 3–15 and Table 3–23 on page 3–15.
- (4) For more information about t_{ZX} delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3–20 on page 3–14 and Table 3–21 on page 3–14.

Table 3–22. t_{xz} IOE Microparameter Adders for Fast Slew Rate for MAX V Devices

Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	16 mA	—	0	—	0	—	0	—	0	ps
	8 mA	—	–69	—	–69	—	–74	—	–91	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	ps
	4 mA	—	–69	—	–69	—	–74	—	–91	ps
2.5-V LVTTTL / LVCMOS	14 mA	—	–7	—	–10	—	–46	—	–56	ps
	7 mA	—	–66	—	–69	—	–82	—	–101	ps
1.8-V LVTTTL / LVCMOS	6 mA	—	45	—	37	—	–7	—	–8	ps
	3 mA	—	34	—	25	—	119	—	147	ps
1.5-V LVCMOS	4 mA	—	166	—	155	—	339	—	418	ps
	2 mA	—	190	—	179	—	464	—	571	ps
1.2-V LVCMOS	3 mA	—	300	—	283	—	817	—	1,006	ps
3.3-V PCI	20 mA	—	–69	—	–69	—	80	—	99	ps
LVDS	—	—	–7	—	–10	—	–46	—	–56	ps
RSDS	—	—	–7	—	–10	—	–46	—	–56	ps

Table 3–23. t_{xz} IOE Microparameter Adders for Slow Slew Rate for MAX V Devices

Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LV TTL	16 mA	—	171	—	174	—	73	—	–132	ps
	8 mA	—	112	—	116	—	758	—	553	ps
3.3-V LV CMOS	8 mA	—	171	—	174	—	73	—	–132	ps
	4 mA	—	112	—	116	—	758	—	553	ps
2.5-V LV TTL / LV CMOS	14 mA	—	213	—	213	—	32	—	–173	ps
	7 mA	—	166	—	166	—	714	—	509	ps
1.8-V LV TTL / LV CMOS	6 mA	—	441	—	438	—	96	—	–109	ps
	3 mA	—	496	—	494	—	963	—	758	ps
1.5-V LV CMOS	4 mA	—	765	—	755	—	238	—	33	ps
	2 mA	—	903	—	897	—	1,319	—	1,114	ps
1.2-V LV CMOS	3 mA	—	1,159	—	1,130	—	400	—	195	ps
3.3-V PCI	20 mA	—	112	—	116	—	303	—	373	ps



The default slew rate setting for MAX V devices in the Quartus II design software is “fast”.

Table 3-24. UFM Block Internal Timing Microparameters for MAX V Devices (Part 1 of 2)

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{ACLK}	Address register clock period	100	—	100	—	100	—	100	—	ns
t _{ASU}	Address register shift signal setup to address register clock	20	—	20	—	20	—	20	—	ns
t _{AH}	Address register shift signal hold to address register clock	20	—	20	—	20	—	20	—	ns
t _{ADS}	Address register data in setup to address register clock	20	—	20	—	20	—	20	—	ns
t _{ADH}	Address register data in hold from address register clock	20	—	20	—	20	—	20	—	ns
t _{DCLK}	Data register clock period	100	—	100	—	100	—	100	—	ns
t _{DSS}	Data register shift signal setup to data register clock	60	—	60	—	60	—	60	—	ns
t _{DSH}	Data register shift signal hold from data register clock	20	—	20	—	20	—	20	—	ns
t _{DDS}	Data register data in setup to data register clock	20	—	20	—	20	—	20	—	ns
t _{DDH}	Data register data in hold from data register clock	20	—	20	—	20	—	20	—	ns
t _{DP}	Program signal to data clock hold time	0	—	0	—	0	—	0	—	ns
t _{PB}	Maximum delay between program rising edge to UFM _{busy} signal rising edge	—	960	—	960	—	960	—	960	ns
t _{BP}	Minimum delay allowed from UFM _{busy} signal going low to program signal going low	20	—	20	—	20	—	20	—	ns
t _{PPMX}	Maximum length of busy pulse during a program	—	100	—	100	—	100	—	100	μs

Figure 3-3 through Figure 3-5 show the read, program, and erase waveforms for UFM block timing parameters listed in Table 3-24.

Figure 3-3. UFM Read Waveform

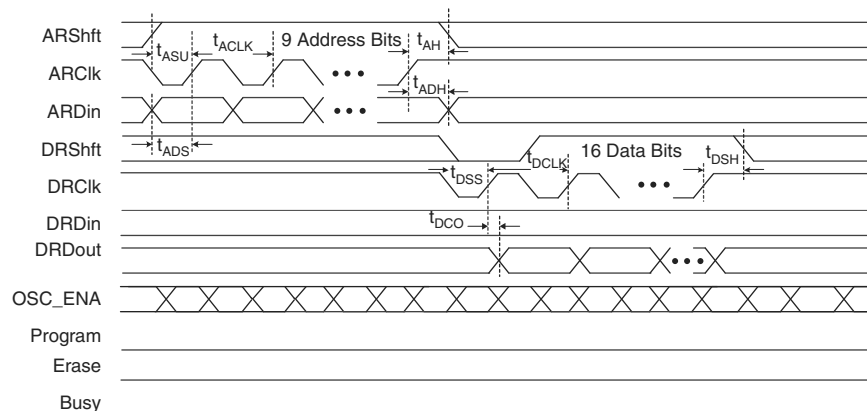


Figure 3-4. UFM Program Waveform

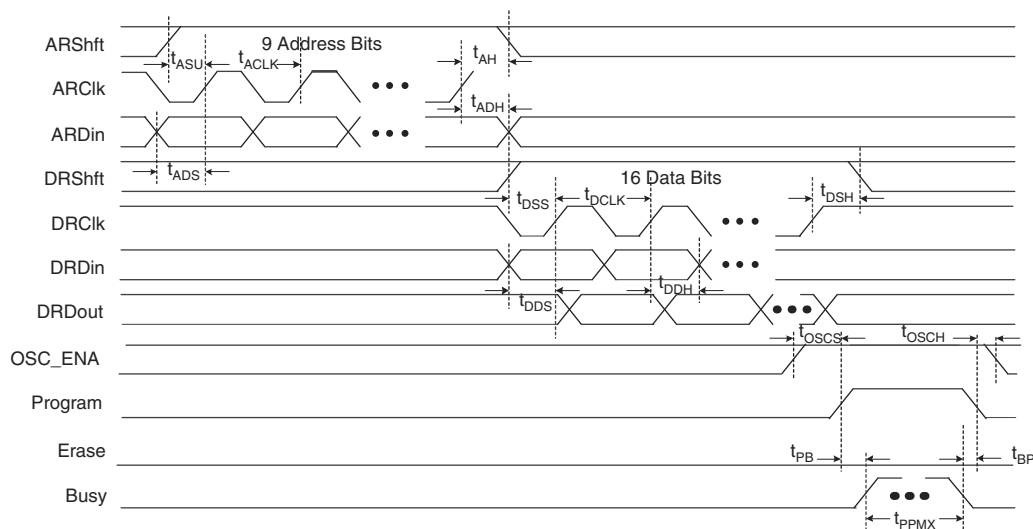


Figure 3-5. UFM Erase Waveform

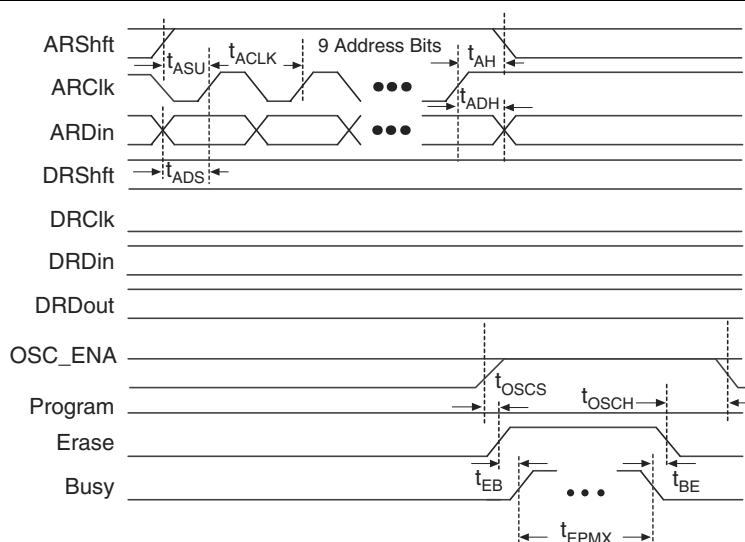


Table 3-25. Routing Delay Internal Timing Microparameters for MAX V Devices

Routing	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
	C4		C5, I5		C4		C5, I5		
	Min	Max	Min	Max	Min	Max	Min	Max	
t _{C4}	—	860	—	1,973	—	561	—	690	ps
t _{R4}	—	655	—	1,479	—	445	—	548	ps
t _{LOCAL}	—	1,143	—	2,947	—	731	—	899	ps

External Timing Parameters

External timing parameters are specified by device density and speed grade. All external I/O timing parameters shown are for the 3.3-V LVTTTL I/O standard with the maximum drive strength and fast slew rate. For external I/O timing using standards other than LVTTTL or for different drive strengths, use the I/O standard input and output delay adders in Table 3-32 on page 3-23 through Table 3-36 on page 3-25.

For more information about each external timing parameters symbol, refer to *AN629: Understanding Timing in Altera CPLDs*.

Table 3–28 lists the external I/O timing parameters for the 5M570Z device.

Table 3–28. Global Clock External I/O Timing Parameters for the 5M570Z Device (Note 1)

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through one LUT	10 pF	—	9.5	—	17.7	ns
t_{PD2}	Best case pin-to-pin delay through one LUT	10 pF	—	5.7	—	8.5	ns
t_{SU}	Global clock setup time	—	2.2	—	4.4	—	ns
t_H	Global clock hold time	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	6.7	2.0	8.7	ns
t_{CH}	Global clock high time	—	253	—	339	—	ps
t_{CL}	Global clock low time	—	253	—	339	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	5.4	—	8.4	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	184.1	—	118.3	MHz

Note to Table 3–28:

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 3–29 lists the external I/O timing parameters for the 5M1270Z device.

Table 3–29. Global Clock External I/O Timing Parameters for the 5M1270Z Device (Note 1), (2)

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through one LUT	10 pF	—	8.1	—	10.0	ns
t_{PD2}	Best case pin-to-pin delay through one LUT	10 pF	—	4.8	—	5.9	ns
t_{SU}	Global clock setup time	—	1.5	—	1.9	—	ns
t_H	Global clock hold time	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	5.9	2.0	7.3	ns
t_{CH}	Global clock high time	—	216	—	266	—	ps
t_{CL}	Global clock low time	—	216	—	266	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	4.0	—	5.0	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	247.5	—	201.1	MHz

Notes to Table 3–29:

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.
- (2) Not applicable to the F324 package of the 5M1270Z device.

Table 3–30 lists the external I/O timing parameters for the F324 package of the 5M1270Z device.

Table 3–30. Global Clock External I/O Timing Parameters for the 5M1270Z Device (Note 1), (2)

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through one LUT	10 pF	—	9.1	—	11.2	ns
t_{PD2}	Best case pin-to-pin delay through one LUT	10 pF	—	4.8	—	5.9	ns
t_{SU}	Global clock setup time	—	1.5	—	1.9	—	ns
t_H	Global clock hold time	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	6.0	2.0	7.4	ns
t_{CH}	Global clock high time	—	216	—	266	—	ps
t_{CL}	Global clock low time	—	216	—	266	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	4.0	—	5.0	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	247.5	—	201.1	MHz

Notes to Table 3–30:

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.
- (2) Only applicable to the F324 package of the 5M1270Z device.

Table 3–31 lists the external I/O timing parameters for the 5M2210Z device.

Table 3–31. Global Clock External I/O Timing Parameters for the 5M2210Z Device (Note 1)

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through one LUT	10 pF	—	9.1	—	11.2	ns
t_{PD2}	Best case pin-to-pin delay through one LUT	10 pF	—	4.8	—	5.9	ns
t_{SU}	Global clock setup time	—	1.5	—	1.9	—	ns
t_H	Global clock hold time	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	6.0	2.0	7.4	ns
t_{CH}	Global clock high time	—	216	—	266	—	ps
t_{CL}	Global clock low time	—	216	—	266	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	4.0	—	5.0	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	247.5	—	201.1	MHz

Note to Table 3–31:

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

External Timing I/O Delay Adders

The I/O delay timing parameters for the I/O standard input and output adders and the input delays are specified by speed grade, independent of device density.

Table 3–32 through Table 3–36 on page 3–25 list the adder delays associated with I/O pins for all packages. If you select an I/O standard other than 3.3-V LVTTL, add the input delay adder to the external t_{SU} timing parameters listed in Table 3–26 on page 3–20 through Table 3–31. If you select an I/O standard other than 3.3-V LVTTL with 16 mA drive strength and fast slew rate, add the output delay adder to the external t_{CO} and t_{PD} listed in Table 3–26 on page 3–20 through Table 3–31.

Table 3–32. External Timing Input Delay Adders for MAX V Devices

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	480	—	591	ps
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	480	—	591	ps
2.5-V LVTTL / LVCMOS	Without Schmitt Trigger	—	42	—	42	—	246	—	303	ps
	With Schmitt Trigger	—	429	—	483	—	787	—	968	ps
1.8-V LVTTL / LVCMOS	Without Schmitt Trigger	—	378	—	368	—	695	—	855	ps
1.5-V LVCMOS	Without Schmitt Trigger	—	681	—	658	—	1,334	—	1,642	ps
1.2-V LVCMOS	Without Schmitt Trigger	—	1,055	—	1,010	—	2,324	—	2,860	ps
3.3-V PCI	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps

Table 3–33. External Timing Input Delay t_{GLOB} Adders for GCLK Pins for MAX V Devices (Part 1 of 2)

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	400	—	493	ps

Table 3-33. External Timing Input Delay t_{GLOB} Adders for GCLK Pins for MAX V Devices (Part 2 of 2)

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	400	—	493	ps
2.5-V LV TTL / LVCMOS	Without Schmitt Trigger	—	242	—	242	—	287	—	353	ps
	With Schmitt Trigger	—	429	—	483	—	550	—	677	ps
1.8-V LV TTL / LVCMOS	Without Schmitt Trigger	—	378	—	368	—	459	—	565	ps
1.5-V LVCMOS	Without Schmitt Trigger	—	681	—	658	—	1,111	—	1,368	ps
1.2-V LVCMOS	Without Schmitt Trigger	—	1,055	—	1,010	—	2,067	—	2,544	ps
3.3-V PCI	Without Schmitt Trigger	—	0	—	0	—	7	—	9	ps

Table 3-34. External Timing Output Delay and t_{OD} Adders for Fast Slew Rate for MAX V Devices

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	16 mA	—	0	—	0	—	0	—	0	ps
	8 mA	—	39	—	58	—	84	—	104	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	ps
	4 mA	—	39	—	58	—	84	—	104	ps
2.5-V LVTTTL / LVCMOS	14 mA	—	122	—	129	—	158	—	195	ps
	7 mA	—	196	—	188	—	251	—	309	ps
1.8-V LVTTTL / LVCMOS	6 mA	—	624	—	624	—	738	—	909	ps
	3 mA	—	686	—	694	—	850	—	1,046	ps
1.5-V LVCMOS	4 mA	—	1,188	—	1,184	—	1,376	—	1,694	ps
	2 mA	—	1,279	—	1,280	—	1,517	—	1,867	ps
1.2-V LVCMOS	3 mA	—	1,911	—	1,883	—	2,206	—	2,715	ps
3.3-V PCI	20 mA	—	39	—	58	—	4	—	5	ps
LVDS	—	—	122	—	129	—	158	—	195	ps
RSDS	—	—	122	—	129	—	158	—	195	ps

Maximum Input and Output Clock Rates

Table 3–37 and Table 3–38 list the maximum input and output clock rates for standard I/O pins in MAX V devices.

Table 3–37. Maximum Input Clock Rate for I/Os for MAX V Devices

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z/5M1270Z/ 5M2210Z	Unit
		C4, C5, I5	
3.3-V LVTTTL	Without Schmitt Trigger	304	MHz
	With Schmitt Trigger	304	MHz
3.3-V LVCMOS	Without Schmitt Trigger	304	MHz
	With Schmitt Trigger	304	MHz
2.5-V LVTTTL	Without Schmitt Trigger	304	MHz
	With Schmitt Trigger	304	MHz
2.5-V LVCMOS	Without Schmitt Trigger	304	MHz
	With Schmitt Trigger	304	MHz
1.8-V LVTTTL	Without Schmitt Trigger	200	MHz
1.8-V LVCMOS	Without Schmitt Trigger	200	MHz
1.5-V LVCMOS	Without Schmitt Trigger	150	MHz
1.2-V LVCMOS	Without Schmitt Trigger	120	MHz
3.3-V PCI	Without Schmitt Trigger	304	MHz

Table 3–38. Maximum Output Clock Rate for I/Os for MAX V Devices

I/O Standard	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z/5M1270Z/ 5M2210Z	Unit
	C4, C5, I5	
3.3-V LVTTTL	304	MHz
3.3-V LVCMOS	304	MHz
2.5-V LVTTTL	304	MHz
2.5-V LVCMOS	304	MHz
1.8-V LVTTTL	200	MHz
1.8-V LVCMOS	200	MHz
1.5-V LVCMOS	150	MHz
1.2-V LVCMOS	120	MHz
3.3-V PCI	304	MHz
LVDS	304	MHz
RSDS	200	MHz

LVDS and RSDS Output Timing Specifications

Table 3–39 lists the emulated LVDS output timing specifications for MAX V devices.

Table 3–39. Emulated LVDS Output Timing Specifications for MAX V Devices

Parameter	Mode	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z/5M1270Z/ 5M2210Z		Unit
		C4, C5, I5		
		Min	Max	
Data rate (1), (2)	×10	—	304	Mbps
	×9	—	304	Mbps
	×8	—	304	Mbps
	×7	—	304	Mbps
	×6	—	304	Mbps
	×5	—	304	Mbps
	×4	—	304	Mbps
	×3	—	304	Mbps
	×2	—	304	Mbps
	×1	—	304	Mbps
t _{DUTY}	—	45	55	%
Total jitter (3)	—	—	0.2	UI
t _{RISE}	—	—	450	ps
t _{FALL}	—	—	450	ps

Notes to Table 3–39:

- (1) The performance of the LVDS_E_3R transmitter system is limited by the lower of the two—the maximum data rate supported by LVDS_E_3R I/O buffer or 2x (F_{MAX} of the ALTLVDS_TX instance). The actual performance of your LVDS_E_3R transmitter system must be attained through the Quartus II timing analysis of the complete design.
- (2) For the input clock pin to achieve 304 Mbps, use I/O standard with V_{CCIO} of 2.5 V and above.
- (3) This specification is based on external clean clock source.

Table 3–40 lists the emulated RSDS output timing specifications for MAX V devices.

Table 3–40. Emulated RSDS Output Timing Specifications for MAX V Devices

Parameter	Mode	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z/5M1270Z/ 5M2210Z		Unit
		C4, C5, I5		
		Min	Max	
Data rate (1)	×10	—	200	Mbps
	×9	—	200	Mbps
	×8	—	200	Mbps
	×7	—	200	Mbps
	×6	—	200	Mbps
	×5	—	200	Mbps
	×4	—	200	Mbps
	×3	—	200	Mbps
	×2	—	200	Mbps
	×1	—	200	Mbps
t _{DUTY}	—	45	55	%
Total jitter (2)	—	—	0.2	UI
t _{RISE}	—	—	450	ps
t _{FALL}	—	—	450	ps

Notes to Table 3–40:

- (1) For the input clock pin to achieve 200 Mbps, use I/O standard with V_{CCIO} of 1.8 V and above.
- (2) This specification is based on external clean clock source.

JTAG Timing Specifications

Figure 3–6 shows the timing waveform for the JTAG signals for the MAX V device family.

Figure 3–6. JTAG Timing Waveform for MAX V Devices

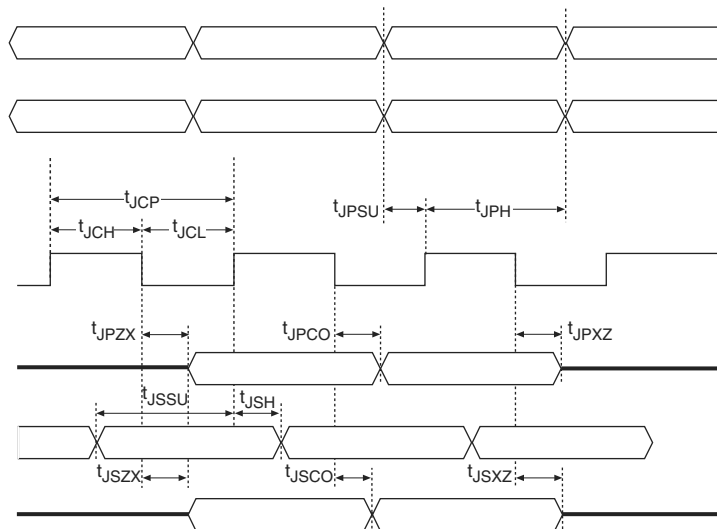


Table 3–41 lists the JTAG timing parameters and values for the MAX V device family.

Table 3–41. JTAG Timing Parameters for MAX V Devices (Part 1 of 2)

Symbol	Parameter	Min	Max	Unit
t_{JCP} (1)	TCK clock period for $V_{CCIO1} = 3.3\text{ V}$	55.5	—	ns
	TCK clock period for $V_{CCIO1} = 2.5\text{ V}$	62.5	—	ns
	TCK clock period for $V_{CCIO1} = 1.8\text{ V}$	100	—	ns
	TCK clock period for $V_{CCIO1} = 1.5\text{ V}$	143	—	ns
t_{JCH}	TCK clock high time	20	—	ns
t_{JCL}	TCK clock low time	20	—	ns
t_{JPSU}	JTAG port setup time (2)	8	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output (2)	—	15	ns
t_{JPZX}	JTAG port high impedance to valid output (2)	—	15	ns
t_{JPXZ}	JTAG port valid output to high impedance (2)	—	15	ns
t_{JSSU}	Capture register setup time	8	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns