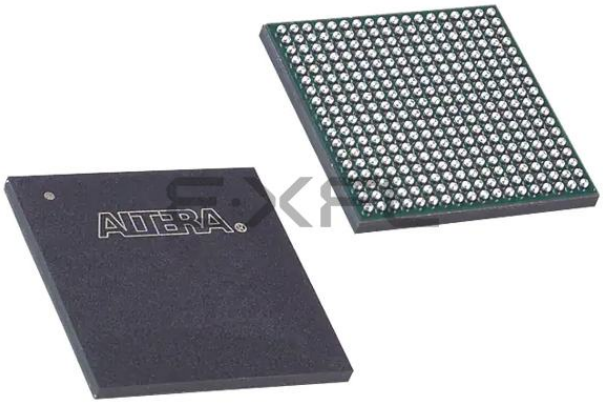

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	6.2 ns
Voltage Supply - Internal	1.71V ~ 1.89V
Number of Logic Elements/Blocks	1270
Number of Macrocells	980
Number of Gates	-
Number of I/O	271
Operating Temperature	0°C ~ 85°C (TJ)
Mounting Type	Surface Mount
Package / Case	324-LBGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5m1270zf324c5n

Programming/Erasure Specifications

Table 3 3 lists the programming/erasure specifications for the MAX V device family.

Table 3 3. Programming/Erasure Specifications for MAX V Devices

Parameter	Block	Minimum	Typical	Maximum	Unit
Erase and reprogram cycles	UFM	—	—	1000(1)	Cycles
	Configuration flash memory (CFM)	—	—	100	Cycles

Note to Table 3 3:

(1) This value applies to the commercial grade devices. For the industrial grade devices, the value is 100 cycles.

DC Electrical Characteristics

Table 3 4 lists DC electrical characteristics for the MAX V device family.

Table 3 4. DC Electrical Characteristics for MAX V Devices (Note 1) (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	V_I = V_{CCIO} max to 0 V (2)	–10	—	10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = V_{CCIO} max to 0 V (2)	–10	—	10	µA
$I_{CCSTANDBY}$	V_{CCINT} supply current (standby) (3)	5M40Z, 5M80Z, 5M160Z, and 5M240Z (Commercial grade) (4), (5)	—	25	90	µA
		5M240Z (Commercial grade) (6)	—	27	96	µA
		5M40Z, 5M80Z, 5M160Z, and 5M240Z (Industrial grade) (5), (7)	—	25	139	µA
		5M240Z (Industrial grade) (6), (7)	—	27	152	µA
		5M570Z (Commercial grade) (4)	—	27	96	µA
		5M570Z (Industrial grade) (7)	—	27	152	µA
		5M1270Z and 5M2210Z	—	2	—	mA
$V_{SCHMITT}$ (8)	Hysteresis for Schmitt trigger input (9)	V_{CCIO} = 3.3 V	—	400	—	mV
		V_{CCIO} = 2.5 V	—	190	—	mV
$I_{CCPOWERUP}$	V_{CCINT} supply current during power-up (10)	MAX V devices	—	—	40	mA
R_{PULLUP}	Value of I/O pin pull-up resistor during user mode and ISP	V_{CCIO} = 3.3 V (11)	5	—	25	k:
		V_{CCIO} = 2.5 V (11)	10	—	40	k:
		V_{CCIO} = 1.8 V (11)	25	—	60	k:
		V_{CCIO} = 1.5 V (11)	45	—	95	k:
		V_{CCIO} = 1.2 V (11)	80	—	130	k:

Table 3 4. DC Electrical Characteristics for MAX V Devices (Note 1) (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{PULLUP}	I/O pin pull-up resistor current when I/O is unprogrammed	—	—	—	300	µA
C_{IO}	Input capacitance for user I/O pin	—	—	—	8	pF
C_{GCLK}	Input capacitance for dual-purpose GCLK/user I/O pin	—	—	—	8	pF

Notes to Table 3 4:

(1) Typical values are for T_A = 25°C, V_{CCINT} = 1.8 V and V_{CCIO} = 1.2, 1.5, 1.8, 2.5, or 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies to all V_{CCIO} settings (3.3, 2.5, 1.8, 1.5, and 1.2 V).

(3) V_I = ground, no load, and no toggling inputs.

(4) Commercial temperature ranges from 0°C to 85°C with the maximum current at 85°C.

(5) Not applicable to the T144 package of the 5M240Z device.

(6) Only applicable to the T144 package of the 5M240Z device.

(7) Industrial temperature ranges from –40°C to 100°C with the maximum current at 100°C.

(8) This value applies to commercial and industrial range devices. For extended temperature range devices, the typical $V_{SCHMITT}$ value is 300 mV for V_{CCIO} = 3.3 V and 120 mV for V_{CCIO} = 2.5 V.

(9) The TCK input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.

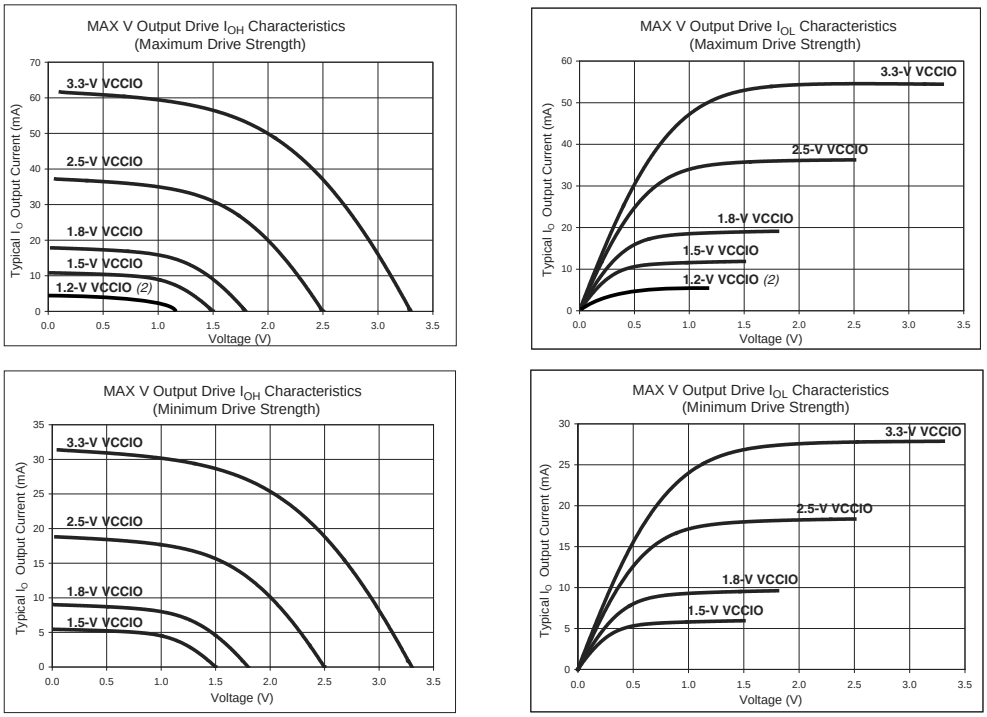
(10) This is a peak current value with a maximum duration of time.

(11) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

Output Drive Characteristics

Figure 3 1 shows the typical drive strength characteristics of MAX V devices.

Figure 3 1. Output Drive Characteristics of MAX V Devices (Note 1)



Notes to Figure 3 1:

(1) The DC output current per pin is subject to the absolute maximum rating listed in Table 3–1 on page 3–1
(2) 1.2-V V_{CCIO} is only applicable to the maximum drive strength.

I/O Standard Specifications

Table 3 5 through Table 3 13 on page 3 8 list the I/O standard specifications for the MAX V device family.

Table 3 5. 3.3-V LVTTL Specifications for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.5	0.8	V
V_{OH}	High-level output voltage	IOH = –4 mA (1)	2.4	—	V
V_{OL}	Low-level output voltage	IOL = 4 mA (1)	—	0.45	V

Note to Table 3 5:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the MAX V Device Architecture chapter.

Table 3 6. 3.3-V LVCMOS Specifications for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.5	0.8	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, IOH = –0.1 mA (1)	V_{CCIO} – 0.2	—	V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, IOL = 0.1 mA (1)	—	0.2	V

Note to Table 3 6:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard. For more information, refer to the MAX V Device Architecture chapter.

Table 3 7. 2.5-V I/O Specifications for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	IOH = –0.1 mA (1)	2.1	—	V
		IOH = –1 mA (1)	2.0	—	V
		IOH = –2 mA (1)	1.7	—	V
V_{OL}	Low-level output voltage	IOL = 0.1 mA (1)	—	0.2	V
		IOL = 1 mA (1)	—	0.4	V
		IOL = 2 mA (1)	—	0.7	V

Note to Table 3 7:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard. For more information, refer to the MAX V Device Architecture chapter.

Table 3 8. 1.8-V I/O Specifications for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.71	1.89	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	2.25 (2)	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –2 mA (1)	V_{CCIO} – 0.45	—	V
V_{OL}	Low-level output voltage	IOL = 2 mA (1)	—	0.45	V

Notes to Table 3 8:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard. For more information, refer to the MAX V Device Architecture chapter.

(2) This maximum V_{IH} reflects the JEDEC specification. The MAX V input buffer can tolerate a maximum of 4.0, as specified by the V_{I} parameter in Table 3–2 on page 3–2

Table 3 9. 1.5-V I/O Specifications for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.425	1.575	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	V_{CCIO} + 0.3 (2)	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –2 mA (1)	0.75 × V_{CCIO}	—	V
V_{OL}	Low-level output voltage	IOL = 2 mA (1)	—	0.25 × V_{CCIO}	V

Notes to Table 3 9:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard. For more information, refer to the MAX V Device Architecture chapter.

(2) This maximum V_{IH} value reflects the JEDEC specification. The MAX V input buffer can tolerate a maximum V_{IH} value of 4.0, as specified by the I_{I} parameter in Table 3–2 on page 3–2.

Table 3 10. 1.2-V I/O Specifications for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.14	1.26	V
V_{IH}	High-level input voltage	—	0.8 × V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage	—	–0.3	0.25 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –2 mA (1)	0.75 × V_{CCIO}	—	V
V_{OL}	Low-level output voltage	IOL = 2 mA (1)	—	0.25 × V_{CCIO}	V

Note to Table 3 10:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard. For more information, refer to the MAX V Device Architecture chapter.

Table 3 11. 3.3-V PCI Specifications for MAX V Devices (Note 1)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	—	0.5 × V_{CCIO}	—	V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage	—	–0.5	—	0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –500 µA	0.9 × V_{CCIO}	—	—	V
V_{OL}	Low-level output voltage	IOL = 1.5 mA	—	—	0.1 × V_{CCIO}	V

Note to Table 3 11:

(1) 3.3-V PCI I/O standard is only supported in Bank 3 of the 5M1270Z and 5M2210Z devices.

Table 3 12. LVDS Specifications for MAX V Devices (Note 1)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	2.375	2.5	2.625	V
V_{OD}	Differential output voltage swing	—	247	—	600	mV
V_{OS}	Output offset voltage	—	1.125	1.25	1.375	V

Note to Table 3 12:

(1) Supports emulated LVDS output using a three-resistor network (LVDS_E_3R).

Power Consumption

You can use the Altera® PowerPlay Early Power Estimator and PowerPlay Power Analyzer to estimate the device power.

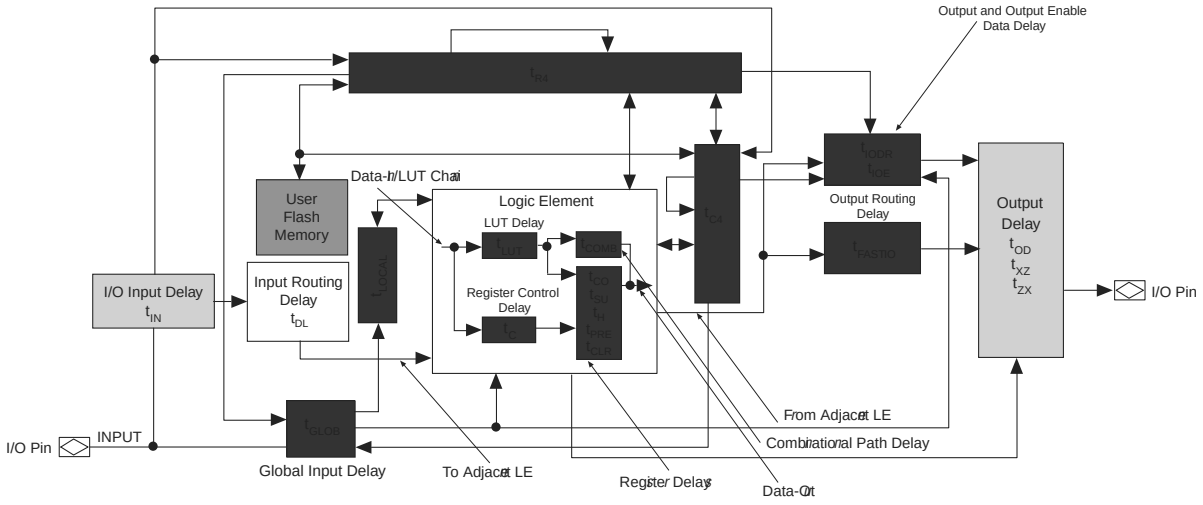
f For more information about these power analysis tools, refer to the PowerPlay Early Power Estimator for Altera CPLDs User Guide and the PowerPlay Power Analysis chapter in volume 3 of the Quartus II Handbook.

Timing Model and Specifications

MAX V devices timing can be analyzed with the Altera Quartus® II software, a variety of industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 3 2 .

MAX V devices have predictable internal delays that allow you to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 3 2. Timing Model for MAX V Devices



You can derive the timing characteristics of any signal path from the timing model and parameters of a particular device. You can calculate external timing parameters, which represent pin-to-pin timing delays, as the sum of the internal parameters.

f For more information, refer to AN629: Understanding Timing in Altera CPLDs

Table 3 17. Device Performance for MAX V Devices (Part 2 of 2)

Resource Used	Design Size and Function	Resources Used			Performance				Unit
					5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z		5M1270Z/ 5M2210Z		
		Mode	LEs	UFM Blocks	C4	C5, I5	C4	C5, I5	
UFM	512 × 16	None	3	1	10.0	10.0	10.0	10.0	MHz
	512 × 16	SPI (2)	37	1	9.7	9.7	8.0	8.0	MHz
	512 × 8	Parallel (3)	73	1	(4)	(4)	(4)	(4)	MHz
	512 × 16	I²C (3)	142	1	100 (5)	100 (5)	100 (5)	100 (5)	kHz

Notes to Table 3 17:

(1) This design is a binary loadable up counter.
(2) This design is configured for read-only operation in Extended mode. Read and write ability increases the number of LEs used.
(3) This design is configured for read-only operation. Read and write ability increases the number of LEs used.
(4) This design is asynchronous.
(5) The I²C megafunction is verified in hardware up to 100-kHz serial clock line rate.

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Table 3 18 through Table 3 25 on page 3 19 list the MAX V device internal timing microparameters for LEs, input/output elements (IOEs), UFM blocks, and MultiTrack interconnects.

f For more information about each internal timing microparameters symbol, refer to AN629: Understanding Timing in Altera CPLDs

Table 3 18. LE Internal Timing Microparameters for MAX V Devices (Part 1 of 2)

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{LUT}	LE combinational look-up table (LUT) delay	—	1,215	—	2,247	—	742	—	914	ps
t_{COMB}	Combinational path delay	—	243	—	309	—	192	—	236	ps
t_{CLR}	LE register clear delay	401	—	545	—	309	—	381	—	ps
t_{PRE}	LE register preset delay	401	—	545	—	309	—	381	—	ps
t_{SU}	LE register setup time before clock	260	—	321	—	271	—	333	—	ps
t_{H}	LE register hold time after clock	0	—	0	—	0	—	0	—	ps
t_{CO}	LE register clock-to-output delay	—	380	—	494	—	305	—	376	ps

Table 3 18. LE Internal Timing Microparameters for MAX V Devices (Part 2 of 2)

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CLKHL}	Minimum clock high or low time	253	—	339	—	216	—	266	—	ps
t_C	Register control delay	—	1,356	—	1,741	—	1,114	—	1,372	ps

Table 3 19. IOE Internal Timing Microparameters for MAX V Devices

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{FASTIO}	Data output delay from adjacent LE to I/O block	—	170	—	428	—	207	—	254	ps
t_{IN}	I/O input pad and buffer delay	—	907	—	986	—	920	—	1,132	ps
t_{GLOB}(1)	I/O input pad and buffer delay used as global signal pin	—	2,261	—	3,322	—	1,974	—	2,430	ps
t_{IOE}	Internally generated output enable delay	—	530	—	1,410	—	374	—	460	ps
t_{DL}	Input routing delay	—	318	—	509	—	291	—	358	ps
t_{OD} (2)	Output delay buffer and pad delay	—	1,319	—	1,543	—	1,383	—	1,702	ps
t_{XZ} (3)	Output buffer disable delay	—	1,045	—	1,276	—	982	—	1,209	ps
t_{ZX} (4)	Output buffer enable delay	—	1,160	—	1,353	—	1,303	—	1,604	ps

Notes to Table 3 19:

(1) Delay numbers for t_{GLOB} differ for each device density and speed grade. The delay numbers for t_{GLOB} shown in Table 3–19 are based on a 5M240Z device target.

MiMice d0.86.6(t)9.7(del.0291 Tw m0 7)]TJ54 T4,82 —TwL Tw(o)-5.8(212 TDa 5M)3.4(240)20.5(Z 7)]2 T64,buffy n8 0 t (D)26.5(m Tt)17.0 0 0 t33(

Table 3–18. LE Internal Timing Microparameters for MAX V Devices (Part 2 of 2)

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CLKHL}	Minimum clock high or low time	253	—	339	—	216	—	266	—	ps
t_{C}	Register control delay	—	1,356	—	1,741	—	1,114	—	1,372	ps

Table 3–19. IOE Internal Timing Microparameters for MAX V Devices

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{FASTIO}	Data output delay from adjacent LE to I/O block	—	170	—	428	—	207	—	254	ps
t_{IN}	I/O input pad and buffer delay	—	907	—	986	—	920	—	1,132	ps
t_{GLOB} *(1)*	I/O input pad and buffer delay used as global signal pin	—	2,261	—	3,322	—	1,974	—	2,430	ps
t_{IOE}	Internally generated output enable delay	—	530	—	1,410	—	374	—	460	ps
t_{DL}	Input routing delay	—	318	—	509	—	291	—	358	ps
t_{OD} *(2)*	Output delay buffer and pad delay	—	1,319	—	1,543	—	1,383	—	1,702	ps
t_{XZ} *(3)*	Output buffer disable delay	—	1,045	—	1,276	—	982	—	1,209	ps
t_{ZX} *(4)*	Output buffer enable delay	—	1,160	—	1,353	—	1,303	—	1,604	ps

Notes to Table 3–19:

(1) Delay numbers for t_{GLOB} differ for each device density and speed grade. The delay numbers for t_{GLOB}, shown in Table 3–19, are based on a 5M240Z device target.

(2) For more information about delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3–34 on page 3–24 and Table 3–35 on page 3–25.

(3) For more information about t_{XZ} delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3–22 on page 3–15 and Table 3–23 on page 3–15.

(4) For more information about t_{ZX} delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3–20 on page 3–14 and Table 3–21 on page 3–14.