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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	1.71V ~ 1.89V
Number of Logic Elements/Blocks	160
Number of Macrocells	128
Number of Gates	-
Number of I/O	54
Operating Temperature	0°C ~ 85°C (TJ)
Mounting Type	Surface Mount
Package / Case	64-TQFP Exposed Pad
Supplier Device Package	64-EQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5m160ze64c4n">https://www.e-xfl.com/product-detail/intel/5m160ze64c4n</a>

## Programming/Erase Specifications

Table 3–3 lists the programming/erase specifications for the MAX V device family.

**Table 3–3. Programming/Erase Specifications for MAX V Devices**

Parameter	Block	Minimum	Typical	Maximum	Unit
Erase and reprogram cycles	UFM	—	—	1000 (1)	Cycles
	Configuration flash memory (CFM)	—	—	100	Cycles

**Note to Table 3–3:**

(1) This value applies to the commercial grade devices. For the industrial grade devices, the value is 100 cycles.

## DC Electrical Characteristics

Table 3–4 lists DC electrical characteristics for the MAX V device family.

**Table 3–4. DC Electrical Characteristics for MAX V Devices (Note 1) (Part 1 of 2)**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$I_I$	Input pin leakage current	$V_I = V_{CCIO}$ max to 0 V (2)	–10	—	10	$\mu$ A
$I_{OZ}$	Tri-stated I/O pin leakage current	$V_O = V_{CCIO}$ max to 0 V (2)	–10	—	10	$\mu$ A
$I_{CCSTANDBY}$	$V_{CCINT}$ supply current (standby) (3)	5M40Z, 5M80Z, 5M160Z, and 5M240Z (Commercial grade) (4), (5)	—	25	90	$\mu$ A
		5M240Z (Commercial grade) (6)	—	27	96	$\mu$ A
		5M40Z, 5M80Z, 5M160Z, and 5M240Z (Industrial grade) (5), (7)	—	25	139	$\mu$ A
		5M240Z (Industrial grade) (6)	—	27	152	$\mu$ A
		5M570Z (Commercial grade) (4)	—	27	96	$\mu$ A
		5M570Z (Industrial grade) (7)	—	27	152	$\mu$ A
		5M1270Z and 5M2210Z	—	2	—	mA
$V_{SCHMITT}$ (8)	Hysteresis for Schmitt trigger input (9)	$V_{CCIO} = 3.3$ V	—	400	—	mV
		$V_{CCIO} = 2.5$ V	—	190	—	mV
$I_{CCPOWERUP}$	$V_{CCINT}$ supply current during power-up (10)	MAX V devices	—	—	40	mA
$R_{PULLUP}$	Value of I/O pin pull-up resistor during user mode and ISP	$V_{CCIO} = 3.3$ V (11)	5	—	25	k $\Omega$
		$V_{CCIO} = 2.5$ V (11)	10	—	40	k $\Omega$
		$V_{CCIO} = 1.8$ V (11)	25	—	60	k $\Omega$
		$V_{CCIO} = 1.5$ V (11)	45	—	95	k $\Omega$
		$V_{CCIO} = 1.2$ V (11)	80	—	130	k $\Omega$

**Table 3-4. DC Electrical Characteristics for MAX V Devices (Note 1) (Part 2 of 2)**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$I_{PULLUP}$	I/O pin pull-up resistor current when I/O is unprogrammed	—	—	—	300	$\mu$ A
$C_{IO}$	Input capacitance for user I/O pin	—	—	—	8	pF
$C_{GCLK}$	Input capacitance for dual-purpose GCLK/user I/O pin	—	—	—	8	pF

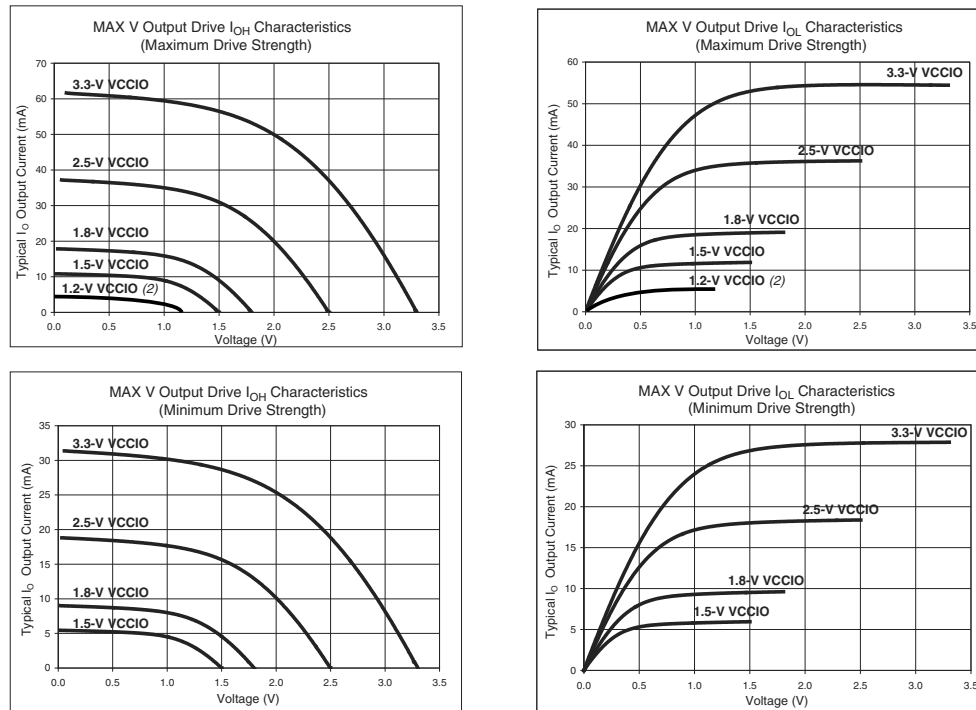
**Notes to Table 3-4:**

- (1) Typical values are for  $T_A = 25^\circ\text{C}$ ,  $V_{CCINT} = 1.8\text{ V}$  and  $V_{CCIO} = 1.2, 1.5, 1.8, 2.5, \text{ or } 3.3\text{ V}$ .
- (2) This value is specified for normal device operation. The value may vary during power-up. This applies to all  $V_{CCIO}$  settings (3.3, 2.5, 1.8, 1.5, and 1.2 V).
- (3)  $V_i =$  ground, no load, and no toggling inputs.
- (4) Commercial temperature ranges from  $0^\circ\text{C}$  to  $85^\circ\text{C}$  with the maximum current at  $85^\circ\text{C}$ .
- (5) Not applicable to the T144 package of the 5M240Z device.
- (6) Only applicable to the T144 package of the 5M240Z device.
- (7) Industrial temperature ranges from  $-40^\circ\text{C}$  to  $100^\circ\text{C}$  with the maximum current at  $100^\circ\text{C}$ .
- (8) This value applies to commercial and industrial range devices. For extended temperature range devices, the  $V_{SCHMITT}$  typical value is 300 mV for  $V_{CCIO} = 3.3\text{ V}$  and 120 mV for  $V_{CCIO} = 2.5\text{ V}$ .
- (9) The  $T_{CK}$  input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.
- (10) This is a peak current value with a maximum duration of  $t_{CONFIG}$  time.
- (11) Pin pull-up resistance values will lower if an external source drives the pin higher than  $V_{CCIO}$ .

## Output Drive Characteristics

Figure 3-1 shows the typical drive strength characteristics of MAX V devices.

**Figure 3-1. Output Drive Characteristics of MAX V Devices (Note 1)**



**Notes to Figure 3-1:**

- (1) The DC output current per pin is subject to the absolute maximum rating of Table 3-1 on page 3-1.
- (2) 1.2-V  $V_{CCIO}$  is only applicable to the maximum drive strength.

## I/O Standard Specifications

Table 3-5 through Table 3-13 on page 3-8 list the I/O standard specifications for the MAX V device family.

**Table 3-5. 3.3-V LVTTTL Specifications for MAX V Devices**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	I/O supply voltage	—	3.0	3.6	V
$V_{IH}$	High-level input voltage	—	1.7	4.0	V
$V_{IL}$	Low-level input voltage	—	-0.5	0.8	V
$V_{OH}$	High-level output voltage	$I_{OH} = -4$ mA (1)	2.4	—	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 4$ mA (1)	—	0.45	V

**Note to Table 3-5:**

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the MAX V Device Architecture chapter.

**Table 3-6. 3.3-V LVCMOS Specifications for MAX V Devices**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	I/O supply voltage	—	3.0	3.6	V
$V_{IH}$	High-level input voltage	—	1.7	4.0	V
$V_{IL}$	Low-level input voltage	—	-0.5	0.8	V
$V_{OH}$	High-level output voltage	$V_{CCIO} = 3.0$ , $IOH = -0.1 \text{ mA}$ (1)	$V_{CCIO} - 0.2$	—	V
$V_{OL}$	Low-level output voltage	$V_{CCIO} = 3.0$ , $IOL = 0.1 \text{ mA}$ (1)	—	0.2	V

**Note to Table 3-6:**

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

**Table 3-7. 2.5-V I/O Specifications for MAX V Devices**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	I/O supply voltage	—	2.375	2.625	V
$V_{IH}$	High-level input voltage	—	1.7	4.0	V
$V_{IL}$	Low-level input voltage	—	-0.5	0.7	V
$V_{OH}$	High-level output voltage	$IOH = -0.1 \text{ mA}$ (1)	2.1	—	V
		$IOH = -1 \text{ mA}$ (1)	2.0	—	V
		$IOH = -2 \text{ mA}$ (1)	1.7	—	V
$V_{OL}$	Low-level output voltage	$IOL = 0.1 \text{ mA}$ (1)	—	0.2	V
		$IOL = 1 \text{ mA}$ (1)	—	0.4	V
		$IOL = 2 \text{ mA}$ (1)	—	0.7	V

**Note to Table 3-7:**

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

**Table 3-8. 1.8-V I/O Specifications for MAX V Devices**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	I/O supply voltage	—	1.71	1.89	V
$V_{IH}$	High-level input voltage	—	$0.65 \times V_{CCIO}$	2.25 (2)	V
$V_{IL}$	Low-level input voltage	—	-0.3	$0.35 \times V_{CCIO}$	V
$V_{OH}$	High-level output voltage	$IOH = -2 \text{ mA}$ (1)	$V_{CCIO} - 0.45$	—	V
$V_{OL}$	Low-level output voltage	$IOL = 2 \text{ mA}$ (1)	—	0.45	V

**Notes to Table 3-8:**

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.
- (2) This maximum  $V_{IH}$  reflects the JEDEC specification. The MAX V input buffer can tolerate a  $V_{IH}$  maximum of 4.0, as specified by the  $V_I$  parameter in Table 3-2 on page 3-2.

## Power-Up Timing

Table 3-15 lists the power-up timing characteristics for the MAX V device family.

**Table 3-15. Power-Up Timing for MAX V Devices**

Symbol	Parameter	Device	Temperature Range	Min	Typ	Max	Unit
$t_{\text{CONFIG}}$	The amount of time from when minimum $V_{\text{CCINT}}$ is reached until the device enters user mode (1)	5M40Z	Commercial and industrial	—	—	200	$\mu\text{s}$
			Extended	—	—	300	$\mu\text{s}$
		5M80Z	Commercial and industrial	—	—	200	$\mu\text{s}$
			Extended	—	—	300	$\mu\text{s}$
		5M160Z	Commercial and industrial	—	—	200	$\mu\text{s}$
			Extended	—	—	300	$\mu\text{s}$
		5M240Z (2)	Commercial and industrial	—	—	200	$\mu\text{s}$
			Extended	—	—	300	$\mu\text{s}$
		5M240Z (3)	Commercial and industrial	—	—	300	$\mu\text{s}$
			Extended	—	—	400	$\mu\text{s}$
		5M570Z	Commercial and industrial	—	—	300	$\mu\text{s}$
			Extended	—	—	400	$\mu\text{s}$
		5M1270Z (4)	Commercial and industrial	—	—	300	$\mu\text{s}$
			Extended	—	—	400	$\mu\text{s}$
		5M1270Z (5)	Commercial and industrial	—	—	450	$\mu\text{s}$
			Extended	—	—	500	$\mu\text{s}$
		5M2210Z	Commercial and industrial	—	—	450	$\mu\text{s}$
			Extended	—	—	500	$\mu\text{s}$

**Notes to Table 3-15:**

- (1) For more information about power-on reset (POR) trigger voltage, refer to the *Hot Socketing and Power-On Reset in MAX V Devices* chapter.
- (2) Not applicable to the T144 package of the 5M240Z device.
- (3) Only applicable to the T144 package of the 5M240Z device.
- (4) Not applicable to the F324 package of the 5M1270Z device.
- (5) Only applicable to the F324 package of the 5M1270Z device.

## Preliminary and Final Timing

This section describes the performance, internal, external, and UFM timing specifications. All specifications are representative of the worst-case supply voltage and junction temperature conditions.

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 3–16 lists the status of the MAX V device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under the worst-case voltage and junction temperature conditions.

**Table 3–16. Timing Model Status for MAX V Devices**

Device	Final
5M40Z	✓
5M80Z	✓
5M160Z	✓
5M240Z	✓
5M570Z	✓
5M1270Z	✓
5M2210Z	✓

## Performance

Table 3–17 lists the MAX V device performance for some common designs. All performance values were obtained with the Quartus II software compilation of megafunctions.

**Table 3–17. Device Performance for MAX V Devices (Part 1 of 2)**

Resource Used	Design Size and Function	Resources Used			Performance				Unit
					5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z		5M1270Z/ 5M2210Z		
		Mode	LEs	UFM Blocks	C4	C5, I5	C4	C5, I5	
LE	16-bit counter (1)	—	16	0	184.1	118.3	247.5	201.1	MHz
	64-bit counter (1)	—	64	0	83.2	80.5	154.8	125.8	MHz
	16-to-1 multiplexer	—	11	0	17.4	20.4	8.0	9.3	ns
	32-to-1 multiplexer	—	24	0	12.5	25.3	9.0	11.4	ns
	16-bit XOR function	—	5	0	9.0	16.1	6.6	8.2	ns
	16-bit decoder with single address line	—	5	0	9.2	16.1	6.6	8.2	ns

**Table 3-17. Device Performance for MAX V Devices (Part 2 of 2)**

Resource Used	Design Size and Function	Resources Used			Performance				Unit
					5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z		5M1270Z/ 5M2210Z		
		Mode	LEs	UFM Blocks	C4	C5, I5	C4	C5, I5	
UFM	512 × 16	None	3	1	10.0	10.0	10.0	10.0	MHz
	512 × 16	SPI (2)	37	1	9.7	9.7	8.0	8.0	MHz
	512 × 8	Parallel (3)	73	1	(4)	(4)	(4)	(4)	MHz
	512 × 16	I <sup>2</sup> C (3)	142	1	100 (5)	100 (5)	100 (5)	100 (5)	kHz

**Notes to Table 3-17:**

- (1) This design is a binary loadable up counter.
- (2) This design is configured for read-only operation in Extended mode. Read and write ability increases the number of logic elements (LEs) used.
- (3) This design is configured for read-only operation. Read and write ability increases the number of LEs used.
- (4) This design is asynchronous.
- (5) The I<sup>2</sup>C megafunction is verified in hardware up to 100-kHz serial clock line rate.

## Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Table 3-18 through Table 3-25 on page 3-19 list the MAX V device internal timing microparameters for LEs, input/output elements (IOEs), UFM blocks, and MultiTrack interconnects.

 For more information about each internal timing microparameters symbol, refer to AN629: Understanding Timing in Altera CPLDs.

**Table 3-18. LE Internal Timing Microparameters for MAX V Devices (Part 1 of 2)**

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>LUT</sub>	LE combinational look-up table (LUT) delay	—	1,215	—	2,247	—	742	—	914	ps
t <sub>COMB</sub>	Combinational path delay	—	243	—	309	—	192	—	236	ps
t <sub>CLR</sub>	LE register clear delay	401	—	545	—	309	—	381	—	ps
t <sub>PRE</sub>	LE register preset delay	401	—	545	—	309	—	381	—	ps
t <sub>SU</sub>	LE register setup time before clock	260	—	321	—	271	—	333	—	ps
t <sub>H</sub>	LE register hold time after clock	0	—	0	—	0	—	0	—	ps
t <sub>CO</sub>	LE register clock-to-output delay	—	380	—	494	—	305	—	376	ps



Table 3–20 through Table 3–23 list the adder delays for  $t_{ZX}$  and  $t_{XZ}$  microparameters when using an I/O standard other than 3.3-V LVTTTL with 16 mA drive strength.

**Table 3–20.  $t_{ZX}$  IOE Microparameter Adders for Fast Slew Rate for MAX V Devices**

Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	16 mA	—	0	—	0	—	0	—	0	ps
	8 mA	—	72	—	74	—	101	—	125	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	ps
	4 mA	—	72	—	74	—	101	—	125	ps
2.5-V LVTTTL / LVCMOS	14 mA	—	126	—	127	—	155	—	191	ps
	7 mA	—	196	—	197	—	545	—	671	ps
1.8-V LVTTTL / LVCMOS	6 mA	—	608	—	610	—	721	—	888	ps
	3 mA	—	681	—	685	—	2012	—	2477	ps
1.5-V LVCMOS	4 mA	—	1162	—	1157	—	1590	—	1957	ps
	2 mA	—	1245	—	1244	—	3269	—	4024	ps
1.2-V LVCMOS	3 mA	—	1889	—	1856	—	2860	—	3520	ps
3.3-V PCI	20 mA	—	72	—	74	—	–18	—	–22	ps
LVDS	—	—	126	—	127	—	155	—	191	ps
RSDS	—	—	126	—	127	—	155	—	191	ps

**Table 3–21.  $t_{ZX}$  IOE Microparameter Adders for Slow Slew Rate for MAX V Devices**


Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	16 mA	—	5,951	—	6,063	—	6,012	—	5,743	ps
	8 mA	—	6,534	—	6,662	—	8,785	—	8,516	ps
3.3-V LVCMOS	8 mA	—	5,951	—	6,063	—	6,012	—	5,743	ps
	4 mA	—	6,534	—	6,662	—	8,785	—	8,516	ps
2.5-V LVTTTL / LVCMOS	14 mA	—	9,110	—	9,237	—	10,072	—	9,803	ps
	7 mA	—	9,830	—	9,977	—	12,945	—	12,676	ps
1.8-V LVTTTL / LVCMOS	6 mA	—	21,800	—	21,787	—	21,185	—	20,916	ps
	3 mA	—	23,020	—	23,037	—	24,597	—	24,328	ps
1.5-V LVCMOS	4 mA	—	39,120	—	39,067	—	34,517	—	34,248	ps
	2 mA	—	40,670	—	40,617	—	39,717	—	39,448	ps
1.2-V LVCMOS	3 mA	—	69,505	—	70,461	—	55,800	—	55,531	ps
3.3-V PCI	20 mA	—	6,534	—	6,662	—	35	—	44	ps

**Table 3–22.  $t_{xz}$  IOE Microparameter Adders for Fast Slew Rate for MAX V Devices**

Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	16 mA	—	0	—	0	—	0	—	0	ps
	8 mA	—	-69	—	-69	—	-74	—	-91	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	ps
	4 mA	—	-69	—	-69	—	-74	—	-91	ps
2.5-V LVTTTL / LVCMOS	14 mA	—	-7	—	-10	—	-46	—	-56	ps
	7 mA	—	-66	—	-69	—	-82	—	-101	ps
1.8-V LVTTTL / LVCMOS	6 mA	—	45	—	37	—	-7	—	-8	ps
	3 mA	—	34	—	25	—	119	—	147	ps
1.5-V LVCMOS	4 mA	—	166	—	155	—	339	—	418	ps
	2 mA	—	190	—	179	—	464	—	571	ps
1.2-V LVCMOS	3 mA	—	300	—	283	—	817	—	1,006	ps
3.3-V PCI	20 mA	—	-69	—	-69	—	80	—	99	ps
LVDS	—	—	-7	—	-10	—	-46	—	-56	ps
RSDS	—	—	-7	—	-10	—	-46	—	-56	ps

**Table 3–23.  $t_{xz}$  IOE Microparameter Adders for Slow Slew Rate for MAX V Devices**

Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	16 mA	—	171	—	174	—	73	—	-132	ps
	8 mA	—	112	—	116	—	758	—	553	ps
3.3-V LVCMOS	8 mA	—	171	—	174	—	73	—	-132	ps
	4 mA	—	112	—	116	—	758	—	553	ps
2.5-V LVTTTL / LVCMOS	14 mA	—	213	—	213	—	32	—	-173	ps
	7 mA	—	166	—	166	—	714	—	509	ps
1.8-V LVTTTL / LVCMOS	6 mA	—	441	—	438	—	96	—	-109	ps
	3 mA	—	496	—	494	—	963	—	758	ps
1.5-V LVCMOS	4 mA	—	765	—	755	—	238	—	33	ps
	2 mA	—	903	—	897	—	1,319	—	1,114	ps
1.2-V LVCMOS	3 mA	—	1,159	—	1,130	—	400	—	195	ps
3.3-V PCI	20 mA	—	112	—	116	—	303	—	373	ps

 The default slew rate setting for MAX V devices in the Quartus II design software is “fast”.

**Table 3-24. UFM Block Internal Timing Microparameters for MAX V Devices (Part 1 of 2)**

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{ACLK}$	Address register clock period	100	—	100	—	100	—	100	—	ns
$t_{ASU}$	Address register shift signal setup to address register clock	20	—	20	—	20	—	20	—	ns
$t_{AH}$	Address register shift signal hold to address register clock	20	—	20	—	20	—	20	—	ns
$t_{ADS}$	Address register data in setup to address register clock	20	—	20	—	20	—	20	—	ns
$t_{ADH}$	Address register data in hold from address register clock	20	—	20	—	20	—	20	—	ns
$t_{DCLK}$	Data register clock period	100	—	100	—	100	—	100	—	ns
$t_{DSS}$	Data register shift signal setup to data register clock	60	—	60	—	60	—	60	—	ns
$t_{DSH}$	Data register shift signal hold from data register clock	20	—	20	—	20	—	20	—	ns
$t_{DDS}$	Data register data in setup to data register clock	20	—	20	—	20	—	20	—	ns
$t_{DDH}$	Data register data in hold from data register clock	20	—	20	—	20	—	20	—	ns
$t_{DP}$	Program signal to data clock hold time	0	—	0	—	0	—	0	—	ns
$t_{PB}$	Maximum delay between program rising edge to UFM <i>busy</i> signal rising edge	—	960	—	960	—	960	—	960	ns
$t_{BP}$	Minimum delay allowed from UFM <i>busy</i> signal going low to program signal going low	20	—	20	—	20	—	20	—	ns
$t_{PPMX}$	Maximum length of <i>busy</i> pulse during a program	—	100	—	100	—	100	—	100	μs

**Table 3-24. UFM Block Internal Timing Microparameters for MAX V Devices (Part 2 of 2)**

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{AE}$	Minimum erase signal to address clock hold time	0	—	0	—	0	—	0	—	ns
$t_{EB}$	Maximum delay between the erase rising edge to the UFM busy signal rising edge	—	960	—	960	—	960	—	960	ns
$t_{BE}$	Minimum delay allowed from the UFM busy signal going low to erase signal going low	20	—	20	—	20	—	20	—	ns
$t_{EPMX}$	Maximum length of busy pulse during an erase	—	500	—	500	—	500	—	500	ms
$t_{DCO}$	Delay from data register clock to data register output	—	5	—	5	—	5	—	5	ns
$t_{OE}$	Delay from OSC_ENA signal reaching UFM to rising clock of osc leaving the UFM	180	—	180	—	180	—	180	—	ns
$t_{RA}$	Maximum read access time	—	65	—	65	—	65	—	65	ns
$t_{OSCS}$	Maximum delay between the OSC_ENA rising edge to the erase/program signal rising edge	250	—	250	—	250	—	250	—	ns
$t_{OSCH}$	Minimum delay allowed from the erase/program signal going low to OSC_ENA signal going low	250	—	250	—	250	—	250	—	ns

Table 3–26 lists the external I/O timing parameters for the 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices.

**Table 3–26. Global Clock External I/O Timing Parameters for the 5M40Z, 5M80Z, 5M160Z, and 5M240Z Devices (Note 1), (2)**

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
$t_{PD1}$	Worst case pin-to-pin delay through one LUT	10 pF	—	7.9	—	14.0	ns
$t_{PD2}$	Best case pin-to-pin delay through one LUT	10 pF	—	5.8	—	8.5	ns
$t_{SU}$	Global clock setup time	—	2.4	—	4.6	—	ns
$t_H$	Global clock hold time	—	0	—	0	—	ns
$t_{CO}$	Global clock to output delay	10 pF	2.0	6.6	2.0	8.6	ns
$t_{CH}$	Global clock high time	—	253	—	339	—	ps
$t_{CL}$	Global clock low time	—	253	—	339	—	ps
$t_{CNT}$	Minimum global clock period for 16-bit counter	—	5.4	—	8.4	—	ns
$f_{CNT}$	Maximum global clock frequency for 16-bit counter	—	—	184.1	—	118.3	MHz

**Notes to Table 3–26:**

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.
- (2) Not applicable to the T144 package of the 5M240Z device.

Table 3–27 lists the external I/O timing parameters for the T144 package of the 5M240Z device.

**Table 3–27. Global Clock External I/O Timing Parameters for the 5M240Z Device (Note 1), (2)**

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
$t_{PD1}$	Worst case pin-to-pin delay through one LUT	10 pF	—	9.5	—	17.7	ns
$t_{PD2}$	Best case pin-to-pin delay through one LUT	10 pF	—	5.7	—	8.5	ns
$t_{SU}$	Global clock setup time	—	2.2	—	4.4	—	ns
$t_H$	Global clock hold time	—	0	—	0	—	ns
$t_{CO}$	Global clock to output delay	10 pF	2.0	6.7	2.0	8.7	ns
$t_{CH}$	Global clock high time	—	253	—	339	—	ps
$t_{CL}$	Global clock low time	—	253	—	339	—	ps
$t_{CNT}$	Minimum global clock period for 16-bit counter	—	5.4	—	8.4	—	ns
$f_{CNT}$	Maximum global clock frequency for 16-bit counter	—	—	184.1	—	118.3	MHz

**Notes to Table 3–27:**

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.
- (2) Only applicable to the T144 package of the 5M240Z device.

Table 3–28 lists the external I/O timing parameters for the 5M570Z device.

**Table 3–28. Global Clock External I/O Timing Parameters for the 5M570Z Device (Note 1)**

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
$t_{PD1}$	Worst case pin-to-pin delay through one LUT	10 pF	—	9.5	—	17.7	ns
$t_{PD2}$	Best case pin-to-pin delay through one LUT	10 pF	—	5.7	—	8.5	ns
$t_{SU}$	Global clock setup time	—	2.2	—	4.4	—	ns
$t_H$	Global clock hold time	—	0	—	0	—	ns
$t_{CO}$	Global clock to output delay	10 pF	2.0	6.7	2.0	8.7	ns
$t_{CH}$	Global clock high time	—	253	—	339	—	ps
$t_{CL}$	Global clock low time	—	253	—	339	—	ps
$t_{CNT}$	Minimum global clock period for 16-bit counter	—	5.4	—	8.4	—	ns
$f_{CNT}$	Maximum global clock frequency for 16-bit counter	—	—	184.1	—	118.3	MHz

**Note to Table 3–28:**

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 3–29 lists the external I/O timing parameters for the 5M1270Z device.

**Table 3–29. Global Clock External I/O Timing Parameters for the 5M1270Z Device (Note 1), (2)**

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
$t_{PD1}$	Worst case pin-to-pin delay through one LUT	10 pF	—	8.1	—	10.0	ns
$t_{PD2}$	Best case pin-to-pin delay through one LUT	10 pF	—	4.8	—	5.9	ns
$t_{SU}$	Global clock setup time	—	1.5	—	1.9	—	ns
$t_H$	Global clock hold time	—	0	—	0	—	ns
$t_{CO}$	Global clock to output delay	10 pF	2.0	5.9	2.0	7.3	ns
$t_{CH}$	Global clock high time	—	216	—	266	—	ps
$t_{CL}$	Global clock low time	—	216	—	266	—	ps
$t_{CNT}$	Minimum global clock period for 16-bit counter	—	4.0	—	5.0	—	ns
$f_{CNT}$	Maximum global clock frequency for 16-bit counter	—	—	247.5	—	201.1	MHz

**Notes to Table 3–29:**

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.  
 (2) Not applicable to the F324 package of the 5M1270Z device.

Table 3–30 lists the external I/O timing parameters for the F324 package of the 5M1270Z device.

**Table 3–30. Global Clock External I/O Timing Parameters for the 5M1270Z Device (Note 1), (2)**

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
$t_{PD1}$	Worst case pin-to-pin delay through one LUT	10 pF	—	9.1	—	11.2	ns
$t_{PD2}$	Best case pin-to-pin delay through one LUT	10 pF	—	4.8	—	5.9	ns
$t_{SU}$	Global clock setup time	—	1.5	—	1.9	—	ns
$t_H$	Global clock hold time	—	0	—	0	—	ns
$t_{CO}$	Global clock to output delay	10 pF	2.0	6.0	2.0	7.4	ns
$t_{CH}$	Global clock high time	—	216	—	266	—	ps
$t_{CL}$	Global clock low time	—	216	—	266	—	ps
$t_{CNT}$	Minimum global clock period for 16-bit counter	—	4.0	—	5.0	—	ns
$f_{CNT}$	Maximum global clock frequency for 16-bit counter	—	—	247.5	—	201.1	MHz

**Notes to Table 3–30:**

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.
- (2) Only applicable to the F324 package of the 5M1270Z device.

Table 3–31 lists the external I/O timing parameters for the 5M2210Z device.

**Table 3–31. Global Clock External I/O Timing Parameters for the 5M2210Z Device (Note 1)**

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
$t_{PD1}$	Worst case pin-to-pin delay through one LUT	10 pF	—	9.1	—	11.2	ns
$t_{PD2}$	Best case pin-to-pin delay through one LUT	10 pF	—	4.8	—	5.9	ns
$t_{SU}$	Global clock setup time	—	1.5	—	1.9	—	ns
$t_H$	Global clock hold time	—	0	—	0	—	ns
$t_{CO}$	Global clock to output delay	10 pF	2.0	6.0	2.0	7.4	ns
$t_{CH}$	Global clock high time	—	216	—	266	—	ps
$t_{CL}$	Global clock low time	—	216	—	266	—	ps
$t_{CNT}$	Minimum global clock period for 16-bit counter	—	4.0	—	5.0	—	ns
$f_{CNT}$	Maximum global clock frequency for 16-bit counter	—	—	247.5	—	201.1	MHz

**Note to Table 3–31:**

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

## External Timing I/O Delay Adders

The I/O delay timing parameters for the I/O standard input and output adders and the input delays are specified by speed grade, independent of device density.

Table 3–32 through Table 3–36 on page 3–25 list the adder delays associated with I/O pins for all packages. If you select an I/O standard other than 3.3-V LVTTTL, add the input delay adder to the external  $t_{SU}$  timing parameters listed in Table 3–26 on page 3–20 through Table 3–31. If you select an I/O standard other than 3.3-V LVTTTL with 16 mA drive strength and fast slew rate, add the output delay adder to the external  $t_{CO}$  and  $t_{PD}$  listed in Table 3–26 on page 3–20 through Table 3–31.

**Table 3–32. External Timing Input Delay Adders for MAX V Devices**

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	480	—	591	ps
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	480	—	591	ps
2.5-V LVTTTL / LVCMOS	Without Schmitt Trigger	—	42	—	42	—	246	—	303	ps
	With Schmitt Trigger	—	429	—	483	—	787	—	968	ps
1.8-V LVTTTL / LVCMOS	Without Schmitt Trigger	—	378	—	368	—	695	—	855	ps
1.5-V LVCMOS	Without Schmitt Trigger	—	681	—	658	—	1,334	—	1,642	ps
1.2-V LVCMOS	Without Schmitt Trigger	—	1,055	—	1,010	—	2,324	—	2,860	ps
3.3-V PCI	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps

**Table 3–33. External Timing Input Delay  $t_{GLOB}$  Adders for GCLK Pins for MAX V Devices (Part 1 of 2)**

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	400	—	493	ps



**Table 3-33. External Timing Input Delay  $t_{GLOB}$  Adders for GCLK Pins for MAX V Devices (Part 2 of 2)**

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	400	—	493	ps
2.5-V LVTTTL / LVCMOS	Without Schmitt Trigger	—	242	—	242	—	287	—	353	ps
	With Schmitt Trigger	—	429	—	483	—	550	—	677	ps
1.8-V LVTTTL / LVCMOS	Without Schmitt Trigger	—	378	—	368	—	459	—	565	ps
1.5-V LVCMOS	Without Schmitt Trigger	—	681	—	658	—	1,111	—	1,368	ps
1.2-V LVCMOS	Without Schmitt Trigger	—	1,055	—	1,010	—	2,067	—	2,544	ps
3.3-V PCI	Without Schmitt Trigger	—	0	—	0	—	7	—	9	ps

**Table 3-34. External Timing Output Delay and  $t_{OD}$  Adders for Fast Slew Rate for MAX V Devices**

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	16 mA	—	0	—	0	—	0	—	0	ps
	8 mA	—	39	—	58	—	84	—	104	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	ps
	4 mA	—	39	—	58	—	84	—	104	ps
2.5-V LVTTTL / LVCMOS	14 mA	—	122	—	129	—	158	—	195	ps
	7 mA	—	196	—	188	—	251	—	309	ps
1.8-V LVTTTL / LVCMOS	6 mA	—	624	—	624	—	738	—	909	ps
	3 mA	—	686	—	694	—	850	—	1,046	ps
1.5-V LVCMOS	4 mA	—	1,188	—	1,184	—	1,376	—	1,694	ps
	2 mA	—	1,279	—	1,280	—	1,517	—	1,867	ps
1.2-V LVCMOS	3 mA	—	1,911	—	1,883	—	2,206	—	2,715	ps
3.3-V PCI	20 mA	—	39	—	58	—	4	—	5	ps
LVDS	—	—	122	—	129	—	158	—	195	ps
RSDS	—	—	122	—	129	—	158	—	195	ps

**Table 3-35. External Timing Output Delay and  $t_{OD}$  Adders for Slow Slew Rate for MAX V Devices**

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	16 mA	—	5,913	—	6,043	—	6,612	—	6,293	ps
	8 mA	—	6,488	—	6,645	—	7,313	—	6,994	ps
3.3-V LVCMOS	8 mA	—	5,913	—	6,043	—	6,612	—	6,293	ps
	4 mA	—	6,488	—	6,645	—	7,313	—	6,994	ps
2.5-V LVTTTL / LVCMOS	14 mA	—	9,088	—	9,222	—	10,021	—	9,702	ps
	7 mA	—	9,808	—	9,962	—	10,881	—	10,562	ps
1.8-V LVTTTL / LVCMOS	6 mA	—	21,758	—	21,782	—	21,134	—	20,815	ps
	3 mA	—	23,028	—	23,032	—	22,399	—	22,080	ps
1.5-V LVCMOS	4 mA	—	39,068	—	39,032	—	34,499	—	34,180	ps
	2 mA	—	40,578	—	40,542	—	36,281	—	35,962	ps
1.2-V LVCMOS	3 mA	—	69,332	—	70,257	—	55,796	—	55,477	ps
3.3-V PCI	20 mA	—	6,488	—	6,645	—	339	—	418	ps

**Table 3-36. IOE Programmable Delays for MAX V Devices**

Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
	C4		C5, I5		C4		C5, I5		
	Min	Max	Min	Max	Min	Max	Min	Max	
Input Delay from Pin to Internal Cells = 1	—	1,858	—	2,214	—	1,592	—	1,960	ps
Input Delay from Pin to Internal Cells = 0	—	569	—	616	—	115	—	142	ps

## LVDS and RSDS Output Timing Specifications

Table 3–39 lists the emulated LVDS output timing specifications for MAX V devices.

**Table 3–39. Emulated LVDS Output Timing Specifications for MAX V Devices**

Parameter	Mode	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z/5M1270Z/ 5M2210Z		Unit
		C4, C5, I5		
		Min	Max	
Data rate (1), (2)	×10	—	304	Mbps
	×9	—	304	Mbps
	×8	—	304	Mbps
	×7	—	304	Mbps
	×6	—	304	Mbps
	×5	—	304	Mbps
	×4	—	304	Mbps
	×3	—	304	Mbps
	×2	—	304	Mbps
×1	—	304	Mbps	
t <sub>DUTY</sub>	—	45	55	%
Total jitter (3)	—	—	0.2	UI
t <sub>RISE</sub>	—	—	450	ps
t <sub>FALL</sub>	—	—	450	ps

**Notes to Table 3–39:**

- (1) The performance of the LVDS\_E\_3R transmitter system is limited by the lower of the two—the maximum data rate supported by LVDS\_E\_3R I/O buffer or 2x (F<sub>MAX</sub> of the ALTLVDS\_TX instance). The actual performance of your LVDS\_E\_3R transmitter system must be attained through the Quartus II timing analysis of the complete design.
- (2) For the input clock pin to achieve 304 Mbps, use I/O standard with V<sub>CCIO</sub> of 2.5 V and above.
- (3) This specification is based on external clean clock source.

Table 3–40 lists the emulated RSDS output timing specifications for MAX V devices.

**Table 3–40. Emulated RSDS Output Timing Specifications for MAX V Devices**

Parameter	Mode	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z/5M1270Z/ 5M2210Z		Unit
		C4, C5, I5		
		Min	Max	
Data rate (1)	×10	—	200	Mbps
	×9	—	200	Mbps
	×8	—	200	Mbps
	×7	—	200	Mbps
	×6	—	200	Mbps
	×5	—	200	Mbps
	×4	—	200	Mbps
	×3	—	200	Mbps
	×2	—	200	Mbps
×1	—	200	Mbps	
$t_{DUTY}$	—	45	55	%
Total jitter (2)	—	—	0.2	UI
$t_{RISE}$	—	—	450	ps
$t_{FALL}$	—	—	450	ps

**Notes to Table 3–40:**

- (1) For the input clock pin to achieve 200 Mbps, use I/O standard with  $V_{CCIO}$  of 1.8 V and above.
- (2) This specification is based on external clean clock source.

**Table 3-41. JTAG Timing Parameters for MAX V Devices (Part 2 of 2)**

Symbol	Parameter	Min	Max	Unit
$t_{JSXZ}$	Update register valid output to high impedance	—	25	ns

**Notes to Table 3-41:**

- (1) Minimum clock period specified for 10 pF load on the TDO pin. Larger loads on TDO degrades the maximum TCK frequency.
- (2) This specification is shown for 3.3-V LVTTTL/LVCMOS and 2.5-V LVTTTL/LVCMOS operation of the JTAG pins. For 1.8-V LVTTTL/LVCMOS and 1.5-V LVCMOS operation, the  $t_{JPSU}$  minimum is 6 ns and  $t_{JPC0}$ ,  $t_{JPZX}$ , and  $t_{JPXZ}$  are maximum values at 35 ns.

## Document Revision History

Table 3-42 lists the revision history for this chapter.

**Table 3-42. Document Revision History**

Date	Version	Changes
May 2011	1.2	Updated Table 3-2, Table 3-15, Table 3-16, and Table 3-33.
January 2011	1.1	Updated Table 3-37, Table 3-38, Table 3-39, and Table 3-40.
December 2010	1.0	Initial release.