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### Understanding **Embedded - CPLDs (Complex Programmable Logic Devices)**

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	1.71V ~ 1.89V
Number of Logic Elements/Blocks	80
Number of Macrocells	64
Number of Gates	-
Number of I/O	54
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	64-TQFP Exposed Pad
Supplier Device Package	64-EQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5m80ze64a5n">https://www.e-xfl.com/product-detail/intel/5m80ze64a5n</a>

## Programming/Erase Specifications

Table 3–3 lists the programming/erase specifications for the MAX V device family.

**Table 3–3. Programming/Erase Specifications for MAX V Devices**

Parameter	Block	Minimum	Typical	Maximum	Unit
Erase and reprogram cycles	UFM	—	—	1000 (1)	Cycles
	Configuration flash memory (CFM)	—	—	100	Cycles

**Note to Table 3–3:**

(1) This value applies to the commercial grade devices. For the industrial grade devices, the value is 100 cycles.

## DC Electrical Characteristics

Table 3–4 lists DC electrical characteristics for the MAX V device family.

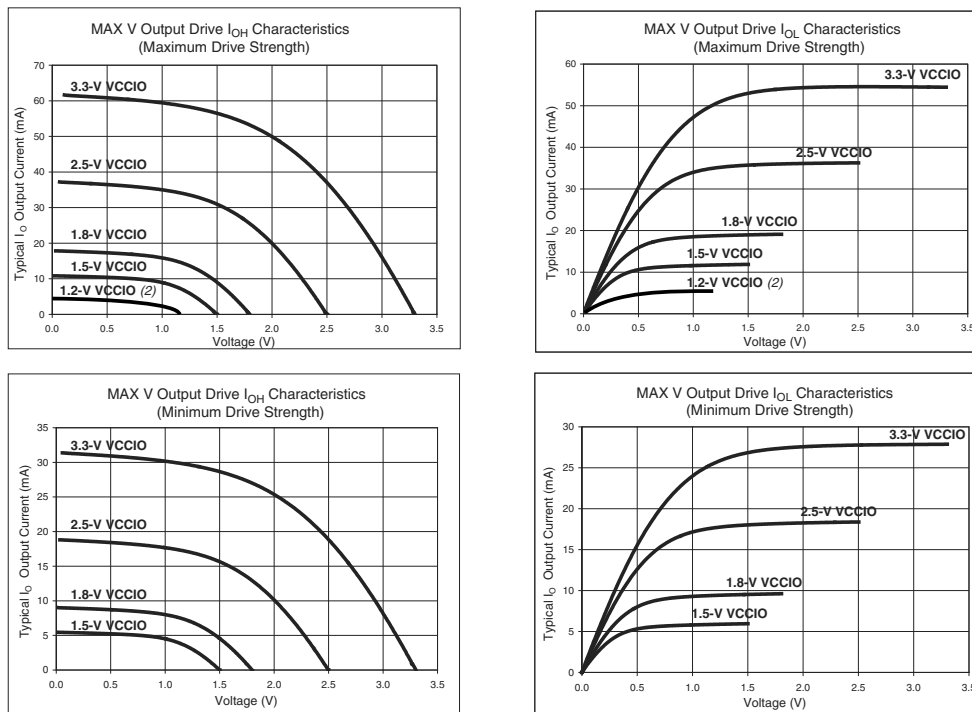
**Table 3–4. DC Electrical Characteristics for MAX V Devices (Note 1) (Part 1 of 2)**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$I_I$	Input pin leakage current	$V_I = V_{CCIO}$ max to 0 V (2)	–10	—	10	$\mu$ A
$I_{OZ}$	Tri-stated I/O pin leakage current	$V_O = V_{CCIO}$ max to 0 V (2)	–10	—	10	$\mu$ A
$I_{CCSTANDBY}$	$V_{CCINT}$ supply current (standby) (3)	5M40Z, 5M80Z, 5M160Z, and 5M240Z (Commercial grade) (4), (5)	—	25	90	$\mu$ A
		5M240Z (Commercial grade) (6)	—	27	96	$\mu$ A
		5M40Z, 5M80Z, 5M160Z, and 5M240Z (Industrial grade) (5), (7)	—	25	139	$\mu$ A
		5M240Z (Industrial grade) (6)	—	27	152	$\mu$ A
		5M570Z (Commercial grade) (4)	—	27	96	$\mu$ A
		5M570Z (Industrial grade) (7)	—	27	152	$\mu$ A
		5M1270Z and 5M2210Z	—	2	—	mA
$V_{SCHMITT}$ (8)	Hysteresis for Schmitt trigger input (9)	$V_{CCIO} = 3.3$ V	—	400	—	mV
		$V_{CCIO} = 2.5$ V	—	190	—	mV
$I_{CCPOWERUP}$	$V_{CCINT}$ supply current during power-up (10)	MAX V devices	—	—	40	mA
$R_{PULLUP}$	Value of I/O pin pull-up resistor during user mode and ISP	$V_{CCIO} = 3.3$ V (11)	5	—	25	k $\Omega$
		$V_{CCIO} = 2.5$ V (11)	10	—	40	k $\Omega$
		$V_{CCIO} = 1.8$ V (11)	25	—	60	k $\Omega$
		$V_{CCIO} = 1.5$ V (11)	45	—	95	k $\Omega$
		$V_{CCIO} = 1.2$ V (11)	80	—	130	k $\Omega$

## Output Drive Characteristics

Figure 3-1 shows the typical drive strength characteristics of MAX V devices.

**Figure 3-1. Output Drive Characteristics of MAX V Devices (Note 1)**



**Notes to Figure 3-1:**

- (1) The DC output current per pin is subject to the absolute maximum rating of Table 3-1 on page 3-1.
- (2) 1.2-V  $V_{CCIO}$  is only applicable to the maximum drive strength.

## I/O Standard Specifications

Table 3-5 through Table 3-13 on page 3-8 list the I/O standard specifications for the MAX V device family.

**Table 3-5. 3.3-V LVTTTL Specifications for MAX V Devices**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	I/O supply voltage	—	3.0	3.6	V
$V_{IH}$	High-level input voltage	—	1.7	4.0	V
$V_{IL}$	Low-level input voltage	—	-0.5	0.8	V
$V_{OH}$	High-level output voltage	$I_{OH} = -4 \text{ mA}$ (1)	2.4	—	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 4 \text{ mA}$ (1)	—	0.45	V

**Note to Table 3-5:**

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

**Table 3-6. 3.3-V LVCMOS Specifications for MAX V Devices**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	I/O supply voltage	—	3.0	3.6	V
$V_{IH}$	High-level input voltage	—	1.7	4.0	V
$V_{IL}$	Low-level input voltage	—	-0.5	0.8	V
$V_{OH}$	High-level output voltage	$V_{CCIO} = 3.0$ , $IOH = -0.1 \text{ mA}$ (1)	$V_{CCIO} - 0.2$	—	V
$V_{OL}$	Low-level output voltage	$V_{CCIO} = 3.0$ , $IOL = 0.1 \text{ mA}$ (1)	—	0.2	V

**Note to Table 3-6:**

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

**Table 3-7. 2.5-V I/O Specifications for MAX V Devices**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	I/O supply voltage	—	2.375	2.625	V
$V_{IH}$	High-level input voltage	—	1.7	4.0	V
$V_{IL}$	Low-level input voltage	—	-0.5	0.7	V
$V_{OH}$	High-level output voltage	$IOH = -0.1 \text{ mA}$ (1)	2.1	—	V
		$IOH = -1 \text{ mA}$ (1)	2.0	—	V
		$IOH = -2 \text{ mA}$ (1)	1.7	—	V
$V_{OL}$	Low-level output voltage	$IOL = 0.1 \text{ mA}$ (1)	—	0.2	V
		$IOL = 1 \text{ mA}$ (1)	—	0.4	V
		$IOL = 2 \text{ mA}$ (1)	—	0.7	V

**Note to Table 3-7:**

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

**Table 3-8. 1.8-V I/O Specifications for MAX V Devices**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	I/O supply voltage	—	1.71	1.89	V
$V_{IH}$	High-level input voltage	—	$0.65 \times V_{CCIO}$	2.25 (2)	V
$V_{IL}$	Low-level input voltage	—	-0.3	$0.35 \times V_{CCIO}$	V
$V_{OH}$	High-level output voltage	$IOH = -2 \text{ mA}$ (1)	$V_{CCIO} - 0.45$	—	V
$V_{OL}$	Low-level output voltage	$IOL = 2 \text{ mA}$ (1)	—	0.45	V

**Notes to Table 3-8:**

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.
- (2) This maximum  $V_{IH}$  reflects the JEDEC specification. The MAX V input buffer can tolerate a  $V_{IH}$  maximum of 4.0, as specified by the  $V_I$  parameter in Table 3-2 on page 3-2.

**Table 3–9. 1.5-V I/O Specifications for MAX V Devices**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	I/O supply voltage	—	1.425	1.575	V
$V_{IH}$	High-level input voltage	—	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$ (2)	V
$V_{IL}$	Low-level input voltage	—	-0.3	$0.35 \times V_{CCIO}$	V
$V_{OH}$	High-level output voltage	$IOH = -2 \text{ mA}$ (1)	$0.75 \times V_{CCIO}$	—	V
$V_{OL}$	Low-level output voltage	$IOL = 2 \text{ mA}$ (1)	—	$0.25 \times V_{CCIO}$	V

**Notes to Table 3–9:**

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.
- (2) This maximum  $V_{IH}$  reflects the JEDEC specification. The MAX V input buffer can tolerate a  $V_{IH}$  maximum of 4.0, as specified by the  $V_I$  parameter in Table 3–2 on page 3–2.

**Table 3–10. 1.2-V I/O Specifications for MAX V Devices**

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{CCIO}$	I/O supply voltage	—	1.14	1.26	V
$V_{IH}$	High-level input voltage	—	$0.8 \times V_{CCIO}$	$V_{CCIO} + 0.3$	V
$V_{IL}$	Low-level input voltage	—	-0.3	$0.25 \times V_{CCIO}$	V
$V_{OH}$	High-level output voltage	$IOH = -2 \text{ mA}$ (1)	$0.75 \times V_{CCIO}$	—	V
$V_{OL}$	Low-level output voltage	$IOL = 2 \text{ mA}$ (1)	—	$0.25 \times V_{CCIO}$	V

**Note to Table 3–10:**

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

**Table 3–11. 3.3-V PCI Specifications for MAX V Devices (Note 1)**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{CCIO}$	I/O supply voltage	—	3.0	3.3	3.6	V
$V_{IH}$	High-level input voltage	—	$0.5 \times V_{CCIO}$	—	$V_{CCIO} + 0.5$	V
$V_{IL}$	Low-level input voltage	—	-0.5	—	$0.3 \times V_{CCIO}$	V
$V_{OH}$	High-level output voltage	$IOH = -500 \mu\text{A}$	$0.9 \times V_{CCIO}$	—	—	V
$V_{OL}$	Low-level output voltage	$IOL = 1.5 \text{ mA}$	—	—	$0.1 \times V_{CCIO}$	V

**Note to Table 3–11:**

- (1) 3.3-V PCI I/O standard is only supported in Bank 3 of the 5M1270Z and 5M2210Z devices.

**Table 3–12. LVDS Specifications for MAX V Devices (Note 1)**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{CCIO}$	I/O supply voltage	—	2.375	2.5	2.625	V
$V_{OD}$	Differential output voltage swing	—	247	—	600	mV
$V_{OS}$	Output offset voltage	—	1.125	1.25	1.375	V

**Note to Table 3–12:**

- (1) Supports emulated LVDS output using a three-resistor network (LVDS\_E\_3R).

## Power-Up Timing

Table 3-15 lists the power-up timing characteristics for the MAX V device family.

**Table 3-15. Power-Up Timing for MAX V Devices**

Symbol	Parameter	Device	Temperature Range	Min	Typ	Max	Unit
$t_{\text{CONFIG}}$	The amount of time from when minimum $V_{\text{CCINT}}$ is reached until the device enters user mode (1)	5M40Z	Commercial and industrial	—	—	200	$\mu\text{s}$
			Extended	—	—	300	$\mu\text{s}$
		5M80Z	Commercial and industrial	—	—	200	$\mu\text{s}$
			Extended	—	—	300	$\mu\text{s}$
		5M160Z	Commercial and industrial	—	—	200	$\mu\text{s}$
			Extended	—	—	300	$\mu\text{s}$
		5M240Z (2)	Commercial and industrial	—	—	200	$\mu\text{s}$
			Extended	—	—	300	$\mu\text{s}$
		5M240Z (3)	Commercial and industrial	—	—	300	$\mu\text{s}$
			Extended	—	—	400	$\mu\text{s}$
		5M570Z	Commercial and industrial	—	—	300	$\mu\text{s}$
			Extended	—	—	400	$\mu\text{s}$
		5M1270Z (4)	Commercial and industrial	—	—	300	$\mu\text{s}$
			Extended	—	—	400	$\mu\text{s}$
		5M1270Z (5)	Commercial and industrial	—	—	450	$\mu\text{s}$
			Extended	—	—	500	$\mu\text{s}$
		5M2210Z	Commercial and industrial	—	—	450	$\mu\text{s}$
			Extended	—	—	500	$\mu\text{s}$

**Notes to Table 3-15:**

- (1) For more information about power-on reset (POR) trigger voltage, refer to the *Hot Socketing and Power-On Reset in MAX V Devices* chapter.
- (2) Not applicable to the T144 package of the 5M240Z device.
- (3) Only applicable to the T144 package of the 5M240Z device.
- (4) Not applicable to the F324 package of the 5M1270Z device.
- (5) Only applicable to the F324 package of the 5M1270Z device.

## Power Consumption

You can use the Altera® PowerPlay Early Power Estimator and PowerPlay Power Analyzer to estimate the device power.

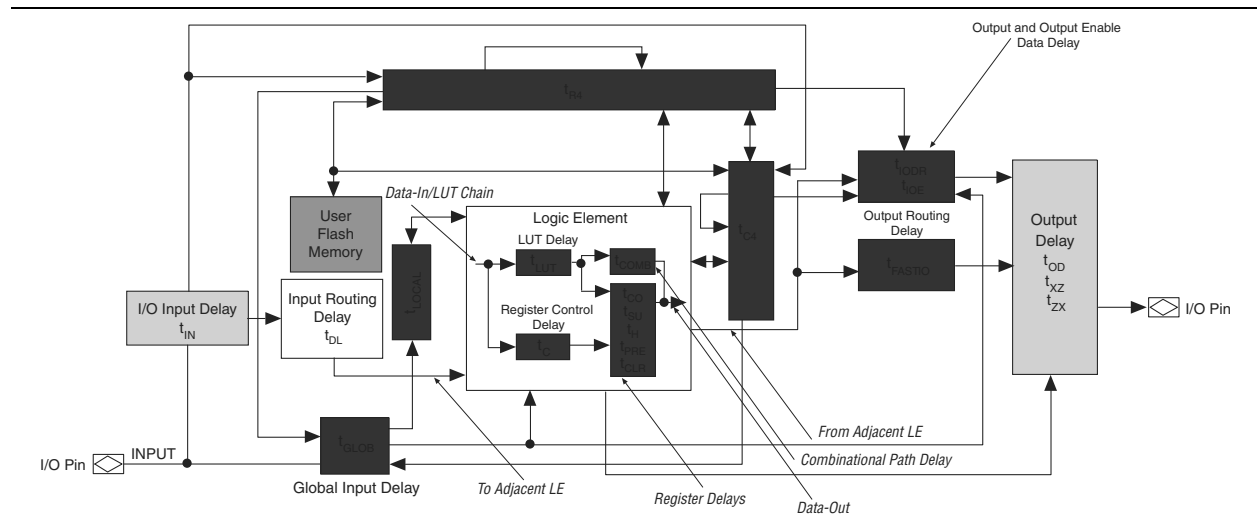
- For more information about these power analysis tools, refer to the *PowerPlay Early Power Estimator for Altera CPLDs User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

## Timing Model and Specifications

MAX V devices timing can be analyzed with the Altera Quartus® II software, a variety of industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 3-2.

MAX V devices have predictable internal delays that allow you to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

**Figure 3-2. Timing Model for MAX V Devices**



You can derive the timing characteristics of any signal path from the timing model and parameters of a particular device. You can calculate external timing parameters, which represent pin-to-pin timing delays, as the sum of the internal parameters.

- For more information, refer to *AN629: Understanding Timing in Altera CPLDs*.

## Preliminary and Final Timing

This section describes the performance, internal, external, and UFM timing specifications. All specifications are representative of the worst-case supply voltage and junction temperature conditions.

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 3–16 lists the status of the MAX V device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under the worst-case voltage and junction temperature conditions.

**Table 3–16. Timing Model Status for MAX V Devices**

Device	Final
5M40Z	✓
5M80Z	✓
5M160Z	✓
5M240Z	✓
5M570Z	✓
5M1270Z	✓
5M2210Z	✓

## Performance

Table 3–17 lists the MAX V device performance for some common designs. All performance values were obtained with the Quartus II software compilation of megafunctions.

**Table 3–17. Device Performance for MAX V Devices (Part 1 of 2)**

Resource Used	Design Size and Function	Resources Used			Performance				Unit
					5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z		5M1270Z/ 5M2210Z		
		Mode	LEs	UFM Blocks	C4	C5, I5	C4	C5, I5	
LE	16-bit counter (1)	—	16	0	184.1	118.3	247.5	201.1	MHz
	64-bit counter (1)	—	64	0	83.2	80.5	154.8	125.8	MHz
	16-to-1 multiplexer	—	11	0	17.4	20.4	8.0	9.3	ns
	32-to-1 multiplexer	—	24	0	12.5	25.3	9.0	11.4	ns
	16-bit XOR function	—	5	0	9.0	16.1	6.6	8.2	ns
	16-bit decoder with single address line	—	5	0	9.2	16.1	6.6	8.2	ns



**Table 3–18. LE Internal Timing Microparameters for MAX V Devices (Part 2 of 2)**

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{CLKHL}$	Minimum clock high or low time	253	—	339	—	216	—	266	—	ps
$t_C$	Register control delay	—	1,356	—	1,741	—	1,114	—	1,372	ps

**Table 3–19. IOE Internal Timing Microparameters for MAX V Devices**

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{FASTIO}$	Data output delay from adjacent LE to I/O block	—	170	—	428	—	207	—	254	ps
$t_{IN}$	I/O input pad and buffer delay	—	907	—	986	—	920	—	1,132	ps
$t_{GLOB} (1)$	I/O input pad and buffer delay used as global signal pin	—	2,261	—	3,322	—	1,974	—	2,430	ps
$t_{IOE}$	Internally generated output enable delay	—	530	—	1,410	—	374	—	460	ps
$t_{DL}$	Input routing delay	—	318	—	509	—	291	—	358	ps
$t_{OD} (2)$	Output delay buffer and pad delay	—	1,319	—	1,543	—	1,383	—	1,702	ps
$t_{XZ} (3)$	Output buffer disable delay	—	1,045	—	1,276	—	982	—	1,209	ps
$t_{ZX} (4)$	Output buffer enable delay	—	1,160	—	1,353	—	1,303	—	1,604	ps

**Notes to Table 3–19:**

- (1) Delay numbers for  $t_{GLOB}$  differ for each device density and speed grade. The delay numbers for  $t_{GLOB}$ , shown in Table 3–19, are based on a 5M240Z device target.
- (2) For more information about delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3–34 on page 3–24 and Table 3–35 on page 3–25.
- (3) For more information about  $t_{XZ}$  delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3–22 on page 3–15 and Table 3–23 on page 3–15.
- (4) For more information about  $t_{ZX}$  delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3–20 on page 3–14 and Table 3–21 on page 3–14.


Table 3–20 through Table 3–23 list the adder delays for  $t_{ZX}$  and  $t_{XZ}$  microparameters when using an I/O standard other than 3.3-V LVTTTL with 16 mA drive strength.

**Table 3–20.  $t_{ZX}$  IOE Microparameter Adders for Fast Slew Rate for MAX V Devices**

Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	16 mA	—	0	—	0	—	0	—	0	ps
	8 mA	—	72	—	74	—	101	—	125	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	ps
	4 mA	—	72	—	74	—	101	—	125	ps
2.5-V LVTTTL / LVCMOS	14 mA	—	126	—	127	—	155	—	191	ps
	7 mA	—	196	—	197	—	545	—	671	ps
1.8-V LVTTTL / LVCMOS	6 mA	—	608	—	610	—	721	—	888	ps
	3 mA	—	681	—	685	—	2012	—	2477	ps
1.5-V LVCMOS	4 mA	—	1162	—	1157	—	1590	—	1957	ps
	2 mA	—	1245	—	1244	—	3269	—	4024	ps
1.2-V LVCMOS	3 mA	—	1889	—	1856	—	2860	—	3520	ps
3.3-V PCI	20 mA	—	72	—	74	—	–18	—	–22	ps
LVDS	—	—	126	—	127	—	155	—	191	ps
RSDS	—	—	126	—	127	—	155	—	191	ps

**Table 3–21.  $t_{ZX}$  IOE Microparameter Adders for Slow Slew Rate for MAX V Devices**

Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	16 mA	—	5,951	—	6,063	—	6,012	—	5,743	ps
	8 mA	—	6,534	—	6,662	—	8,785	—	8,516	ps
3.3-V LVCMOS	8 mA	—	5,951	—	6,063	—	6,012	—	5,743	ps
	4 mA	—	6,534	—	6,662	—	8,785	—	8,516	ps
2.5-V LVTTTL / LVCMOS	14 mA	—	9,110	—	9,237	—	10,072	—	9,803	ps
	7 mA	—	9,830	—	9,977	—	12,945	—	12,676	ps
1.8-V LVTTTL / LVCMOS	6 mA	—	21,800	—	21,787	—	21,185	—	20,916	ps
	3 mA	—	23,020	—	23,037	—	24,597	—	24,328	ps
1.5-V LVCMOS	4 mA	—	39,120	—	39,067	—	34,517	—	34,248	ps
	2 mA	—	40,670	—	40,617	—	39,717	—	39,448	ps
1.2-V LVCMOS	3 mA	—	69,505	—	70,461	—	55,800	—	55,531	ps
3.3-V PCI	20 mA	—	6,534	—	6,662	—	35	—	44	ps

 The default slew rate setting for MAX V devices in the Quartus II design software is “fast”.

**Table 3-24. UFM Block Internal Timing Microparameters for MAX V Devices (Part 1 of 2)**

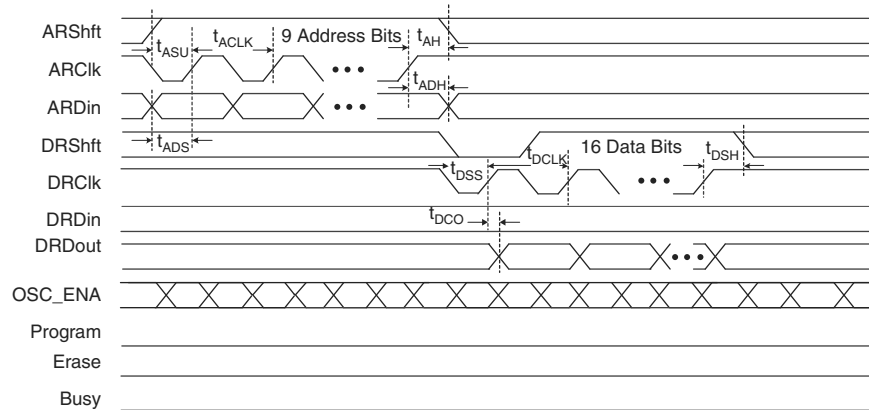
Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{\text{ACLK}}$	Address register clock period	100	—	100	—	100	—	100	—	ns
$t_{\text{ASU}}$	Address register shift signal setup to address register clock	20	—	20	—	20	—	20	—	ns
$t_{\text{AH}}$	Address register shift signal hold to address register clock	20	—	20	—	20	—	20	—	ns
$t_{\text{ADS}}$	Address register data in setup to address register clock	20	—	20	—	20	—	20	—	ns
$t_{\text{ADH}}$	Address register data in hold from address register clock	20	—	20	—	20	—	20	—	ns
$t_{\text{DCLK}}$	Data register clock period	100	—	100	—	100	—	100	—	ns
$t_{\text{DSS}}$	Data register shift signal setup to data register clock	60	—	60	—	60	—	60	—	ns
$t_{\text{DSH}}$	Data register shift signal hold from data register clock	20	—	20	—	20	—	20	—	ns
$t_{\text{DDS}}$	Data register data in setup to data register clock	20	—	20	—	20	—	20	—	ns
$t_{\text{DDH}}$	Data register data in hold from data register clock	20	—	20	—	20	—	20	—	ns
$t_{\text{DP}}$	Program signal to data clock hold time	0	—	0	—	0	—	0	—	ns
$t_{\text{PB}}$	Maximum delay between program rising edge to UFM <i>busy</i> signal rising edge	—	960	—	960	—	960	—	960	ns
$t_{\text{BP}}$	Minimum delay allowed from UFM <i>busy</i> signal going low to program signal going low	20	—	20	—	20	—	20	—	ns
$t_{\text{PPMX}}$	Maximum length of <i>busy</i> pulse during a program	—	100	—	100	—	100	—	100	$\mu\text{s}$

**Table 3-24. UFM Block Internal Timing Microparameters for MAX V Devices (Part 2 of 2)**

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{AE}$	Minimum erase signal to address clock hold time	0	—	0	—	0	—	0	—	ns
$t_{EB}$	Maximum delay between the erase rising edge to the UFM busy signal rising edge	—	960	—	960	—	960	—	960	ns
$t_{BE}$	Minimum delay allowed from the UFM busy signal going low to erase signal going low	20	—	20	—	20	—	20	—	ns
$t_{EPMX}$	Maximum length of busy pulse during an erase	—	500	—	500	—	500	—	500	ms
$t_{DCO}$	Delay from data register clock to data register output	—	5	—	5	—	5	—	5	ns
$t_{OE}$	Delay from OSC_ENA signal reaching UFM to rising clock of osc leaving the UFM	180	—	180	—	180	—	180	—	ns
$t_{RA}$	Maximum read access time	—	65	—	65	—	65	—	65	ns
$t_{OSCS}$	Maximum delay between the OSC_ENA rising edge to the erase/program signal rising edge	250	—	250	—	250	—	250	—	ns
$t_{OSCH}$	Minimum delay allowed from the erase/program signal going low to OSC_ENA signal going low	250	—	250	—	250	—	250	—	ns

Figure 3-3 through Figure 3-5 show the read, program, and erase waveforms for UFM block timing parameters listed in Table 3-24.

**Figure 3-3. UFM Read Waveform**



**Figure 3-4. UFM Program Waveform**

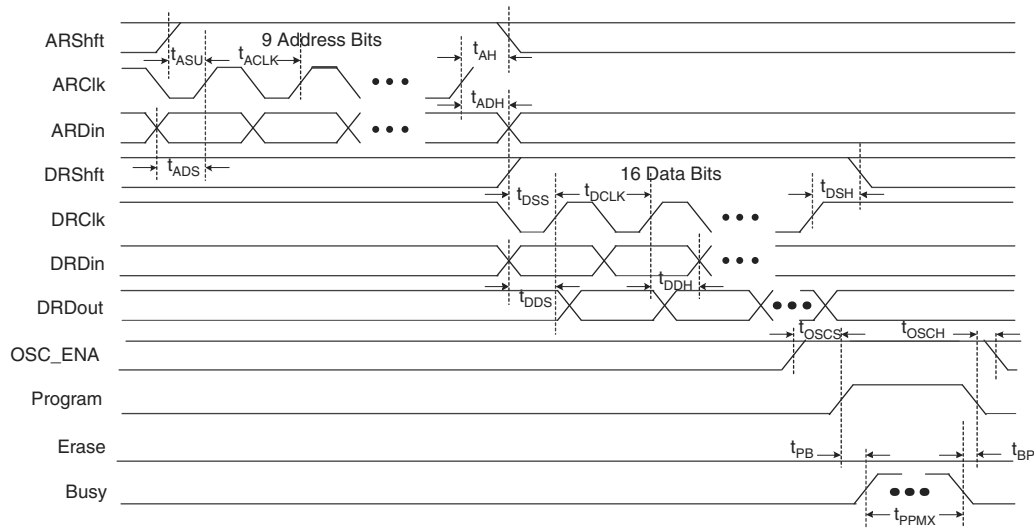


Table 3–26 lists the external I/O timing parameters for the 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices.

**Table 3–26. Global Clock External I/O Timing Parameters for the 5M40Z, 5M80Z, 5M160Z, and 5M240Z Devices (Note 1), (2)**

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
$t_{PD1}$	Worst case pin-to-pin delay through one LUT	10 pF	—	7.9	—	14.0	ns
$t_{PD2}$	Best case pin-to-pin delay through one LUT	10 pF	—	5.8	—	8.5	ns
$t_{SU}$	Global clock setup time	—	2.4	—	4.6	—	ns
$t_H$	Global clock hold time	—	0	—	0	—	ns
$t_{CO}$	Global clock to output delay	10 pF	2.0	6.6	2.0	8.6	ns
$t_{CH}$	Global clock high time	—	253	—	339	—	ps
$t_{CL}$	Global clock low time	—	253	—	339	—	ps
$t_{CNT}$	Minimum global clock period for 16-bit counter	—	5.4	—	8.4	—	ns
$f_{CNT}$	Maximum global clock frequency for 16-bit counter	—	—	184.1	—	118.3	MHz

**Notes to Table 3–26:**

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.
- (2) Not applicable to the T144 package of the 5M240Z device.

Table 3–27 lists the external I/O timing parameters for the T144 package of the 5M240Z device.

**Table 3–27. Global Clock External I/O Timing Parameters for the 5M240Z Device (Note 1), (2)**

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
$t_{PD1}$	Worst case pin-to-pin delay through one LUT	10 pF	—	9.5	—	17.7	ns
$t_{PD2}$	Best case pin-to-pin delay through one LUT	10 pF	—	5.7	—	8.5	ns
$t_{SU}$	Global clock setup time	—	2.2	—	4.4	—	ns
$t_H$	Global clock hold time	—	0	—	0	—	ns
$t_{CO}$	Global clock to output delay	10 pF	2.0	6.7	2.0	8.7	ns
$t_{CH}$	Global clock high time	—	253	—	339	—	ps
$t_{CL}$	Global clock low time	—	253	—	339	—	ps
$t_{CNT}$	Minimum global clock period for 16-bit counter	—	5.4	—	8.4	—	ns
$f_{CNT}$	Maximum global clock frequency for 16-bit counter	—	—	184.1	—	118.3	MHz

**Notes to Table 3–27:**

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.
- (2) Only applicable to the T144 package of the 5M240Z device.

Table 3–28 lists the external I/O timing parameters for the 5M570Z device.

**Table 3–28. Global Clock External I/O Timing Parameters for the 5M570Z Device (Note 1)**

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
$t_{PD1}$	Worst case pin-to-pin delay through one LUT	10 pF	—	9.5	—	17.7	ns
$t_{PD2}$	Best case pin-to-pin delay through one LUT	10 pF	—	5.7	—	8.5	ns
$t_{SU}$	Global clock setup time	—	2.2	—	4.4	—	ns
$t_H$	Global clock hold time	—	0	—	0	—	ns
$t_{CO}$	Global clock to output delay	10 pF	2.0	6.7	2.0	8.7	ns
$t_{CH}$	Global clock high time	—	253	—	339	—	ps
$t_{CL}$	Global clock low time	—	253	—	339	—	ps
$t_{CNT}$	Minimum global clock period for 16-bit counter	—	5.4	—	8.4	—	ns
$f_{CNT}$	Maximum global clock frequency for 16-bit counter	—	—	184.1	—	118.3	MHz

**Note to Table 3–28:**

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 3–29 lists the external I/O timing parameters for the 5M1270Z device.

**Table 3–29. Global Clock External I/O Timing Parameters for the 5M1270Z Device (Note 1), (2)**

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
$t_{PD1}$	Worst case pin-to-pin delay through one LUT	10 pF	—	8.1	—	10.0	ns
$t_{PD2}$	Best case pin-to-pin delay through one LUT	10 pF	—	4.8	—	5.9	ns
$t_{SU}$	Global clock setup time	—	1.5	—	1.9	—	ns
$t_H$	Global clock hold time	—	0	—	0	—	ns
$t_{CO}$	Global clock to output delay	10 pF	2.0	5.9	2.0	7.3	ns
$t_{CH}$	Global clock high time	—	216	—	266	—	ps
$t_{CL}$	Global clock low time	—	216	—	266	—	ps
$t_{CNT}$	Minimum global clock period for 16-bit counter	—	4.0	—	5.0	—	ns
$f_{CNT}$	Maximum global clock frequency for 16-bit counter	—	—	247.5	—	201.1	MHz

**Notes to Table 3–29:**

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.  
 (2) Not applicable to the F324 package of the 5M1270Z device.

Table 3–30 lists the external I/O timing parameters for the F324 package of the 5M1270Z device.

**Table 3–30. Global Clock External I/O Timing Parameters for the 5M1270Z Device (Note 1), (2)**

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
$t_{PD1}$	Worst case pin-to-pin delay through one LUT	10 pF	—	9.1	—	11.2	ns
$t_{PD2}$	Best case pin-to-pin delay through one LUT	10 pF	—	4.8	—	5.9	ns
$t_{SU}$	Global clock setup time	—	1.5	—	1.9	—	ns
$t_H$	Global clock hold time	—	0	—	0	—	ns
$t_{CO}$	Global clock to output delay	10 pF	2.0	6.0	2.0	7.4	ns
$t_{CH}$	Global clock high time	—	216	—	266	—	ps
$t_{CL}$	Global clock low time	—	216	—	266	—	ps
$t_{CNT}$	Minimum global clock period for 16-bit counter	—	4.0	—	5.0	—	ns
$f_{CNT}$	Maximum global clock frequency for 16-bit counter	—	—	247.5	—	201.1	MHz

**Notes to Table 3–30:**

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.
- (2) Only applicable to the F324 package of the 5M1270Z device.

Table 3–31 lists the external I/O timing parameters for the 5M2210Z device.

**Table 3–31. Global Clock External I/O Timing Parameters for the 5M2210Z Device (Note 1)**

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
$t_{PD1}$	Worst case pin-to-pin delay through one LUT	10 pF	—	9.1	—	11.2	ns
$t_{PD2}$	Best case pin-to-pin delay through one LUT	10 pF	—	4.8	—	5.9	ns
$t_{SU}$	Global clock setup time	—	1.5	—	1.9	—	ns
$t_H$	Global clock hold time	—	0	—	0	—	ns
$t_{CO}$	Global clock to output delay	10 pF	2.0	6.0	2.0	7.4	ns
$t_{CH}$	Global clock high time	—	216	—	266	—	ps
$t_{CL}$	Global clock low time	—	216	—	266	—	ps
$t_{CNT}$	Minimum global clock period for 16-bit counter	—	4.0	—	5.0	—	ns
$f_{CNT}$	Maximum global clock frequency for 16-bit counter	—	—	247.5	—	201.1	MHz

**Note to Table 3–31:**

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.



## External Timing I/O Delay Adders

The I/O delay timing parameters for the I/O standard input and output adders and the input delays are specified by speed grade, independent of device density.

Table 3–32 through Table 3–36 on page 3–25 list the adder delays associated with I/O pins for all packages. If you select an I/O standard other than 3.3-V LVTTTL, add the input delay adder to the external  $t_{SU}$  timing parameters listed in Table 3–26 on page 3–20 through Table 3–31. If you select an I/O standard other than 3.3-V LVTTTL with 16 mA drive strength and fast slew rate, add the output delay adder to the external  $t_{CO}$  and  $t_{PD}$  listed in Table 3–26 on page 3–20 through Table 3–31.

**Table 3–32. External Timing Input Delay Adders for MAX V Devices**

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	480	—	591	ps
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	480	—	591	ps
2.5-V LVTTTL / LVCMOS	Without Schmitt Trigger	—	42	—	42	—	246	—	303	ps
	With Schmitt Trigger	—	429	—	483	—	787	—	968	ps
1.8-V LVTTTL / LVCMOS	Without Schmitt Trigger	—	378	—	368	—	695	—	855	ps
1.5-V LVCMOS	Without Schmitt Trigger	—	681	—	658	—	1,334	—	1,642	ps
1.2-V LVCMOS	Without Schmitt Trigger	—	1,055	—	1,010	—	2,324	—	2,860	ps
3.3-V PCI	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps

**Table 3–33. External Timing Input Delay  $t_{GLOB}$  Adders for GCLK Pins for MAX V Devices (Part 1 of 2)**

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	400	—	493	ps

## Maximum Input and Output Clock Rates

Table 3-37 and Table 3-38 list the maximum input and output clock rates for standard I/O pins in MAX V devices.

**Table 3-37. Maximum Input Clock Rate for I/Os for MAX V Devices**

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z/5M1270Z/ 5M2210Z	Unit
		C4, C5, I5	
3.3-V LVTTTL	Without Schmitt Trigger	304	MHz
	With Schmitt Trigger	304	MHz
3.3-V LVCMOS	Without Schmitt Trigger	304	MHz
	With Schmitt Trigger	304	MHz
2.5-V LVTTTL	Without Schmitt Trigger	304	MHz
	With Schmitt Trigger	304	MHz
2.5-V LVCMOS	Without Schmitt Trigger	304	MHz
	With Schmitt Trigger	304	MHz
1.8-V LVTTTL	Without Schmitt Trigger	200	MHz
1.8-V LVCMOS	Without Schmitt Trigger	200	MHz
1.5-V LVCMOS	Without Schmitt Trigger	150	MHz
1.2-V LVCMOS	Without Schmitt Trigger	120	MHz
3.3-V PCI	Without Schmitt Trigger	304	MHz

**Table 3-38. Maximum Output Clock Rate for I/Os for MAX V Devices**

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z/5M1270Z/ 5M2210Z	Unit
		C4, C5, I5	
3.3-V LVTTTL		304	MHz
3.3-V LVCMOS		304	MHz
2.5-V LVTTTL		304	MHz
2.5-V LVCMOS		304	MHz
1.8-V LVTTTL		200	MHz
1.8-V LVCMOS		200	MHz
1.5-V LVCMOS		150	MHz
1.2-V LVCMOS		120	MHz
3.3-V PCI		304	MHz
LVDS		304	MHz
RSDS		200	MHz

## LVDS and RSDS Output Timing Specifications

Table 3–39 lists the emulated LVDS output timing specifications for MAX V devices.

**Table 3–39. Emulated LVDS Output Timing Specifications for MAX V Devices**

Parameter	Mode	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z/5M1270Z/ 5M2210Z		Unit
		C4, C5, I5		
		Min	Max	
Data rate (1), (2)	×10	—	304	Mbps
	×9	—	304	Mbps
	×8	—	304	Mbps
	×7	—	304	Mbps
	×6	—	304	Mbps
	×5	—	304	Mbps
	×4	—	304	Mbps
	×3	—	304	Mbps
	×2	—	304	Mbps
×1	—	304	Mbps	
t <sub>DUTY</sub>	—	45	55	%
Total jitter (3)	—	—	0.2	UI
t <sub>RISE</sub>	—	—	450	ps
t <sub>FALL</sub>	—	—	450	ps

**Notes to Table 3–39:**

- (1) The performance of the LVDS\_E\_3R transmitter system is limited by the lower of the two—the maximum data rate supported by LVDS\_E\_3R I/O buffer or 2x (F<sub>MAX</sub> of the ALTLVDS\_TX instance). The actual performance of your LVDS\_E\_3R transmitter system must be attained through the Quartus II timing analysis of the complete design.
- (2) For the input clock pin to achieve 304 Mbps, use I/O standard with V<sub>CCIO</sub> of 2.5 V and above.
- (3) This specification is based on external clean clock source.

Table 3–40 lists the emulated RSDS output timing specifications for MAX V devices.

**Table 3–40. Emulated RSDS Output Timing Specifications for MAX V Devices**

Parameter	Mode	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z/5M1270Z/ 5M2210Z		Unit
		C4, C5, I5		
		Min	Max	
Data rate (1)	×10	—	200	Mbps
	×9	—	200	Mbps
	×8	—	200	Mbps
	×7	—	200	Mbps
	×6	—	200	Mbps
	×5	—	200	Mbps
	×4	—	200	Mbps
	×3	—	200	Mbps
	×2	—	200	Mbps
×1	—	200	Mbps	
$t_{DUTY}$	—	45	55	%
Total jitter (2)	—	—	0.2	UI
$t_{RISE}$	—	—	450	ps
$t_{FALL}$	—	—	450	ps

**Notes to Table 3–40:**

- (1) For the input clock pin to achieve 200 Mbps, use I/O standard with  $V_{CCIO}$  of 1.8 V and above.
- (2) This specification is based on external clean clock source.

## JTAG Timing Specifications

Figure 3-6 shows the timing waveform for the JTAG signals for the MAX V device family.

**Figure 3-6. JTAG Timing Waveform for MAX V Devices**

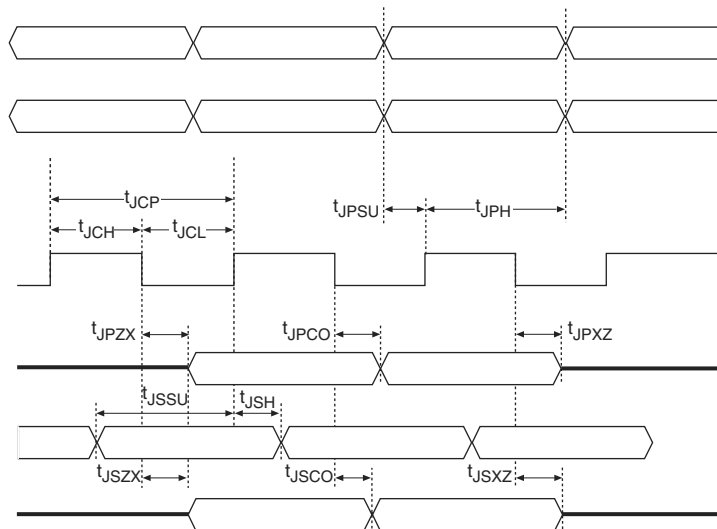


Table 3-41 lists the JTAG timing parameters and values for the MAX V device family.

**Table 3-41. JTAG Timing Parameters for MAX V Devices (Part 1 of 2)**

Symbol	Parameter	Min	Max	Unit
$t_{JCP}$ (1)	TCK clock period for $V_{CCI01} = 3.3$ V	55.5	—	ns
	TCK clock period for $V_{CCI01} = 2.5$ V	62.5	—	ns
	TCK clock period for $V_{CCI01} = 1.8$ V	100	—	ns
	TCK clock period for $V_{CCI01} = 1.5$ V	143	—	ns
$t_{JCH}$	TCK clock high time	20	—	ns
$t_{JCL}$	TCK clock low time	20	—	ns
$t_{JPSU}$	JTAG port setup time (2)	8	—	ns
$t_{JPH}$	JTAG port hold time	10	—	ns
$t_{JPCO}$	JTAG port clock to output (2)	—	15	ns
$t_{JPZX}$	JTAG port high impedance to valid output (2)	—	15	ns
$t_{JPXZ}$	JTAG port valid output to high impedance (2)	—	15	ns
$t_{JSSU}$	Capture register setup time	8	—	ns
$t_{JSH}$	Capture register hold time	10	—	ns
$t_{JSCO}$	Update register clock to output	—	25	ns
$t_{JSZX}$	Update register high impedance to valid output	—	25	ns