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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

| | |
|---------------------------------|---|
| Product Status | Active |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 7.5 ns |
| Voltage Supply - Internal | 1.71V ~ 1.89V |
| Number of Logic Elements/Blocks | 80 |
| Number of Macrocells | 64 |
| Number of Gates | - |
| Number of I/O | 52 |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 68-TFBGA |
| Supplier Device Package | 68-MBGA (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5m80zm68c5n |

Recommended Operating Conditions

Table 3–2 lists recommended operating conditions for the MAX V device family.

Table 3–2. Recommended Operating Conditions for MAX V Devices

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|-----------------|---|--------------------|---------|------------|------|
| V_{CCINT} (1) | 1.8-V supply voltage for internal logic and in-system programming (ISP) | MAX V devices | 1.71 | 1.89 | V |
| V_{CCIO} (1) | Supply voltage for I/O buffers, 3.3-V operation | — | 3.00 | 3.60 | V |
| | Supply voltage for I/O buffers, 2.5-V operation | — | 2.375 | 2.625 | V |
| | Supply voltage for I/O buffers, 1.8-V operation | — | 1.71 | 1.89 | V |
| | Supply voltage for I/O buffers, 1.5-V operation | — | 1.425 | 1.575 | V |
| | Supply voltage for I/O buffers, 1.2-V operation | — | 1.14 | 1.26 | V |
| V_I | Input voltage | (2), (3), (4) | –0.5 | 4.0 | V |
| V_O | Output voltage | — | 0 | V_{CCIO} | V |
| T_J | Operating junction temperature | Commercial range | 0 | 85 | °C |
| | | Industrial range | –40 | 100 | °C |
| | | Extended range (5) | –40 | 125 | °C |

Notes to Table 3–2:

- (1) MAX V device ISP and/or user flash memory (UFM) programming using JTAG or logic array is not guaranteed outside the recommended operating conditions (for example, if brown-out occurs in the system during a potential write/program sequence to the UFM, Altera recommends that you read back the UFM contents and verify it against the intended write data).
- (2) The minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) During transitions, the inputs may overshoot to the voltages shown below based on the input duty cycle. The DC case is equivalent to 100% duty cycle. For more information about 5.0-V tolerance, refer to the *Using MAX V Devices in Multi-Voltage Systems* chapter.

| V_{IN} | Max. Duty Cycle |
|----------|-----------------|
| 4.0 V | 100% (DC) |
| 4.1 V | 90% |
| 4.2 V | 50% |
| 4.3 V | 30% |
| 4.4 V | 17% |
| 4.5 V | 10% |
- (4) All pins, including the clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (5) For the extended temperature range of 100 to 125°C, MAX V UFM programming (erase/write) is only supported using the JTAG interface. UFM programming using the logic array interface is not guaranteed in this range.

Programming/Erase Specifications

Table 3–3 lists the programming/erase specifications for the MAX V device family.

Table 3–3. Programming/Erase Specifications for MAX V Devices

| Parameter | Block | Minimum | Typical | Maximum | Unit |
|----------------------------|----------------------------------|---------|---------|----------|--------|
| Erase and reprogram cycles | UFM | — | — | 1000 (1) | Cycles |
| | Configuration flash memory (CFM) | — | — | 100 | Cycles |

Note to Table 3–3:

(1) This value applies to the commercial grade devices. For the industrial grade devices, the value is 100 cycles.

DC Electrical Characteristics

Table 3–4 lists DC electrical characteristics for the MAX V device family.

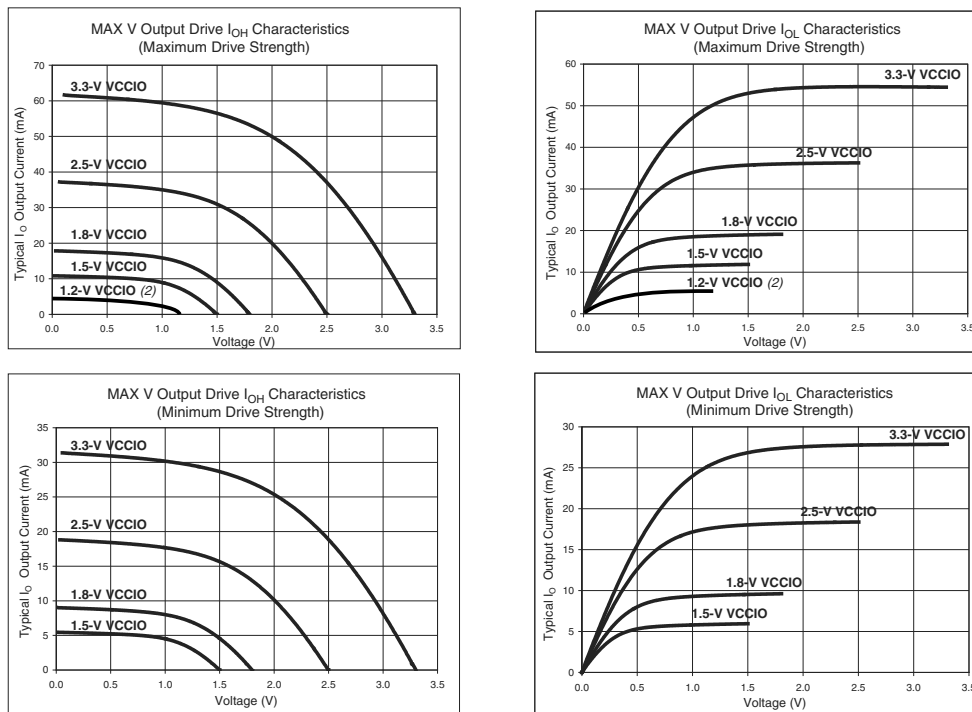
Table 3–4. DC Electrical Characteristics for MAX V Devices (Note 1) (Part 1 of 2)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|-------------------|--|--|---------|---------|---------|------------|
| I_I | Input pin leakage current | $V_I = V_{CCIO}$ max to 0 V (2) | –10 | — | 10 | μ A |
| I_{OZ} | Tri-stated I/O pin leakage current | $V_O = V_{CCIO}$ max to 0 V (2) | –10 | — | 10 | μ A |
| $I_{CCSTANDBY}$ | V_{CCINT} supply current (standby) (3) | 5M40Z, 5M80Z, 5M160Z, and 5M240Z (Commercial grade) (4), (5) | — | 25 | 90 | μ A |
| | | 5M240Z (Commercial grade) (6) | — | 27 | 96 | μ A |
| | | 5M40Z, 5M80Z, 5M160Z, and 5M240Z (Industrial grade) (5), (7) | — | 25 | 139 | μ A |
| | | 5M240Z (Industrial grade) (6) | — | 27 | 152 | μ A |
| | | 5M570Z (Commercial grade) (4) | — | 27 | 96 | μ A |
| | | 5M570Z (Industrial grade) (7) | — | 27 | 152 | μ A |
| | | 5M1270Z and 5M2210Z | — | 2 | — | mA |
| $V_{SCHMITT}$ (8) | Hysteresis for Schmitt trigger input (9) | $V_{CCIO} = 3.3$ V | — | 400 | — | mV |
| | | $V_{CCIO} = 2.5$ V | — | 190 | — | mV |
| $I_{CCPOWERUP}$ | V_{CCINT} supply current during power-up (10) | MAX V devices | — | — | 40 | mA |
| R_{PULLUP} | Value of I/O pin pull-up resistor during user mode and ISP | $V_{CCIO} = 3.3$ V (11) | 5 | — | 25 | k Ω |
| | | $V_{CCIO} = 2.5$ V (11) | 10 | — | 40 | k Ω |
| | | $V_{CCIO} = 1.8$ V (11) | 25 | — | 60 | k Ω |
| | | $V_{CCIO} = 1.5$ V (11) | 45 | — | 95 | k Ω |
| | | $V_{CCIO} = 1.2$ V (11) | 80 | — | 130 | k Ω |

Output Drive Characteristics

Figure 3-1 shows the typical drive strength characteristics of MAX V devices.

Figure 3-1. Output Drive Characteristics of MAX V Devices (Note 1)



Notes to Figure 3-1:

- (1) The DC output current per pin is subject to the absolute maximum rating of Table 3-1 on page 3-1.
- (2) 1.2-V V_{CCIO} is only applicable to the maximum drive strength.

I/O Standard Specifications

Table 3-5 through Table 3-13 on page 3-8 list the I/O standard specifications for the MAX V device family.

Table 3-5. 3.3-V LVTTTL Specifications for MAX V Devices

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|------------|---------------------------|------------------------------|---------|---------|------|
| V_{CCIO} | I/O supply voltage | — | 3.0 | 3.6 | V |
| V_{IH} | High-level input voltage | — | 1.7 | 4.0 | V |
| V_{IL} | Low-level input voltage | — | -0.5 | 0.8 | V |
| V_{OH} | High-level output voltage | $I_{OH} = -4 \text{ mA}$ (1) | 2.4 | — | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 4 \text{ mA}$ (1) | — | 0.45 | V |

Note to Table 3-5:

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

Table 3-6. 3.3-V LVCMOS Specifications for MAX V Devices

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|------------|---------------------------|---|------------------|---------|------|
| V_{CCIO} | I/O supply voltage | — | 3.0 | 3.6 | V |
| V_{IH} | High-level input voltage | — | 1.7 | 4.0 | V |
| V_{IL} | Low-level input voltage | — | -0.5 | 0.8 | V |
| V_{OH} | High-level output voltage | $V_{CCIO} = 3.0$, $IOH = -0.1 \text{ mA}$ (1) | $V_{CCIO} - 0.2$ | — | V |
| V_{OL} | Low-level output voltage | $V_{CCIO} = 3.0$, $IOL = 0.1 \text{ mA}$ (1) | — | 0.2 | V |

Note to Table 3-6:

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

Table 3-7. 2.5-V I/O Specifications for MAX V Devices

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|------------|---------------------------|-----------------------------|---------|---------|------|
| V_{CCIO} | I/O supply voltage | — | 2.375 | 2.625 | V |
| V_{IH} | High-level input voltage | — | 1.7 | 4.0 | V |
| V_{IL} | Low-level input voltage | — | -0.5 | 0.7 | V |
| V_{OH} | High-level output voltage | $IOH = -0.1 \text{ mA}$ (1) | 2.1 | — | V |
| | | $IOH = -1 \text{ mA}$ (1) | 2.0 | — | V |
| | | $IOH = -2 \text{ mA}$ (1) | 1.7 | — | V |
| V_{OL} | Low-level output voltage | $IOL = 0.1 \text{ mA}$ (1) | — | 0.2 | V |
| | | $IOL = 1 \text{ mA}$ (1) | — | 0.4 | V |
| | | $IOL = 2 \text{ mA}$ (1) | — | 0.7 | V |

Note to Table 3-7:

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

Table 3-8. 1.8-V I/O Specifications for MAX V Devices

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|------------|---------------------------|---------------------------|------------------------|------------------------|------|
| V_{CCIO} | I/O supply voltage | — | 1.71 | 1.89 | V |
| V_{IH} | High-level input voltage | — | $0.65 \times V_{CCIO}$ | 2.25 (2) | V |
| V_{IL} | Low-level input voltage | — | -0.3 | $0.35 \times V_{CCIO}$ | V |
| V_{OH} | High-level output voltage | $IOH = -2 \text{ mA}$ (1) | $V_{CCIO} - 0.45$ | — | V |
| V_{OL} | Low-level output voltage | $IOL = 2 \text{ mA}$ (1) | — | 0.45 | V |

Notes to Table 3-8:

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.
- (2) This maximum V_{IH} reflects the JEDEC specification. The MAX V input buffer can tolerate a V_{IH} maximum of 4.0, as specified by the V_I parameter in Table 3-2 on page 3-2.

Table 3–9. 1.5-V I/O Specifications for MAX V Devices

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|------------|---------------------------|---------------------------|------------------------|------------------------|------|
| V_{CCIO} | I/O supply voltage | — | 1.425 | 1.575 | V |
| V_{IH} | High-level input voltage | — | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ (2) | V |
| V_{IL} | Low-level input voltage | — | -0.3 | $0.35 \times V_{CCIO}$ | V |
| V_{OH} | High-level output voltage | $IOH = -2 \text{ mA}$ (1) | $0.75 \times V_{CCIO}$ | — | V |
| V_{OL} | Low-level output voltage | $IOL = 2 \text{ mA}$ (1) | — | $0.25 \times V_{CCIO}$ | V |

Notes to Table 3–9:

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.
- (2) This maximum V_{IH} reflects the JEDEC specification. The MAX V input buffer can tolerate a V_{IH} maximum of 4.0, as specified by the V_I parameter in Table 3–2 on page 3–2.

Table 3–10. 1.2-V I/O Specifications for MAX V Devices

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|------------|---------------------------|---------------------------|------------------------|------------------------|------|
| V_{CCIO} | I/O supply voltage | — | 1.14 | 1.26 | V |
| V_{IH} | High-level input voltage | — | $0.8 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | V |
| V_{IL} | Low-level input voltage | — | -0.3 | $0.25 \times V_{CCIO}$ | V |
| V_{OH} | High-level output voltage | $IOH = -2 \text{ mA}$ (1) | $0.75 \times V_{CCIO}$ | — | V |
| V_{OL} | Low-level output voltage | $IOL = 2 \text{ mA}$ (1) | — | $0.25 \times V_{CCIO}$ | V |

Note to Table 3–10:

- (1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

Table 3–11. 3.3-V PCI Specifications for MAX V Devices (Note 1)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|------------|---------------------------|--------------------------|-----------------------|---------|-----------------------|------|
| V_{CCIO} | I/O supply voltage | — | 3.0 | 3.3 | 3.6 | V |
| V_{IH} | High-level input voltage | — | $0.5 \times V_{CCIO}$ | — | $V_{CCIO} + 0.5$ | V |
| V_{IL} | Low-level input voltage | — | -0.5 | — | $0.3 \times V_{CCIO}$ | V |
| V_{OH} | High-level output voltage | $IOH = -500 \mu\text{A}$ | $0.9 \times V_{CCIO}$ | — | — | V |
| V_{OL} | Low-level output voltage | $IOL = 1.5 \text{ mA}$ | — | — | $0.1 \times V_{CCIO}$ | V |

Note to Table 3–11:

- (1) 3.3-V PCI I/O standard is only supported in Bank 3 of the 5M1270Z and 5M2210Z devices.

Table 3–12. LVDS Specifications for MAX V Devices (Note 1)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|------------|-----------------------------------|------------|---------|---------|---------|------|
| V_{CCIO} | I/O supply voltage | — | 2.375 | 2.5 | 2.625 | V |
| V_{OD} | Differential output voltage swing | — | 247 | — | 600 | mV |
| V_{OS} | Output offset voltage | — | 1.125 | 1.25 | 1.375 | V |

Note to Table 3–12:

- (1) Supports emulated LVDS output using a three-resistor network (LVDS_E_3R).

Table 3–13. RSDS Specifications for MAX V Devices (Note 1)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|------------|-----------------------------------|------------|---------|---------|---------|------|
| V_{CCIO} | I/O supply voltage | — | 2.375 | 2.5 | 2.625 | V |
| V_{OD} | Differential output voltage swing | — | 247 | — | 600 | mV |
| V_{OS} | Output offset voltage | — | 1.125 | 1.25 | 1.375 | V |

Note to Table 3–13:

(1) Supports emulated RSDS output using a three-resistor network (RSDS_E_3R).

Bus Hold Specifications

Table 3–14 lists the bus hold specifications for the MAX V device family.

Table 3–14. Bus Hold Specifications for MAX V Devices

| Parameter | Conditions | V_{CCIO} Level | | | | | | | | | | Unit |
|-------------------------|----------------------------------|------------------|------|-------|------|-------|------|-------|------|-------|------|---------|
| | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.3 V | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | $V_{IN} > V_{IL}$ (maximum) | 10 | — | 20 | — | 30 | — | 50 | — | 70 | — | μ A |
| High sustaining current | $V_{IN} < V_{IH}$ (minimum) | -10 | — | -20 | — | -30 | — | -50 | — | -70 | — | μ A |
| Low overdrive current | $0\text{ V} < V_{IN} < V_{CCIO}$ | — | 130 | — | 160 | — | 200 | — | 300 | — | 500 | μ A |
| High overdrive current | $0\text{ V} < V_{IN} < V_{CCIO}$ | — | -130 | — | -160 | — | -200 | — | -300 | — | -500 | μ A |

Power-Up Timing

Table 3-15 lists the power-up timing characteristics for the MAX V device family.

Table 3-15. Power-Up Timing for MAX V Devices

| Symbol | Parameter | Device | Temperature Range | Min | Typ | Max | Unit |
|---------------------|--|-------------|---------------------------|-----|-----|-----|---------------|
| t_{CONFIG} | The amount of time from when minimum V_{CCINT} is reached until the device enters user mode (1) | 5M40Z | Commercial and industrial | — | — | 200 | μs |
| | | | Extended | — | — | 300 | μs |
| | | 5M80Z | Commercial and industrial | — | — | 200 | μs |
| | | | Extended | — | — | 300 | μs |
| | | 5M160Z | Commercial and industrial | — | — | 200 | μs |
| | | | Extended | — | — | 300 | μs |
| | | 5M240Z (2) | Commercial and industrial | — | — | 200 | μs |
| | | | Extended | — | — | 300 | μs |
| | | 5M240Z (3) | Commercial and industrial | — | — | 300 | μs |
| | | | Extended | — | — | 400 | μs |
| | | 5M570Z | Commercial and industrial | — | — | 300 | μs |
| | | | Extended | — | — | 400 | μs |
| | | 5M1270Z (4) | Commercial and industrial | — | — | 300 | μs |
| | | | Extended | — | — | 400 | μs |
| | | 5M1270Z (5) | Commercial and industrial | — | — | 450 | μs |
| | | | Extended | — | — | 500 | μs |
| | | 5M2210Z | Commercial and industrial | — | — | 450 | μs |
| | | | Extended | — | — | 500 | μs |

Notes to Table 3-15:

- (1) For more information about power-on reset (POR) trigger voltage, refer to the *Hot Socketing and Power-On Reset in MAX V Devices* chapter.
- (2) Not applicable to the T144 package of the 5M240Z device.
- (3) Only applicable to the T144 package of the 5M240Z device.
- (4) Not applicable to the F324 package of the 5M1270Z device.
- (5) Only applicable to the F324 package of the 5M1270Z device.

Table 3-17. Device Performance for MAX V Devices (Part 2 of 2)

| Resource Used | Design Size and Function | Resources Used | | | Performance | | | | Unit |
|---------------|--------------------------|----------------------|-----|------------|---|---------|------------------|---------|------|
| | | | | | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z | | 5M1270Z/ 5M2210Z | | |
| | | Mode | LEs | UFM Blocks | C4 | C5, I5 | C4 | C5, I5 | |
| UFM | 512 × 16 | None | 3 | 1 | 10.0 | 10.0 | 10.0 | 10.0 | MHz |
| | 512 × 16 | SPI (2) | 37 | 1 | 9.7 | 9.7 | 8.0 | 8.0 | MHz |
| | 512 × 8 | Parallel (3) | 73 | 1 | (4) | (4) | (4) | (4) | MHz |
| | 512 × 16 | I ² C (3) | 142 | 1 | 100 (5) | 100 (5) | 100 (5) | 100 (5) | kHz |

Notes to Table 3-17:

- (1) This design is a binary loadable up counter.
- (2) This design is configured for read-only operation in Extended mode. Read and write ability increases the number of logic elements (LEs) used.
- (3) This design is configured for read-only operation. Read and write ability increases the number of LEs used.
- (4) This design is asynchronous.
- (5) The I²C megafunction is verified in hardware up to 100-kHz serial clock line rate.

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Table 3-18 through Table 3-25 on page 3-19 list the MAX V device internal timing microparameters for LEs, input/output elements (IOEs), UFM blocks, and MultiTrack interconnects.

 For more information about each internal timing microparameters symbol, refer to AN629: Understanding Timing in Altera CPLDs.

Table 3-18. LE Internal Timing Microparameters for MAX V Devices (Part 1 of 2)

| Symbol | Parameter | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z | | | | 5M1270Z/ 5M2210Z | | | | Unit |
|-------------------|--|---|-------|--------|-------|------------------|-----|--------|-----|------|
| | | C4 | | C5, I5 | | C4 | | C5, I5 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t _{LUT} | LE combinational look-up table (LUT) delay | — | 1,215 | — | 2,247 | — | 742 | — | 914 | ps |
| t _{COMB} | Combinational path delay | — | 243 | — | 309 | — | 192 | — | 236 | ps |
| t _{CLR} | LE register clear delay | 401 | — | 545 | — | 309 | — | 381 | — | ps |
| t _{PRE} | LE register preset delay | 401 | — | 545 | — | 309 | — | 381 | — | ps |
| t _{SU} | LE register setup time before clock | 260 | — | 321 | — | 271 | — | 333 | — | ps |
| t _H | LE register hold time after clock | 0 | — | 0 | — | 0 | — | 0 | — | ps |
| t _{CO} | LE register clock-to-output delay | — | 380 | — | 494 | — | 305 | — | 376 | ps |

Table 3-18. LE Internal Timing Microparameters for MAX V Devices (Part 2 of 2)

| Symbol | Parameter | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z | | | | 5M1270Z/ 5M2210Z | | | | Unit |
|-------------|--------------------------------|---|-------|--------|-------|------------------|-------|--------|-------|------|
| | | C4 | | C5, I5 | | C4 | | C5, I5 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{CLKHL} | Minimum clock high or low time | 253 | — | 339 | — | 216 | — | 266 | — | ps |
| t_C | Register control delay | — | 1,356 | — | 1,741 | — | 1,114 | — | 1,372 | ps |

Table 3-19. IOE Internal Timing Microparameters for MAX V Devices

| Symbol | Parameter | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z | | | | 5M1270Z/ 5M2210Z | | | | Unit |
|----------------|--|---|-------|--------|-------|------------------|-------|--------|-------|------|
| | | C4 | | C5, I5 | | C4 | | C5, I5 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{FASTIO} | Data output delay from adjacent LE to I/O block | — | 170 | — | 428 | — | 207 | — | 254 | ps |
| t_{IN} | I/O input pad and buffer delay | — | 907 | — | 986 | — | 920 | — | 1,132 | ps |
| $t_{GLOB} (1)$ | I/O input pad and buffer delay used as global signal pin | — | 2,261 | — | 3,322 | — | 1,974 | — | 2,430 | ps |
| t_{IOE} | Internally generated output enable delay | — | 530 | — | 1,410 | — | 374 | — | 460 | ps |
| t_{DL} | Input routing delay | — | 318 | — | 509 | — | 291 | — | 358 | ps |
| $t_{OD} (2)$ | Output delay buffer and pad delay | — | 1,319 | — | 1,543 | — | 1,383 | — | 1,702 | ps |
| $t_{XZ} (3)$ | Output buffer disable delay | — | 1,045 | — | 1,276 | — | 982 | — | 1,209 | ps |
| $t_{ZX} (4)$ | Output buffer enable delay | — | 1,160 | — | 1,353 | — | 1,303 | — | 1,604 | ps |

Notes to Table 3-19:

- (1) Delay numbers for t_{GLOB} differ for each device density and speed grade. The delay numbers for t_{GLOB} , shown in Table 3-19, are based on a 5M240Z device target.
- (2) For more information about delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3-34 on page 3-24 and Table 3-35 on page 3-25.
- (3) For more information about t_{XZ} delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3-22 on page 3-15 and Table 3-23 on page 3-15.
- (4) For more information about t_{ZX} delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3-20 on page 3-14 and Table 3-21 on page 3-14.

Table 3–20 through Table 3–23 list the adder delays for t_{ZX} and t_{XZ} microparameters when using an I/O standard other than 3.3-V LVTTTL with 16 mA drive strength.

Table 3–20. t_{ZX} IOE Microparameter Adders for Fast Slew Rate for MAX V Devices

| Standard | | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z | | | | 5M1270Z/ 5M2210Z | | | | Unit |
|--------------------------|-------|---|------|--------|------|------------------|------|--------|------|------|
| | | C4 | | C5, I5 | | C4 | | C5, I5 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| 3.3-V LVTTTL | 16 mA | — | 0 | — | 0 | — | 0 | — | 0 | ps |
| | 8 mA | — | 72 | — | 74 | — | 101 | — | 125 | ps |
| 3.3-V LVCMOS | 8 mA | — | 0 | — | 0 | — | 0 | — | 0 | ps |
| | 4 mA | — | 72 | — | 74 | — | 101 | — | 125 | ps |
| 2.5-V LVTTTL / LVCMOS | 14 mA | — | 126 | — | 127 | — | 155 | — | 191 | ps |
| | 7 mA | — | 196 | — | 197 | — | 545 | — | 671 | ps |
| 1.8-V LVTTTL / LVCMOS | 6 mA | — | 608 | — | 610 | — | 721 | — | 888 | ps |
| | 3 mA | — | 681 | — | 685 | — | 2012 | — | 2477 | ps |
| 1.5-V LVCMOS | 4 mA | — | 1162 | — | 1157 | — | 1590 | — | 1957 | ps |
| | 2 mA | — | 1245 | — | 1244 | — | 3269 | — | 4024 | ps |
| 1.2-V LVCMOS | 3 mA | — | 1889 | — | 1856 | — | 2860 | — | 3520 | ps |
| 3.3-V PCI | 20 mA | — | 72 | — | 74 | — | -18 | — | -22 | ps |
| LVDS | — | — | 126 | — | 127 | — | 155 | — | 191 | ps |
| RSDS | — | — | 126 | — | 127 | — | 155 | — | 191 | ps |

Table 3–21. t_{ZX} IOE Microparameter Adders for Slow Slew Rate for MAX V Devices

| Standard | | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z | | | | 5M1270Z/ 5M2210Z | | | | Unit |
|--------------------------|-------|---|--------|--------|--------|------------------|--------|--------|--------|------|
| | | C4 | | C5, I5 | | C4 | | C5, I5 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| 3.3-V LVTTTL | 16 mA | — | 5,951 | — | 6,063 | — | 6,012 | — | 5,743 | ps |
| | 8 mA | — | 6,534 | — | 6,662 | — | 8,785 | — | 8,516 | ps |
| 3.3-V LVCMOS | 8 mA | — | 5,951 | — | 6,063 | — | 6,012 | — | 5,743 | ps |
| | 4 mA | — | 6,534 | — | 6,662 | — | 8,785 | — | 8,516 | ps |
| 2.5-V LVTTTL / LVCMOS | 14 mA | — | 9,110 | — | 9,237 | — | 10,072 | — | 9,803 | ps |
| | 7 mA | — | 9,830 | — | 9,977 | — | 12,945 | — | 12,676 | ps |
| 1.8-V LVTTTL / LVCMOS | 6 mA | — | 21,800 | — | 21,787 | — | 21,185 | — | 20,916 | ps |
| | 3 mA | — | 23,020 | — | 23,037 | — | 24,597 | — | 24,328 | ps |
| 1.5-V LVCMOS | 4 mA | — | 39,120 | — | 39,067 | — | 34,517 | — | 34,248 | ps |
| | 2 mA | — | 40,670 | — | 40,617 | — | 39,717 | — | 39,448 | ps |
| 1.2-V LVCMOS | 3 mA | — | 69,505 | — | 70,461 | — | 55,800 | — | 55,531 | ps |
| 3.3-V PCI | 20 mA | — | 6,534 | — | 6,662 | — | 35 | — | 44 | ps |

Table 3–22. t_{xz} IOE Microparameter Adders for Fast Slew Rate for MAX V Devices

| Standard | | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z | | | | 5M1270Z/ 5M2210Z | | | | Unit |
|--------------------------|-------|---|-----|--------|-----|------------------|-----|--------|-------|------|
| | | C4 | | C5, I5 | | C4 | | C5, I5 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| 3.3-V LVTTTL | 16 mA | — | 0 | — | 0 | — | 0 | — | 0 | ps |
| | 8 mA | — | -69 | — | -69 | — | -74 | — | -91 | ps |
| 3.3-V LVCMOS | 8 mA | — | 0 | — | 0 | — | 0 | — | 0 | ps |
| | 4 mA | — | -69 | — | -69 | — | -74 | — | -91 | ps |
| 2.5-V LVTTTL / LVCMOS | 14 mA | — | -7 | — | -10 | — | -46 | — | -56 | ps |
| | 7 mA | — | -66 | — | -69 | — | -82 | — | -101 | ps |
| 1.8-V LVTTTL / LVCMOS | 6 mA | — | 45 | — | 37 | — | -7 | — | -8 | ps |
| | 3 mA | — | 34 | — | 25 | — | 119 | — | 147 | ps |
| 1.5-V LVCMOS | 4 mA | — | 166 | — | 155 | — | 339 | — | 418 | ps |
| | 2 mA | — | 190 | — | 179 | — | 464 | — | 571 | ps |
| 1.2-V LVCMOS | 3 mA | — | 300 | — | 283 | — | 817 | — | 1,006 | ps |
| 3.3-V PCI | 20 mA | — | -69 | — | -69 | — | 80 | — | 99 | ps |
| LVDS | — | — | -7 | — | -10 | — | -46 | — | -56 | ps |
| RSDS | — | — | -7 | — | -10 | — | -46 | — | -56 | ps |

Table 3–23. t_{xz} IOE Microparameter Adders for Slow Slew Rate for MAX V Devices

| Standard | | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z | | | | 5M1270Z/ 5M2210Z | | | | Unit |
|--------------------------|-------|---|-------|--------|-------|------------------|-------|--------|-------|------|
| | | C4 | | C5, I5 | | C4 | | C5, I5 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| 3.3-V LVTTTL | 16 mA | — | 171 | — | 174 | — | 73 | — | -132 | ps |
| | 8 mA | — | 112 | — | 116 | — | 758 | — | 553 | ps |
| 3.3-V LVCMOS | 8 mA | — | 171 | — | 174 | — | 73 | — | -132 | ps |
| | 4 mA | — | 112 | — | 116 | — | 758 | — | 553 | ps |
| 2.5-V LVTTTL / LVCMOS | 14 mA | — | 213 | — | 213 | — | 32 | — | -173 | ps |
| | 7 mA | — | 166 | — | 166 | — | 714 | — | 509 | ps |
| 1.8-V LVTTTL / LVCMOS | 6 mA | — | 441 | — | 438 | — | 96 | — | -109 | ps |
| | 3 mA | — | 496 | — | 494 | — | 963 | — | 758 | ps |
| 1.5-V LVCMOS | 4 mA | — | 765 | — | 755 | — | 238 | — | 33 | ps |
| | 2 mA | — | 903 | — | 897 | — | 1,319 | — | 1,114 | ps |
| 1.2-V LVCMOS | 3 mA | — | 1,159 | — | 1,130 | — | 400 | — | 195 | ps |
| 3.3-V PCI | 20 mA | — | 112 | — | 116 | — | 303 | — | 373 | ps |

Figure 3-3 through Figure 3-5 show the read, program, and erase waveforms for UFM block timing parameters listed in Table 3-24.

Figure 3-3. UFM Read Waveform

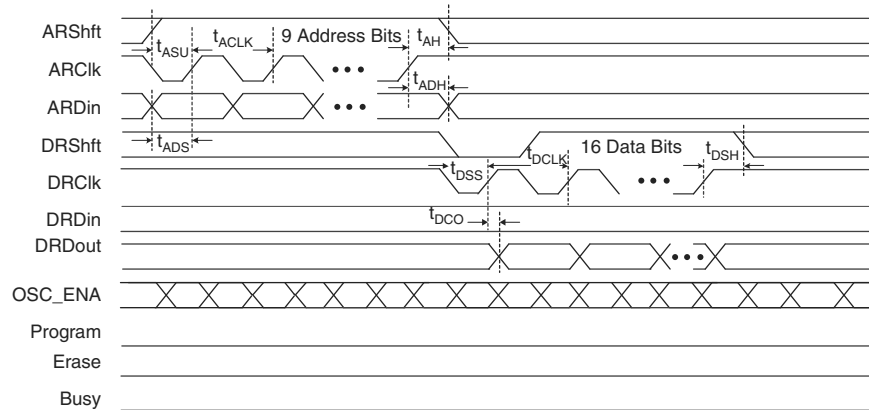


Figure 3-4. UFM Program Waveform

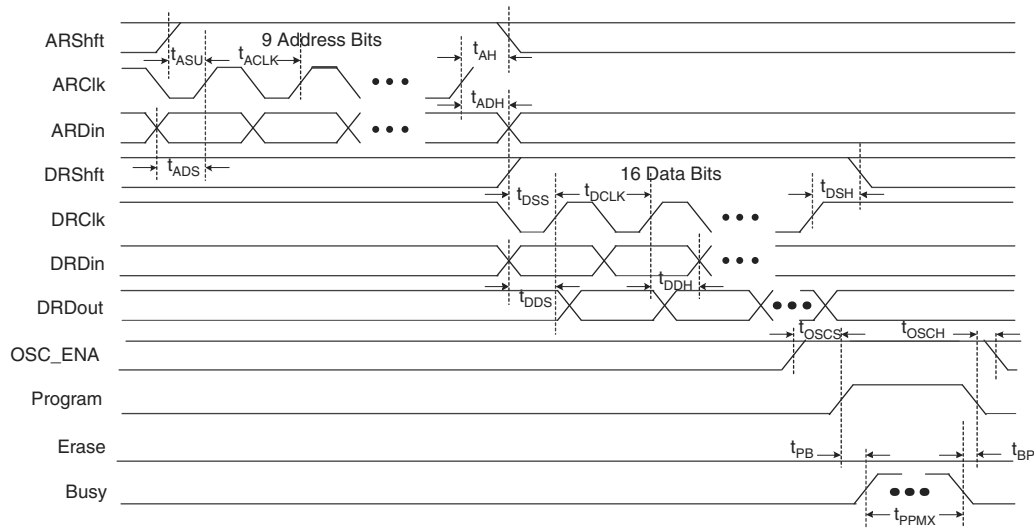


Figure 3-5. UFM Erase Waveform

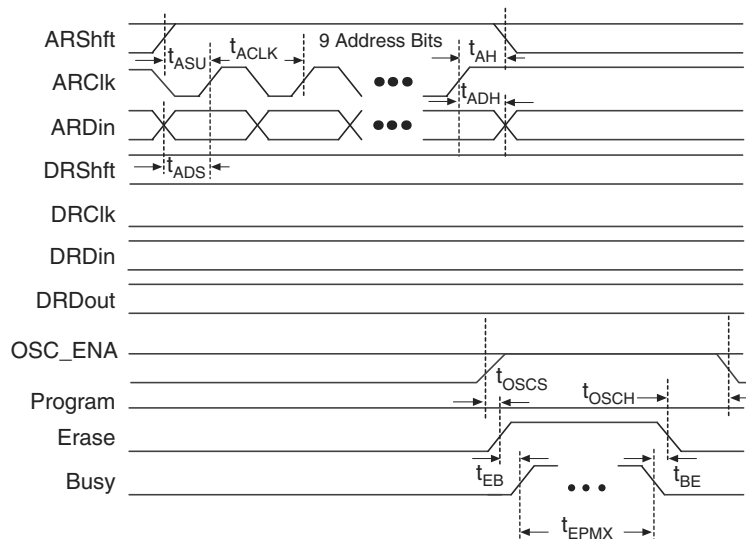


Table 3-25. Routing Delay Internal Timing Microparameters for MAX V Devices

| Routing | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z | | | | 5M1270Z/ 5M2210Z | | | | Unit |
|-------------|---|-------|--------|-------|------------------|-----|--------|-----|------|
| | C4 | | C5, I5 | | C4 | | C5, I5 | | |
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{C4} | — | 860 | — | 1,973 | — | 561 | — | 690 | ps |
| t_{R4} | — | 655 | — | 1,479 | — | 445 | — | 548 | ps |
| t_{LOCAL} | — | 1,143 | — | 2,947 | — | 731 | — | 899 | ps |

External Timing Parameters

External timing parameters are specified by device density and speed grade. All external I/O timing parameters shown are for the 3.3-V LVTTTL I/O standard with the maximum drive strength and fast slew rate. For external I/O timing using standards other than LVTTTL or for different drive strengths, use the I/O standard input and output delay adders in Table 3-32 on page 3-23 through Table 3-36 on page 3-25.

For more information about each external timing parameters symbol, refer to AN629: *Understanding Timing in Altera CPLDs*.

Table 3–26 lists the external I/O timing parameters for the 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices.

Table 3–26. Global Clock External I/O Timing Parameters for the 5M40Z, 5M80Z, 5M160Z, and 5M240Z Devices (Note 1), (2)

| Symbol | Parameter | Condition | C4 | | C5, I5 | | Unit |
|-----------|---|-----------|-----|-------|--------|-------|------|
| | | | Min | Max | Min | Max | |
| t_{PD1} | Worst case pin-to-pin delay through one LUT | 10 pF | — | 7.9 | — | 14.0 | ns |
| t_{PD2} | Best case pin-to-pin delay through one LUT | 10 pF | — | 5.8 | — | 8.5 | ns |
| t_{SU} | Global clock setup time | — | 2.4 | — | 4.6 | — | ns |
| t_H | Global clock hold time | — | 0 | — | 0 | — | ns |
| t_{CO} | Global clock to output delay | 10 pF | 2.0 | 6.6 | 2.0 | 8.6 | ns |
| t_{CH} | Global clock high time | — | 253 | — | 339 | — | ps |
| t_{CL} | Global clock low time | — | 253 | — | 339 | — | ps |
| t_{CNT} | Minimum global clock period for 16-bit counter | — | 5.4 | — | 8.4 | — | ns |
| f_{CNT} | Maximum global clock frequency for 16-bit counter | — | — | 184.1 | — | 118.3 | MHz |

Notes to Table 3–26:

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.
- (2) Not applicable to the T144 package of the 5M240Z device.

Table 3–27 lists the external I/O timing parameters for the T144 package of the 5M240Z device.

Table 3–27. Global Clock External I/O Timing Parameters for the 5M240Z Device (Note 1), (2)

| Symbol | Parameter | Condition | C4 | | C5, I5 | | Unit |
|-----------|---|-----------|-----|-------|--------|-------|------|
| | | | Min | Max | Min | Max | |
| t_{PD1} | Worst case pin-to-pin delay through one LUT | 10 pF | — | 9.5 | — | 17.7 | ns |
| t_{PD2} | Best case pin-to-pin delay through one LUT | 10 pF | — | 5.7 | — | 8.5 | ns |
| t_{SU} | Global clock setup time | — | 2.2 | — | 4.4 | — | ns |
| t_H | Global clock hold time | — | 0 | — | 0 | — | ns |
| t_{CO} | Global clock to output delay | 10 pF | 2.0 | 6.7 | 2.0 | 8.7 | ns |
| t_{CH} | Global clock high time | — | 253 | — | 339 | — | ps |
| t_{CL} | Global clock low time | — | 253 | — | 339 | — | ps |
| t_{CNT} | Minimum global clock period for 16-bit counter | — | 5.4 | — | 8.4 | — | ns |
| f_{CNT} | Maximum global clock frequency for 16-bit counter | — | — | 184.1 | — | 118.3 | MHz |

Notes to Table 3–27:

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.
- (2) Only applicable to the T144 package of the 5M240Z device.

External Timing I/O Delay Adders

The I/O delay timing parameters for the I/O standard input and output adders and the input delays are specified by speed grade, independent of device density.

Table 3–32 through Table 3–36 on page 3–25 list the adder delays associated with I/O pins for all packages. If you select an I/O standard other than 3.3-V LVTTTL, add the input delay adder to the external t_{SU} timing parameters listed in Table 3–26 on page 3–20 through Table 3–31. If you select an I/O standard other than 3.3-V LVTTTL with 16 mA drive strength and fast slew rate, add the output delay adder to the external t_{CO} and t_{PD} listed in Table 3–26 on page 3–20 through Table 3–31.

Table 3–32. External Timing Input Delay Adders for MAX V Devices

| I/O Standard | | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z | | | | 5M1270Z/ 5M2210Z | | | | Unit |
|--------------------------|-------------------------|---|-------|--------|-------|------------------|-------|--------|-------|------|
| | | C4 | | C5, I5 | | C4 | | C5, I5 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| 3.3-V LVTTTL | Without Schmitt Trigger | — | 0 | — | 0 | — | 0 | — | 0 | ps |
| | With Schmitt Trigger | — | 387 | — | 442 | — | 480 | — | 591 | ps |
| 3.3-V LVCMOS | Without Schmitt Trigger | — | 0 | — | 0 | — | 0 | — | 0 | ps |
| | With Schmitt Trigger | — | 387 | — | 442 | — | 480 | — | 591 | ps |
| 2.5-V LVTTTL / LVCMOS | Without Schmitt Trigger | — | 42 | — | 42 | — | 246 | — | 303 | ps |
| | With Schmitt Trigger | — | 429 | — | 483 | — | 787 | — | 968 | ps |
| 1.8-V LVTTTL / LVCMOS | Without Schmitt Trigger | — | 378 | — | 368 | — | 695 | — | 855 | ps |
| 1.5-V LVCMOS | Without Schmitt Trigger | — | 681 | — | 658 | — | 1,334 | — | 1,642 | ps |
| 1.2-V LVCMOS | Without Schmitt Trigger | — | 1,055 | — | 1,010 | — | 2,324 | — | 2,860 | ps |
| 3.3-V PCI | Without Schmitt Trigger | — | 0 | — | 0 | — | 0 | — | 0 | ps |

Table 3–33. External Timing Input Delay t_{GLOB} Adders for GCLK Pins for MAX V Devices (Part 1 of 2)

| I/O Standard | | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z | | | | 5M1270Z/ 5M2210Z | | | | Unit |
|--------------|-------------------------|---|-----|--------|-----|------------------|-----|--------|-----|------|
| | | C4 | | C5, I5 | | C4 | | C5, I5 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| 3.3-V LVTTTL | Without Schmitt Trigger | — | 0 | — | 0 | — | 0 | — | 0 | ps |
| | With Schmitt Trigger | — | 387 | — | 442 | — | 400 | — | 493 | ps |

Table 3-33. External Timing Input Delay t_{GLOB} Adders for GCLK Pins for MAX V Devices (Part 2 of 2)

| I/O Standard | | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z | | | | 5M1270Z/ 5M2210Z | | | | Unit |
|-----------------------|-------------------------|---|-------|--------|-------|------------------|-------|--------|-------|------|
| | | C4 | | C5, I5 | | C4 | | C5, I5 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| 3.3-V LVCMOS | Without Schmitt Trigger | — | 0 | — | 0 | — | 0 | — | 0 | ps |
| | With Schmitt Trigger | — | 387 | — | 442 | — | 400 | — | 493 | ps |
| 2.5-V LVTTTL / LVCMOS | Without Schmitt Trigger | — | 242 | — | 242 | — | 287 | — | 353 | ps |
| | With Schmitt Trigger | — | 429 | — | 483 | — | 550 | — | 677 | ps |
| 1.8-V LVTTTL / LVCMOS | Without Schmitt Trigger | — | 378 | — | 368 | — | 459 | — | 565 | ps |
| 1.5-V LVCMOS | Without Schmitt Trigger | — | 681 | — | 658 | — | 1,111 | — | 1,368 | ps |
| 1.2-V LVCMOS | Without Schmitt Trigger | — | 1,055 | — | 1,010 | — | 2,067 | — | 2,544 | ps |
| 3.3-V PCI | Without Schmitt Trigger | — | 0 | — | 0 | — | 7 | — | 9 | ps |

Table 3-34. External Timing Output Delay and t_{OD} Adders for Fast Slew Rate for MAX V Devices

| I/O Standard | | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z | | | | 5M1270Z/ 5M2210Z | | | | Unit |
|-----------------------|-------|---|-------|--------|-------|------------------|-------|--------|-------|------|
| | | C4 | | C5, I5 | | C4 | | C5, I5 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| 3.3-V LVTTTL | 16 mA | — | 0 | — | 0 | — | 0 | — | 0 | ps |
| | 8 mA | — | 39 | — | 58 | — | 84 | — | 104 | ps |
| 3.3-V LVCMOS | 8 mA | — | 0 | — | 0 | — | 0 | — | 0 | ps |
| | 4 mA | — | 39 | — | 58 | — | 84 | — | 104 | ps |
| 2.5-V LVTTTL / LVCMOS | 14 mA | — | 122 | — | 129 | — | 158 | — | 195 | ps |
| | 7 mA | — | 196 | — | 188 | — | 251 | — | 309 | ps |
| 1.8-V LVTTTL / LVCMOS | 6 mA | — | 624 | — | 624 | — | 738 | — | 909 | ps |
| | 3 mA | — | 686 | — | 694 | — | 850 | — | 1,046 | ps |
| 1.5-V LVCMOS | 4 mA | — | 1,188 | — | 1,184 | — | 1,376 | — | 1,694 | ps |
| | 2 mA | — | 1,279 | — | 1,280 | — | 1,517 | — | 1,867 | ps |
| 1.2-V LVCMOS | 3 mA | — | 1,911 | — | 1,883 | — | 2,206 | — | 2,715 | ps |
| 3.3-V PCI | 20 mA | — | 39 | — | 58 | — | 4 | — | 5 | ps |
| LVDS | — | — | 122 | — | 129 | — | 158 | — | 195 | ps |
| RSDS | — | — | 122 | — | 129 | — | 158 | — | 195 | ps |

Table 3-35. External Timing Output Delay and t_{OD} Adders for Slow Slew Rate for MAX V Devices

| I/O Standard | | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z | | | | 5M1270Z/ 5M2210Z | | | | Unit |
|-----------------------|-------|---|--------|--------|--------|------------------|--------|--------|--------|------|
| | | C4 | | C5, I5 | | C4 | | C5, I5 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| 3.3-V LVTTTL | 16 mA | — | 5,913 | — | 6,043 | — | 6,612 | — | 6,293 | ps |
| | 8 mA | — | 6,488 | — | 6,645 | — | 7,313 | — | 6,994 | ps |
| 3.3-V LVCMOS | 8 mA | — | 5,913 | — | 6,043 | — | 6,612 | — | 6,293 | ps |
| | 4 mA | — | 6,488 | — | 6,645 | — | 7,313 | — | 6,994 | ps |
| 2.5-V LVTTTL / LVCMOS | 14 mA | — | 9,088 | — | 9,222 | — | 10,021 | — | 9,702 | ps |
| | 7 mA | — | 9,808 | — | 9,962 | — | 10,881 | — | 10,562 | ps |
| 1.8-V LVTTTL / LVCMOS | 6 mA | — | 21,758 | — | 21,782 | — | 21,134 | — | 20,815 | ps |
| | 3 mA | — | 23,028 | — | 23,032 | — | 22,399 | — | 22,080 | ps |
| 1.5-V LVCMOS | 4 mA | — | 39,068 | — | 39,032 | — | 34,499 | — | 34,180 | ps |
| | 2 mA | — | 40,578 | — | 40,542 | — | 36,281 | — | 35,962 | ps |
| 1.2-V LVCMOS | 3 mA | — | 69,332 | — | 70,257 | — | 55,796 | — | 55,477 | ps |
| 3.3-V PCI | 20 mA | — | 6,488 | — | 6,645 | — | 339 | — | 418 | ps |

Table 3-36. IOE Programmable Delays for MAX V Devices

| Parameter | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z | | | | 5M1270Z/ 5M2210Z | | | | Unit |
|--|---|-------|--------|-------|------------------|-------|--------|-------|------|
| | C4 | | C5, I5 | | C4 | | C5, I5 | | |
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| Input Delay from Pin to Internal Cells = 1 | — | 1,858 | — | 2,214 | — | 1,592 | — | 1,960 | ps |
| Input Delay from Pin to Internal Cells = 0 | — | 569 | — | 616 | — | 115 | — | 142 | ps |

LVDS and RSDS Output Timing Specifications

Table 3–39 lists the emulated LVDS output timing specifications for MAX V devices.

Table 3–39. Emulated LVDS Output Timing Specifications for MAX V Devices

| Parameter | Mode | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z/5M1270Z/ 5M2210Z | | Unit |
|--------------------|------|---|------|------|
| | | C4, C5, I5 | | |
| | | Min | Max | |
| Data rate (1), (2) | ×10 | — | 304 | Mbps |
| | ×9 | — | 304 | Mbps |
| | ×8 | — | 304 | Mbps |
| | ×7 | — | 304 | Mbps |
| | ×6 | — | 304 | Mbps |
| | ×5 | — | 304 | Mbps |
| | ×4 | — | 304 | Mbps |
| | ×3 | — | 304 | Mbps |
| | ×2 | — | 304 | Mbps |
| ×1 | — | 304 | Mbps | |
| t _{DUTY} | — | 45 | 55 | % |
| Total jitter (3) | — | — | 0.2 | UI |
| t _{RISE} | — | — | 450 | ps |
| t _{FALL} | — | — | 450 | ps |

Notes to Table 3–39:

- (1) The performance of the LVDS_E_3R transmitter system is limited by the lower of the two—the maximum data rate supported by LVDS_E_3R I/O buffer or 2x (F_{MAX} of the ALTLVDS_TX instance). The actual performance of your LVDS_E_3R transmitter system must be attained through the Quartus II timing analysis of the complete design.
- (2) For the input clock pin to achieve 304 Mbps, use I/O standard with V_{CCIO} of 2.5 V and above.
- (3) This specification is based on external clean clock source.

Table 3–40 lists the emulated RSDS output timing specifications for MAX V devices.

Table 3–40. Emulated RSDS Output Timing Specifications for MAX V Devices

| Parameter | Mode | 5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z/5M1270Z/ 5M2210Z | | Unit |
|------------------|------|---|-----|------|
| | | C4, C5, I5 | | |
| | | Min | Max | |
| Data rate (1) | ×10 | — | 200 | Mbps |
| | ×9 | — | 200 | Mbps |
| | ×8 | — | 200 | Mbps |
| | ×7 | — | 200 | Mbps |
| | ×6 | — | 200 | Mbps |
| | ×5 | — | 200 | Mbps |
| | ×4 | — | 200 | Mbps |
| | ×3 | — | 200 | Mbps |
| | ×2 | — | 200 | Mbps |
| | ×1 | — | 200 | Mbps |
| t_{DUTY} | — | 45 | 55 | % |
| Total jitter (2) | — | — | 0.2 | UI |
| t_{RISE} | — | — | 450 | ps |
| t_{FALL} | — | — | 450 | ps |

Notes to Table 3–40:

- (1) For the input clock pin to achieve 200 Mbps, use I/O standard with V_{CCIO} of 1.8 V and above.
- (2) This specification is based on external clean clock source.

JTAG Timing Specifications

Figure 3-6 shows the timing waveform for the JTAG signals for the MAX V device family.

Figure 3-6. JTAG Timing Waveform for MAX V Devices

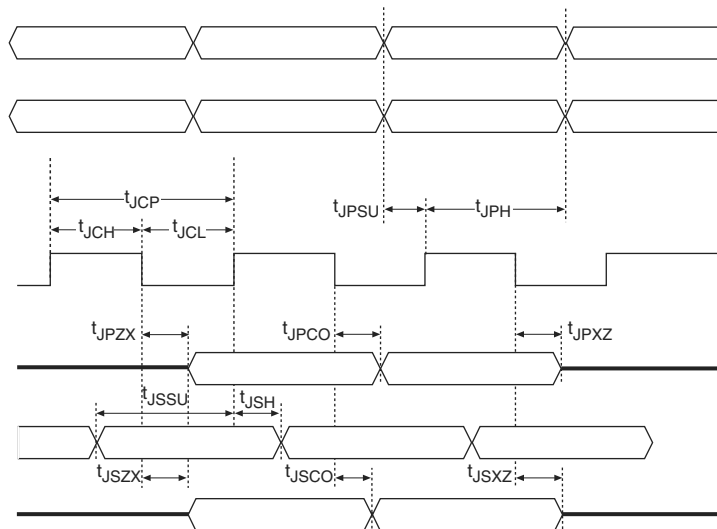


Table 3-41 lists the JTAG timing parameters and values for the MAX V device family.

Table 3-41. JTAG Timing Parameters for MAX V Devices (Part 1 of 2)

| Symbol | Parameter | Min | Max | Unit |
|---------------|--|------|-----|------|
| t_{JCP} (1) | TCK clock period for $V_{CCI01} = 3.3$ V | 55.5 | — | ns |
| | TCK clock period for $V_{CCI01} = 2.5$ V | 62.5 | — | ns |
| | TCK clock period for $V_{CCI01} = 1.8$ V | 100 | — | ns |
| | TCK clock period for $V_{CCI01} = 1.5$ V | 143 | — | ns |
| t_{JCH} | TCK clock high time | 20 | — | ns |
| t_{JCL} | TCK clock low time | 20 | — | ns |
| t_{JPSU} | JTAG port setup time (2) | 8 | — | ns |
| t_{JPH} | JTAG port hold time | 10 | — | ns |
| t_{JPCO} | JTAG port clock to output (2) | — | 15 | ns |
| t_{JPZX} | JTAG port high impedance to valid output (2) | — | 15 | ns |
| t_{JPXZ} | JTAG port valid output to high impedance (2) | — | 15 | ns |
| t_{JSSU} | Capture register setup time | 8 | — | ns |
| t_{JSH} | Capture register hold time | 10 | — | ns |
| t_{JSCO} | Update register clock to output | — | 25 | ns |
| t_{JSZX} | Update register high impedance to valid output | — | 25 | ns |