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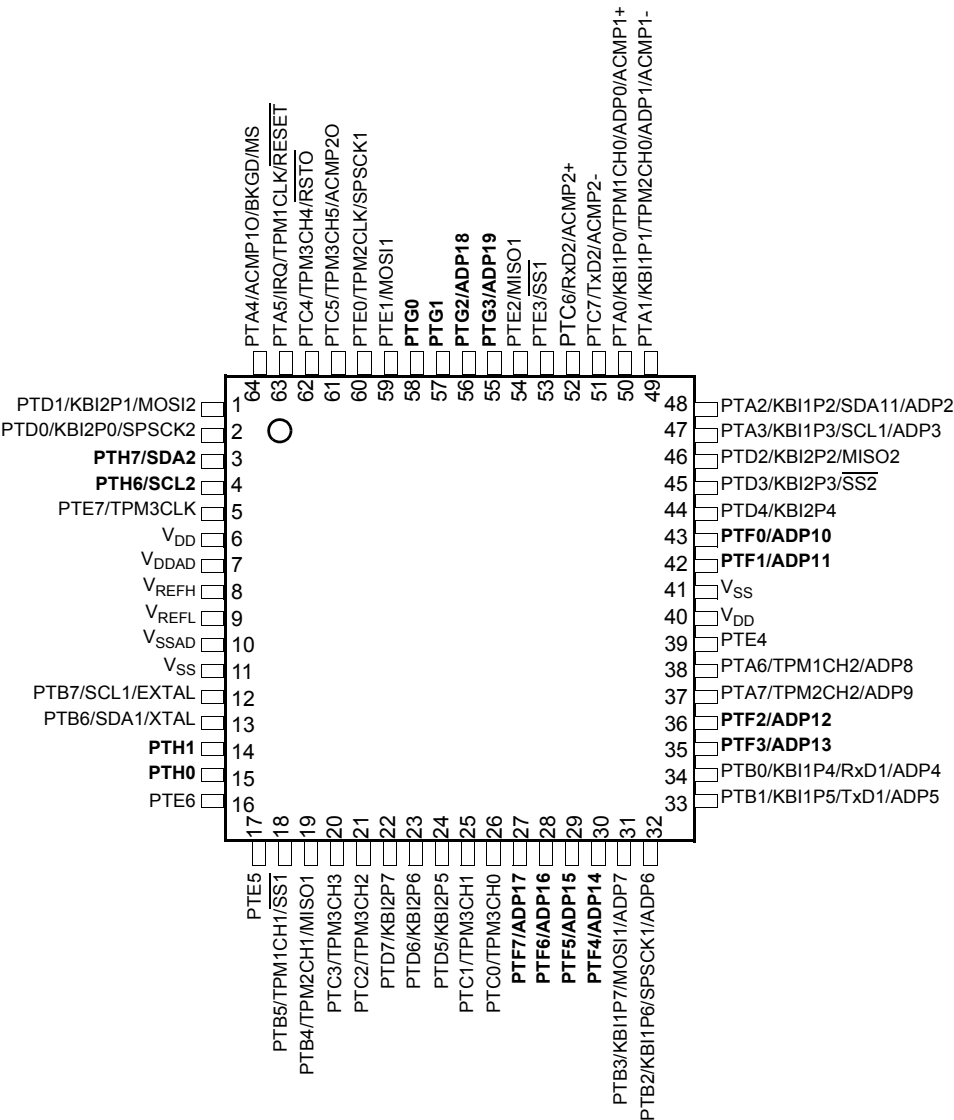
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	50MHz
Connectivity	I ² C, LINbus, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 22x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08qe128clh

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Pins in **bold** are added from the next smaller package.

Figure 3. Pin Assignments in 64-Pin LQFP Package

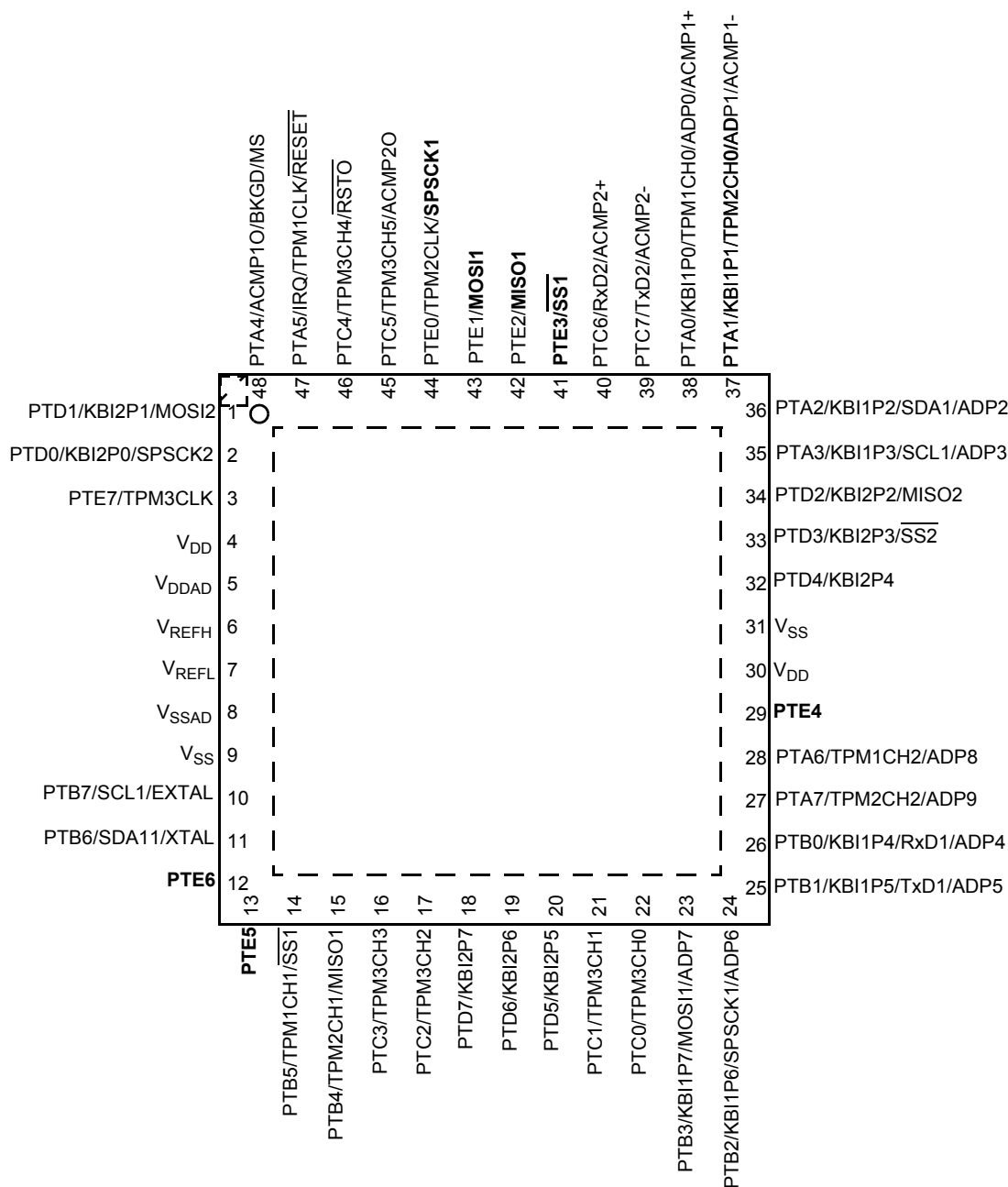


Figure 4. Pin Assignments in 48-Pin QFN Package

Table 2. MC9S08QE128 Series Pin Assignment by Package and Pin Count

Pin Number					Lowest	← Priority →	Highest		
80	64	48	44	32	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	1	1	1	PTD1	KBI2P1	MOSI2		
2	2	2	2	2	PTD0	KBI2P0	SPSCK2		
3	3	—	—	—	PTH7	SDA2			
4	4	—	—	—	PTH6	SCL2			
5	—	—	—	—	PTH5				
6	—	—	—	—	PTH4				
7	5	3	3	—	PTE7	TPM3CLK			
8	6	4	4	3					V _{DD}
9	7	5	5	4					V _{DDA}
10	8	6	6	—					V _{REFH}
11	9	7	7	—					V _{REFL}
12	10	8	8	5					V _{SSA}
13	11	9	9	6					V _{SS}
14	12	10	10	7	PTB7	SCL1			EXTAL
15	13	11	11	8	PTB6	SDA1			XTAL
16	—	—	—	—	PTH3				
17	—	—	—	—	PTH2				
18	14	—	—	—	PTH1				
19	15	—	—	—	PTH0				
20	16	12	—	—	PTE6				
21	17	13	—	—	PTE5				
22	18	14	12	9	PTB5	TPM1CH1	SS1		
23	19	15	13	10	PTB4	TPM2CH1	MISO1		
24	20	16	14	11	PTC3	TPM3CH3			
25	21	17	15	12	PTC2	TPM3CH2			
26	22	18	16	—	PTD7	KBI2P7			
27	23	19	17	—	PTD6	KBI2P6			
28	24	20	18	—	PTD5	KBI2P5			
29	—	—	—	—	PTJ7				
30	—	—	—	—	PTJ6				
31	—	—	—	—	PTJ5				
32	—	—	—	—	PTJ4				
33	25	21	19	13	PTC1	TPM3CH1			
34	26	22	20	14	PTC0	TPM3CH0			
35	27	—	—	—	PTF7				ADP17
36	28	—	—	—	PTF6				ADP16
37	29	—	—	—	PTF5				ADP15
38	30	—	—	—	PTF4				ADP14
39	31	23	21	15	PTB3	KBI1P7	MOSI1		ADP7
40	32	24	22	16	PTB2	KBI1P6	SPSCK1		ADP6

- ³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{IN} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T _A	−40 to 85	°C
Maximum junction temperature		T _{JM}	95	°C
Thermal resistance Single-layer board				
	32-pin LQFP	θ _{JA}	82	°C/W
	44-pin LQFP		68	
	48-pin QFN		81	
	64-pin LQFP	θ _{JA}	69	°C/W
	80-pin LQFP		60	
Thermal resistance Four-layer board				
	32-pin LQFP	θ _{JA}	54	°C/W
	44-pin LQFP		46	
	48-pin QFN		26	
	64-pin LQFP	θ _{JA}	50	°C/W
	80-pin LQFP		47	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typ ¹	Max	Unit	
1		Operating Voltage			1.8 ²		3.6	V	
2	C	Output high voltage All I/O pins, low-drive strength	V _{OH}	1.8 V, I _{Load} = –2 mA	V _{DD} – 0.5	—	—	V	
	P	All I/O pins, high-drive strength		2.7 V, I _{Load} = –10 mA	V _{DD} – 0.5	—	—		
	T	2.3 V, I _{Load} = –6 mA		V _{DD} – 0.5	—	—			
	C	1.8V, I _{Load} = –3 mA		V _{DD} – 0.5	—	—			
3	D	Output high current Max total I _{OH} for all ports	I _{OHT}		—	—	100	mA	
4	C	Output low voltage All I/O pins, low-drive strength	V _{OL}	1.8 V, I _{Load} = 2 mA	—	—	0.5	V	
	P	All I/O pins, high-drive strength		2.7 V, I _{Load} = 10 mA	—	—	0.5		
	T	2.3 V, I _{Load} = 6 mA		—	—	0.5			
	C	1.8 V, I _{Load} = 3 mA		—	—	0.5			
5	D	Output low current Max total I _{OL} for all ports	I _{OLT}		—	—	100	mA	
6	P	Input high voltage all digital inputs	V _{IH}	V _{DD} > 2.7 V	0.70 x V _{DD}	—	—	V	
	C	V _{DD} > 1.8 V		0.85 x V _{DD}	—	—			
7	P	Input low voltage all digital inputs	V _{IL}	V _{DD} > 2.7 V	—	—	0.35 x V _{DD}		
	C	V _{DD} > 1.8 V		—	—	0.30 x V _{DD}			
8	C	Input hysteresis all digital inputs	V _{hys}		0.06 x V _{DD}	—	—	mV	
9	P	Input leakage current all input only pins (Per pin)	I _{In}	V _{In} = V _{DD} or V _{SS}	—	—	1	μA	
10	P	Hi-Z (off-state) leakage current all input/output (per pin)	I _{OZ}	V _{In} = V _{DD} or V _{SS}	—	—	1	μA	
11	P	Pull-up resistors all digital inputs, when enabled	R _{PU}		17.5	—	52.5	kΩ	
12	D	DC injection current ^{3, 4, 5} Single pin limit	I _{IC}	V _{IN} < V _{SS} , V _{IN} > V _{DD}	–0.2	—	0.2	mA	
		Total MCU limit, includes sum of all stressed pins			–5	—	5	mA	
13	C	Input Capacitance, all pins	C _{In}		—	—	8	pF	
14	C	RAM retention voltage	V _{RAM}		—	0.6	1.0	V	
15	C	POR re-arm voltage ⁶	V _{POR}		0.9	1.4	1.79	V	
16	D	POR re-arm time	t _{POR}		10	—	—	μs	
17	P	Low-voltage detection threshold — high range ⁷	V _{LVDH} ⁸	V _{DD} falling V _{DD} rising	2.11 2.16	2.16 2.21	2.22 2.27	V	

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typ ¹	Max	Unit	Temp (°C)
6	P	Stop2 mode supply current	S2I _{DD}	n/a	3	0.35	0.6	μA	-40 to 25
	C					0.98	2.0		70
	P					2.5	7.5		85
	C				2	0.25	0.5		-40 to 25
	C					1.4	1.9		70
	C					1.91	6.5		85
7	P	Stop3 mode supply current No clocks active	S3I _{DD}	n/a	3	0.45	1.0	μA	-40 to 25
	C					1.99	4.2		70
	P					5.0	15.0		85
	C				2	0.35	0.7		-40 to 25
	C					2.9	3.9		70
	C					3.77	13.2		85

¹ Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

Table 10. Stop Mode Adders

Num	C	Parameter	Condition	Temperature (°C)				Units
				-40	25	70	85	
1	T	LPO		50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN ¹		63	70	77	81	uA
4	T	RTC	does not include clock source current	50	75	100	150	nA
5	T	LVD ¹	LVDSE = 1	90	100	110	115	uA
6	T	ACMP ¹	not using the bandgap (BGBE = 0)	18	20	22	23	uA
7	T	ADC ¹	ADLPC = ADLSMP = 1 not using the bandgap (BGBE = 0)	95	106	114	120	uA

¹ Not available in stop2 mode.

3.8 External Oscillator (XOSC) Characteristics

Reference Figure 13 and Figure 14 for crystal or resonator circuits.

Table 11. XOSC and ICS Specifications (Temperature Range = -40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ ¹	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)					
		Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		High range (RANGE = 1), high gain (HGO = 1)	f_{hi}	1	—	16	MHz
		High range (RANGE = 1), low power (HGO = 0)	f_{hi}	1	—	8	MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1, C_2	See Note ² See Note ³			
3	D	Feedback resistor	R_F				
		Low range, low power (RANGE=0, HGO=0) ²		—	—	—	MΩ
		Low range, High Gain (RANGE=0, HGO=1)		—	10	—	
		High range (RANGE=1, HGO=X)		—	1	—	
4	D	Series resistor —	R_S				kΩ
		Low range, low power (RANGE = 0, HGO = 0) ²		—	—	—	
		Low range, high gain (RANGE = 0, HGO = 1)		—	0	—	
		High range, low power (RANGE = 1, HGO = 0)		—	100	—	
		High range, high gain (RANGE = 1, HGO = 1)					
		≥ 8 MHz		—	0	0	
		4 MHz		—	0	10	
		1 MHz		—	0	20	
5	C	Crystal start-up time ⁴					
		Low range, low power	t_{CSTL}	—	200	—	ms
		Low range, high power		—	400	—	
		High range, low power	t_{CSTH}	—	5	—	
		High range, high power		—	15	—	
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)					
		FEE or FBE mode	f_{extal}	0.03125	—	40.0	MHz
		FBELP mode		0	—	50.33	MHz

¹ Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

² Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

³ See crystal or resonator manufacturer's recommendation.

⁴ Proper PC board layout procedures must be followed to achieve specifications.

Table 13. Control Timing (continued)

Num	C	Rating	Symbol	Min	Typ ¹	Max	Unit
7	D	IRQ pulse width Asynchronous path ² Synchronous path ⁴	$t_{\text{LIH}}, t_{\text{HIL}}$	100 $1.5 \times t_{\text{cyc}}$	— —	— —	ns
8	D	Keyboard interrupt pulse width Asynchronous path ² Synchronous path ⁴	$t_{\text{LIH}}, t_{\text{HIL}}$	100 $1.5 \times t_{\text{cyc}}$	— —	— —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF) ⁵ Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	$t_{\text{Rise}}, t_{\text{Fall}}$	— —	8 31	— —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	$t_{\text{Rise}}, t_{\text{Fall}}$	— —	7 24	— —	ns
10		Voltage regulator recovery time	t_{VRR}	—	4	—	μs

¹ Typical values are based on characterization data at $V_{\text{DD}} = 3.0\text{V}$, 25°C unless otherwise stated.

² This is the shortest pulse that is guaranteed to be recognized as a reset or interrupt pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

³ To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD} .

⁴ This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

⁵ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range -40°C to 85°C .

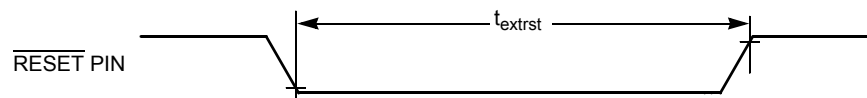
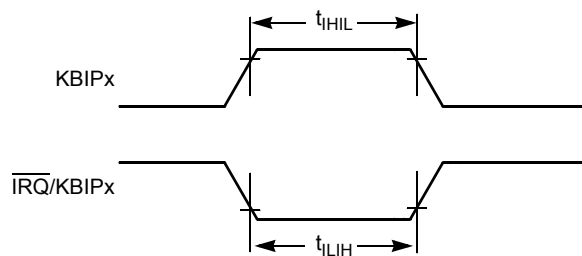
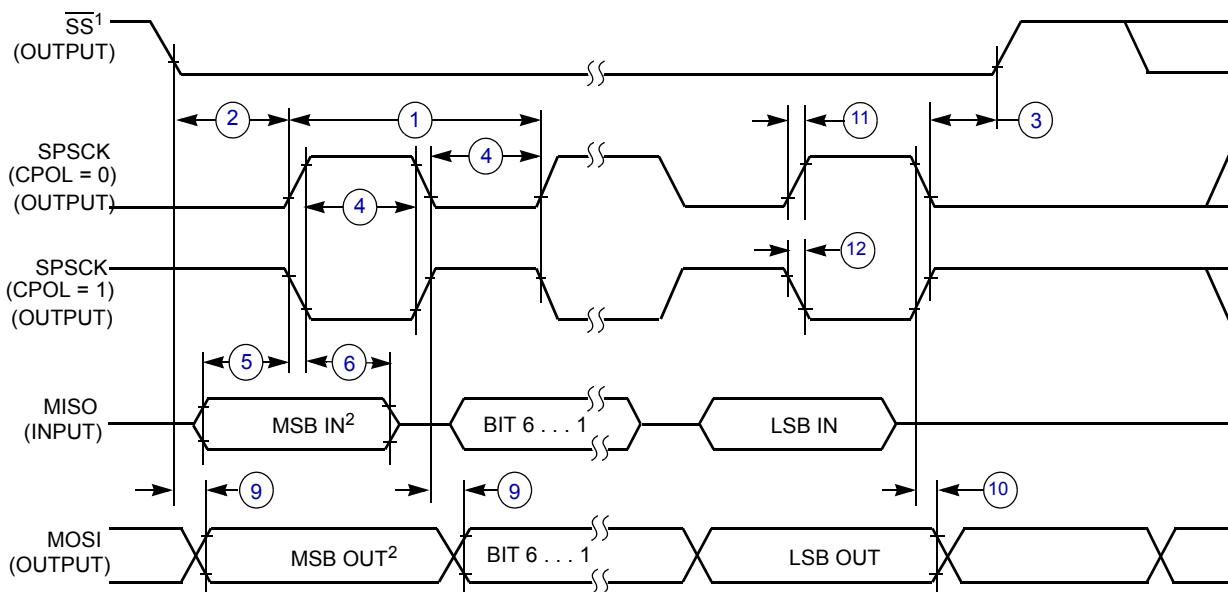


Figure 17. Reset Timing

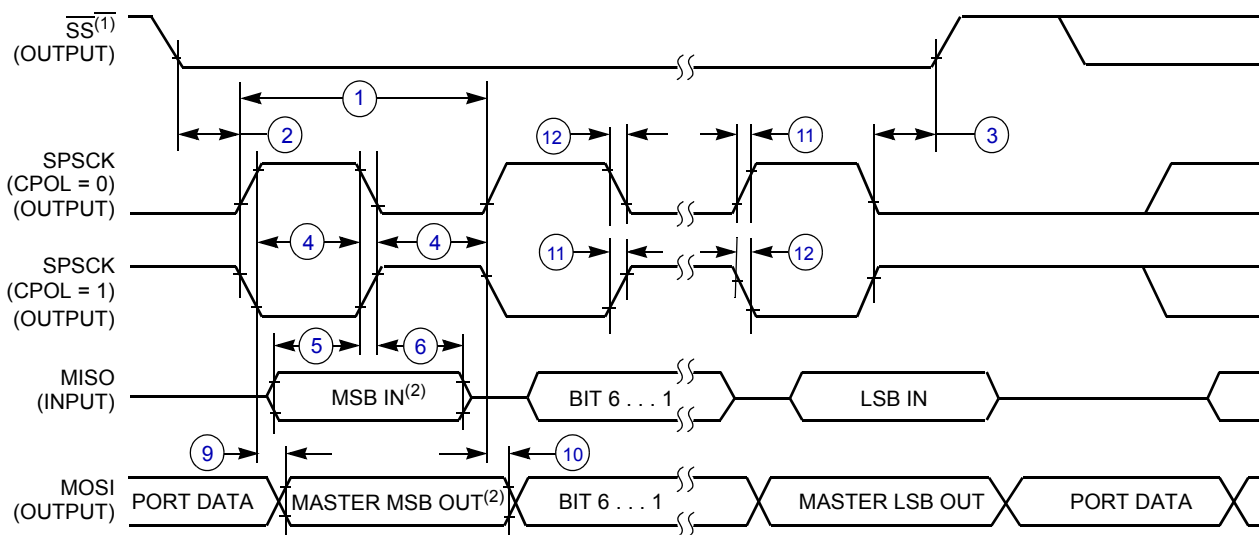

Figure 18. $\overline{\text{IRQ}}/\text{KBIPx}$ Timing



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 21. SPI Master Timing (CPHA = 0)



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 22. SPI Master Timing (CPHA = 1)

3.11 Analog Comparator (ACMP) Electricals

Table 16. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DD}	1.80	—	3.6	V
C	Supply current (active)	I_{DDAC}	—	20	35	μA
D	Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DD}	V
C	Analog input offset voltage	V_{AIO}	—	20	40	mV
C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs

3.12 ADC Characteristics

Table 17. 12-bit ADC Operating Conditions

C	Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
D	Supply voltage	Absolute	V_{DDAD}	1.8	—	3.6	V	
		Delta to V_{DD} ($V_{DD} - V_{DDAD}$) ²	ΔV_{DDAD}	-100	0	+100	mV	
D	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSAD}$) ²	ΔV_{SSAD}	-100	0	+100	mV	
D	Ref Voltage High		V_{REFH}	1.8	V_{DDAD}	V_{DDAD}	V	
D	Ref Voltage Low		V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	
D	Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
C	Input Capacitance		C_{ADIN}	—	4.5	5.5	pF	
C	Input Resistance		R_{ADIN}	—	5	7	k Ω	
C	Analog Source Resistance	12 bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$	R_{AS}	— —	— —	2 5	k Ω	External to MCU
		10 bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$		— —	— —	5 10		
		8 bit mode (all valid f_{ADCK})		—	—	10		
D	ADC Conversion Clock Freq.	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
		Low Power (ADLPC=1)		0.4	—	4.0		

¹ Typical values assume $V_{DDAD} = 3.0\text{V}$, Temp = 25°C, $f_{ADCK} = 1.0\text{MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.

² DC potential difference.



Table 18. 12-bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

MC9S08QE128 Series Data Sheet, Rev. 7

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section of the *MC9S08QE128 Reference Manual*.

Table 19. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase -40°C to 85°C	$V_{\text{prog/erase}}$	1.8		3.6	V
D	Supply voltage for read operation	V_{Read}	1.8		3.6	V
D	Internal FCLK frequency ¹	f_{FCLK}	150		200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	μs
P	Byte program time (random location) ⁽²⁾	t_{prog}	9			t_{Fcyc}
P	Byte program time (burst mode) ⁽²⁾	t_{Burst}	4			t_{Fcyc}
P	Page erase time ²	t_{Page}	4000			t_{Fcyc}
P	Mass erase time ⁽²⁾	t_{Mass}	20,000			t_{Fcyc}
	Byte program current ³	R_{IDDBP}	—	4	—	mA
	Page erase current ³	R_{IDDPE}	—	6	—	mA
C	Program/erase endurance ⁴ T_L to T_H = -40°C to + 85°C $T = 25^\circ\text{C}$		10,000 —	— 100,000	— —	cycles
C	Data retention ⁵	$t_{\text{D_ret}}$	15	100	—	years

¹ The frequency of this clock is controlled by a software setting.

² These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

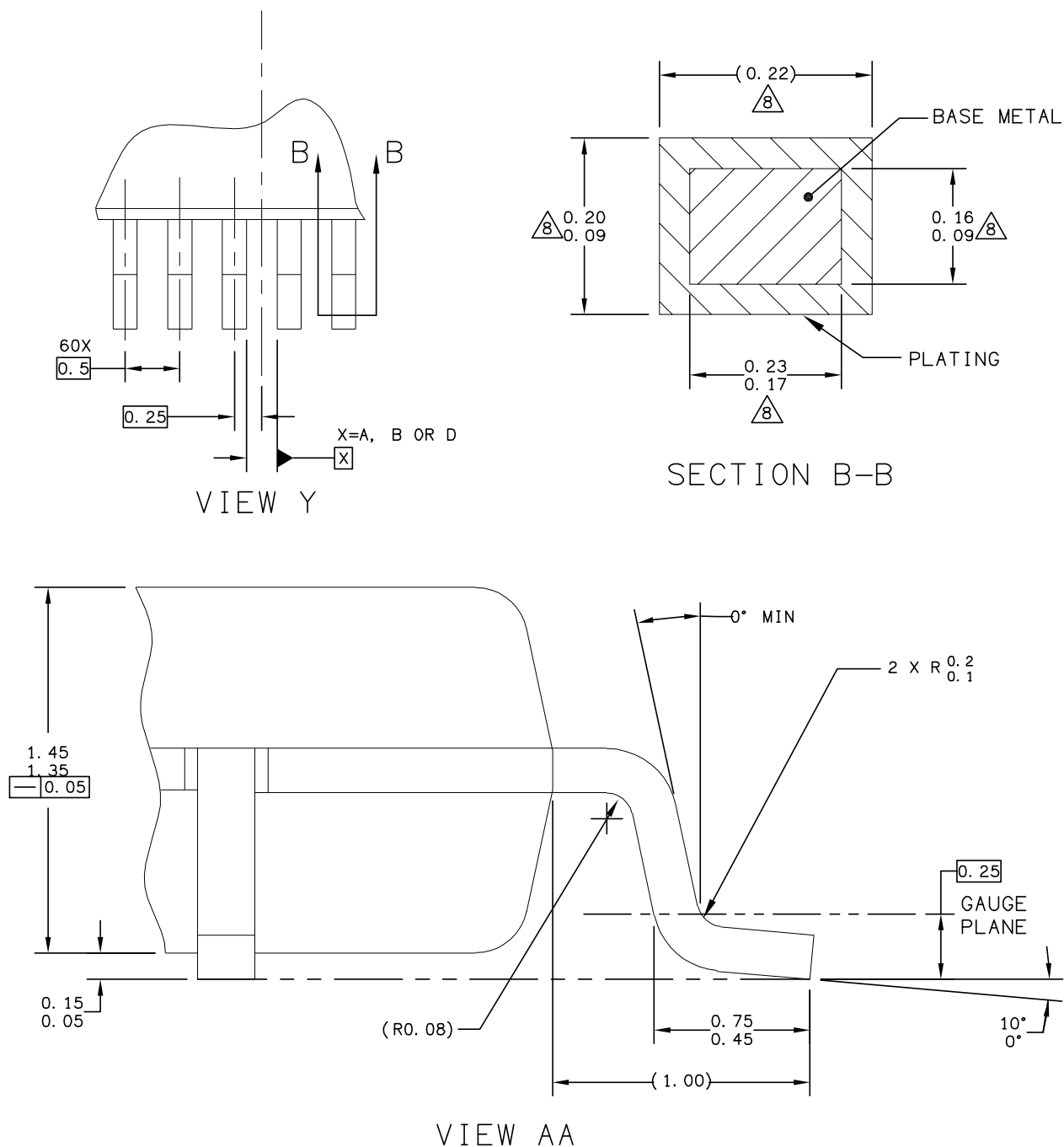
³ The program and erase currents are additional to the standard run I_{DD} . These values are measured at room temperatures with $V_{DD} = 3.0$ V, bus frequency = 4.0 MHz.

⁴ **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

⁵ **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory*.

5.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in [Table 21](#). For the latest available drawings please visit our web site (<http://www.freescale.com>) and enter the package's document number into the keyword search box.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W		REV: D
	CASE NUMBER: 840F-02		06 APR 2005
	STANDARD: JEDEC MS-026 BCD		

Figure 28. 64-pin LQFP Package Drawing (Case 840F, Doc #98ASS23234W), Sheet 2 of 3

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

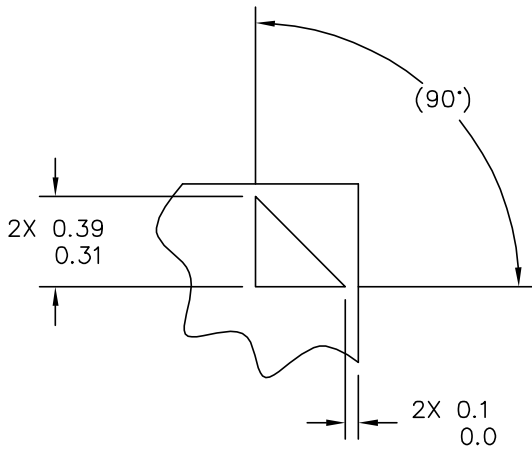
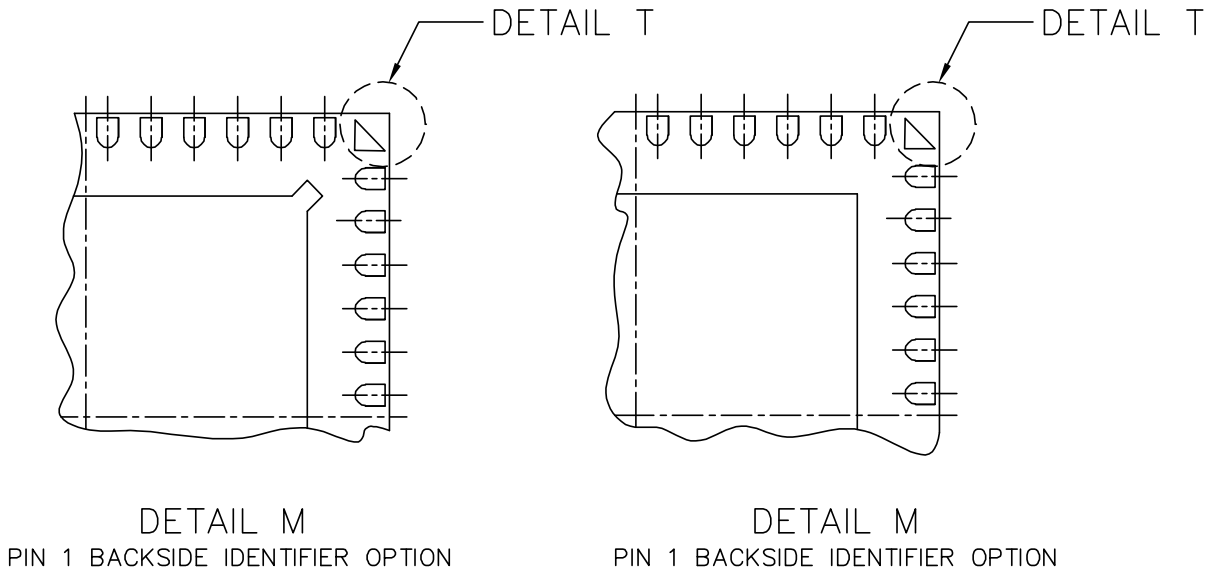
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE		DOCUMENT NO: 98ASS23234W		REV: D	
		CASE NUMBER: 840F-02		06 APR 2005	
		STANDARD: JEDEC MS-026 BCD			

Figure 29. 64-pin LQFP Package Drawing (Case 840F, Doc #98ASS23234W), Sheet 3 of 3



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TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)		DOCUMENT NO: 98ARH99048A		REV: F	
		CASE NUMBER: 1314-05		05 DEC 2005	
		STANDARD: JEDEC-MO-220 VKKD-2			

Figure 31. 48-pin QFN Package Drawing (Case 1314, Doc #98ARH99048A), Sheet 2 of 3

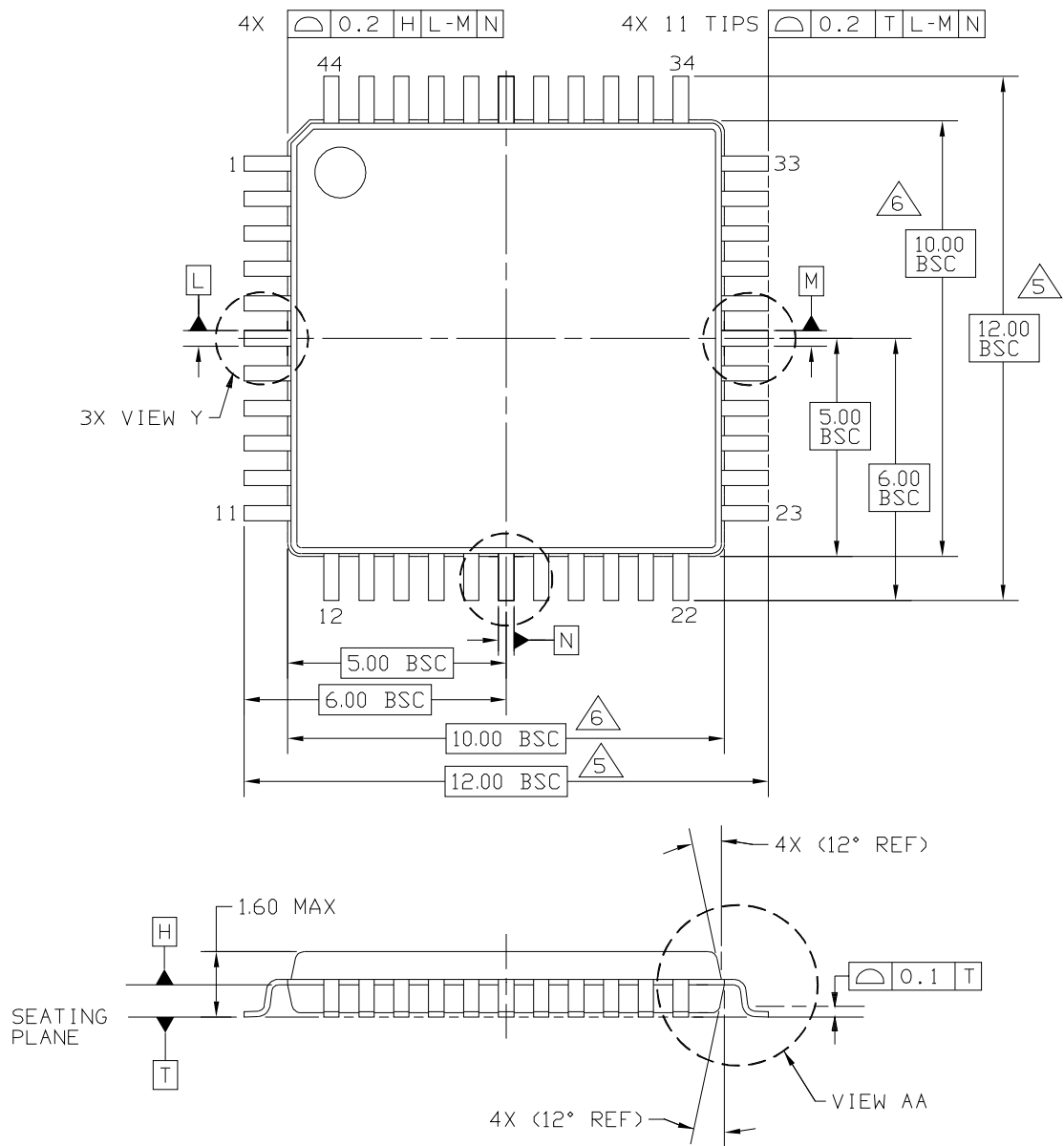


DETAIL T

- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFN.
 4. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
 5. MIN METAL GAP SHOULD BE 0.2MM.

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	TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)		DOCUMENT NO: 98ARH99048A CASE NUMBER: 1314-05 STANDARD: JEDEC-MO-220 VKKD-2	REV: F 05 DEC 2005

Figure 32. 48-pin QFN Package Drawing (Case 1314, Doc #98ARH99048A), Sheet 3 of 3



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TITLE: 44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK		DOCUMENT NO: 98ASS23225W		REV: D
		CASE NUMBER: 824D-02		26 FEB 2007
		STANDARD: JEDEC MS-026-BCB		

Figure 33. 44-pin LQFP Package Drawing (Case 824D, Doc #98ASS23225W), Sheet 1 of 3

6 Product Documentation

Find the most current versions of all documents at: <http://www.freescale.com>

Reference Manual (MC9S08QE128RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

7 Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web are the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://www.freescale.com>

The following revision history table summarizes changes contained in this document.

Table 22. Revision History

Revision	Date	Description of Changes
4	9 Nov 2007	Replaced 44 QFP package with 44 LQFP package.
		Changed ACMP electricals, V_{AIO} specification's test category from P to C.
5	28 May 2008	Updated the tables Thermal Characteristics , DC Characteristics , Supply Current Characteristics , XOSC and ICS Specifications (Temperature Range = -40 to 85°C Ambient) , ICS Frequency Specifications (Temperature Range = -40 to 85°C Ambient) , Control Timing , and Analog Comparator Electrical Specifications , 12-bit ADC Characteristics (VREFH = VDDAD, VREFL = VSSAD) Updated the figures Typical Run IDD for FBE and FEI, IDD vs. VDD (ACMP and ADC off, All Other Modules Enabled) , Deviation of DCO Output from Trimmed Frequency (50.33 MHz, 3.0 V) , and Deviation of DCO Output from Trimmed Frequency (50.33 MHz, 25°C)
6	24 Jun 2008	Updated the table Thermal Characteristics Updated the row corresponding to Num 18 in the table DC Characteristics Updated the tables MC9S08QE128 Series Features by MCU and Package , DC Characteristics , Supply Current Characteristics , Thermal Characteristics , Control Timing , and Ordering Information Updated the figures Typical Run IDD for FBE and FEI, IDD vs. VDD (ADC off, All Other Modules Enabled) , Deviation of DCO Output Across Temperature at VDD = 3.0 V , and Deviation of DCO Output Across VDD at 25°C
7	2 Oct 2008	Updated the Stop2 and Stop3 mode supply current in the Supply Current Characteristics table. Replaced the stop mode adders section from the Supply Current Characteristics with its own Stop Mode Adders table with new specifications.