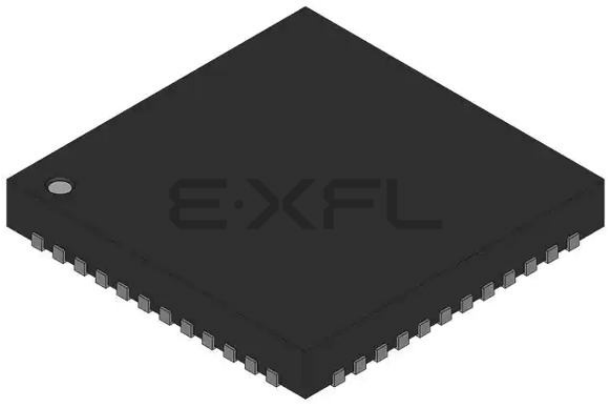

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	50MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08qe64cft

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

Freescale Semiconductor
Data Sheet: Technical Data

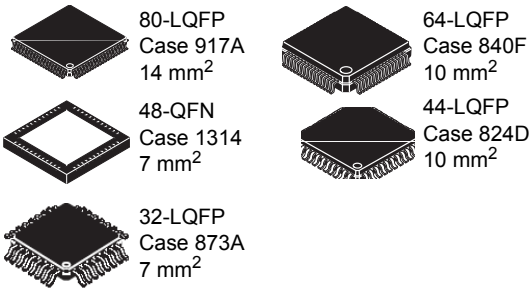
An Energy Efficient Solution by Freescale

Document Number: MC9S08QE128
Rev. 7, 10/2008

MC9S08QE128 Series

Covers: MC9S08QE128, MC9S08QE96, MC9S08QE64

MC9S08QE128



- 8-Bit HCS08 Central Processor Unit (CPU)
  - Up to 50.33-MHz HCS08 CPU above 2.4V, 40-MHz CPU above 2.1V, and 20-MHz CPU above 1.8V, across temperature range
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Flash read/program/erase over full operating voltage and temperature
  - Random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two low power stop modes; reduced power wait mode
  - Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode
  - Very low power external oscillator can be used in stop3 mode to provide accurate clock to active peripherals
  - Very low power real time counter for use in run, wait, and stop modes with internal and external clock sources
  - 6 µs typical wake up time from stop modes
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — FLL controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation; supports CPU freq. from 2 to 50.33 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints)
  - On-chip in-circuit emulator (ICE) debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints.
- ADC — 24-channel, 12-bit resolution; 2.5 µs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6V to 1.8V
- ACMPx — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; outputs can be optionally routed to TPM module; operation in stop3
- SCIx — Two SCIs with full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake up on active edge
- SPIx— Two serial peripheral interfaces with Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; MSB-first or LSB-first shifting
- IICx — Two IICs with; Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10 bit addressing
- TPMx — One 6-channel and two 3-channel; Selectable input capture, output compare, or buffered edge- or center-aligned PWMs on each channel
- RTC — 8-bit modulus counter with binary or decimal based prescaler; External clock source for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components
- Input/Output
  - 70 GPIOs and 1 input-only and 1 output-only pin
  - 16 KBI interrupts with selectable polarity
  - Hysteresis and configurable pull-up device on all input pins; Configurable slew rate and drive strength on all output pins.
  - SET/CLR registers on 16 pins (PTC and PTE)

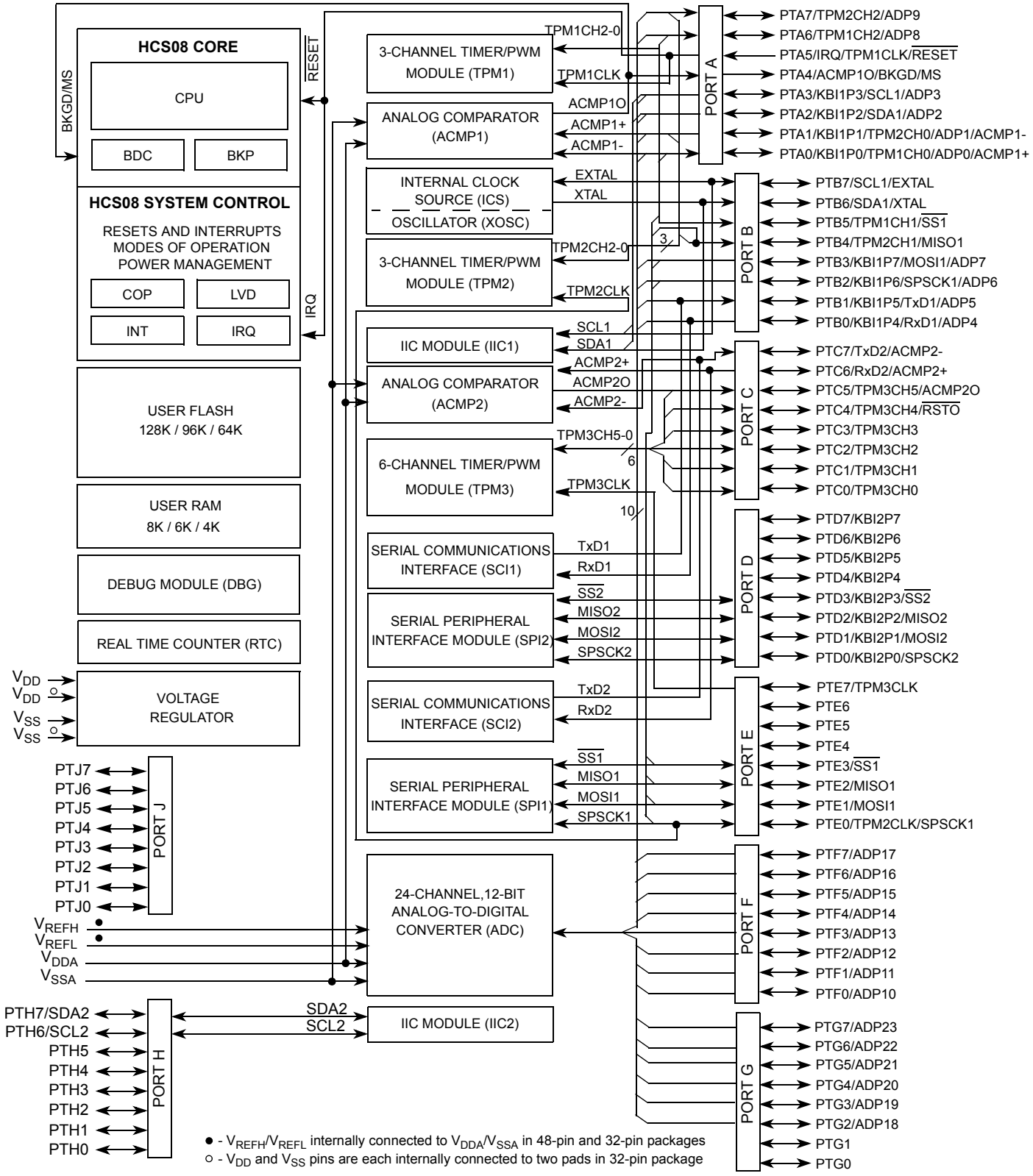


Figure 1. MC9S08QE128 Series Block Diagram

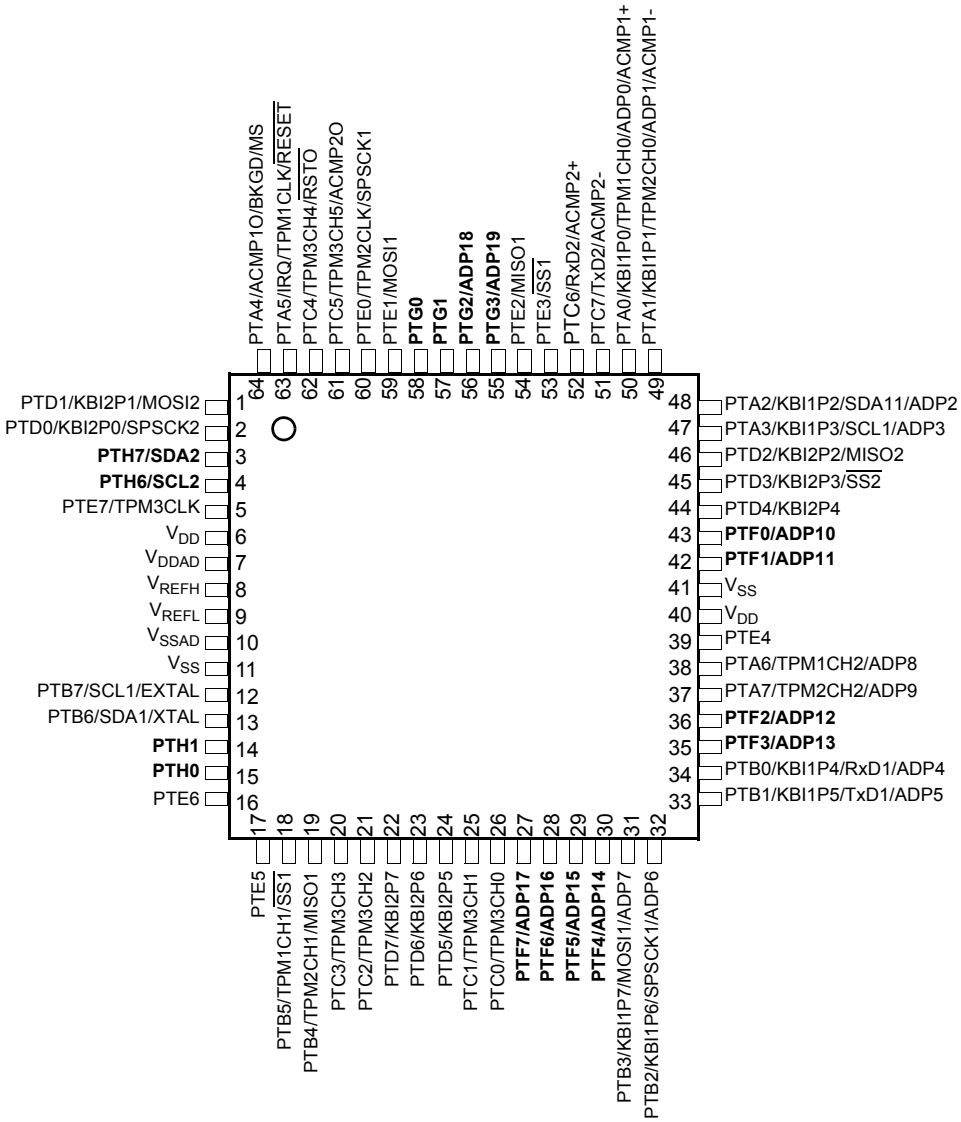
1 MC9S08QE128 Series Comparison

The following table compares the various device derivatives available within the MC9S08QE128 series.

Table 1. MC9S08QE128 Series Features by MCU and Package

Feature	MC9S08QE128				MC9S08QE96				MC9S08QE64			
Flash size (bytes)	131072				98304				65536			
RAM size (bytes)	8064				6016				4096			
Pin quantity	80	64	48	44	80	64	48	44	64	48	44	32
ACMP1	yes											
ACMP2	yes											
ADC channels	24	22	10	10	24	22	10	10	22	10	10	10
DBG	yes											
ICS	yes											
IIC1	yes											
IIC2	yes	yes	no	no	yes	yes	no	no	yes	no	no	no
IRQ	yes											
KBI	16	16	16	16	16	16	16	16	16	16	16	12
Port I/O[1]	70	54	38	34	70	54	38	34	54	38	34	26
RTC	yes											
SCI1	yes											
SCI2	yes											
SPI1	yes											
SPI2	yes											
TPM1 channels	3											
TPM2 channels	3											
TPM3 channels	6											
XOSC	yes											

[1] Port I/O count does not include the input only PTA5/IRQ/TPM1CLK/$\overline{\text{RESET}}$ or the output only PTA4/ACMP1O/BKGD/MS.



Pins in **bold** are added from the next smaller package.

Figure 3. Pin Assignments in 64-Pin LQFP Package

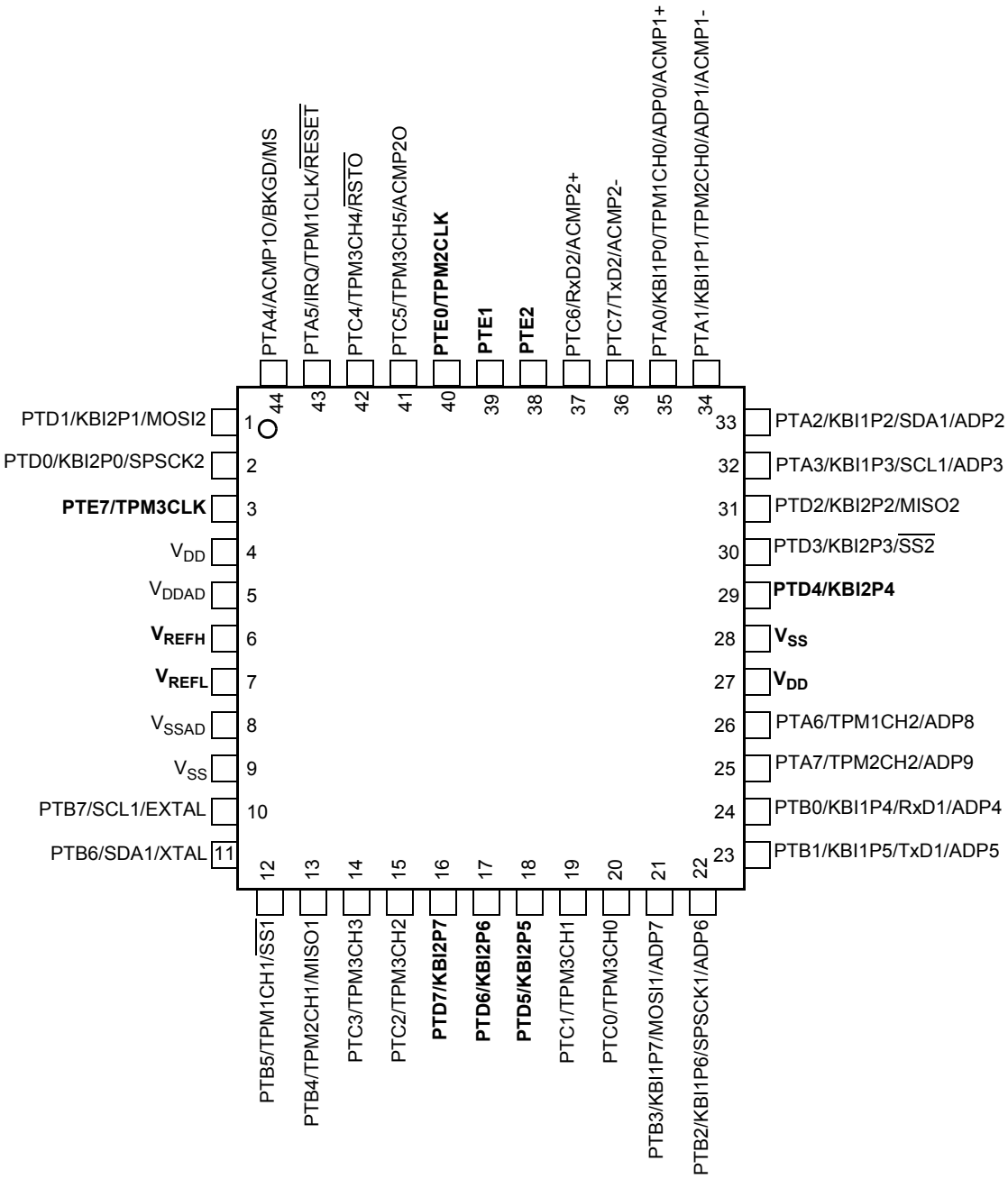


Figure 5. Pin Assignments in 44-Pin LQFP Package

Table 2. MC9S08QE128 Series Pin Assignment by Package and Pin Count (continued)

Pin Number					Lowest ← Priority → Highest				
80	**64**	**48**	**44**	**32**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
41	33	25	23	17	PTB1	KBI1P5	TxD1		ADP5
42	34	26	24	18	PTB0	KBI1P4	RxD1		ADP4
43	—	—	—	—	PTJ3				
44	—	—	—	—	PTJ2				
45	35	—	—	—	PTF3				ADP13
46	36	—	—	—	PTF2				ADP12
47	37	27	25	19	PTA7	TPM2CH2			ADP9
48	38	28	26	20	PTA6	TPM1CH2			ADP8
49	39	29	—	—	PTE4				
50	40	30	27	—					V_{DD}
51	41	31	28	—					V_{SS}
52	42	—	—	—	PTF1				ADP11
53	43	—	—	—	PTF0				ADP10
54	—	—	—	—	PTJ1				
55	—	—	—	—	PTJ0				
56	44	32	29	—	PTD4	KBI2P4			
57	45	33	30	21	PTD3	KBI2P3	$\overline{SS2}$		
58	46	34	31	22	PTD2	KBI2P2	MISO2		
59	47	35	32	23	PTA3	KBI1P3	SCL1		ADP3
60	48	36	33	24	PTA2	KBI1P2	SDA1		ADP2
61	49	37	34	25	PTA1	KBI1P1	TPM2CH0	ADP1	ACMP1-
62	50	38	35	26	PTA0	KBI1P0	TPM1CH0	ADP0	ACMP1+
63	51	39	36	27	PTC7	TxD2			ACMP2-
64	52	40	37	28	PTC6	RxD2			ACMP2+
65	—	—	—	—	PTG7				ADP23
66	—	—	—	—	PTG6				ADP22
67	—	—	—	—	PTG5				ADP21
68	—	—	—	—	PTG4				ADP20
69	53	41	—	—	PTE3	$\overline{SS1}$			
70	54	42	38	—	PTE2	MISO1			
71	55	—	—	—	PTG3				ADP19
72	56	—	—	—	PTG2				ADP18
73	57	—	—	—	PTG1				
74	58	—	—	—	PTG0				
75	59	43	39	—	PTE1	MOSI1			
76	60	44	40	—	PTE0	TPM2CLK	SPSCK1		
77	61	45	41	29	PTC5	TPM3CH5			ACMP2O
78	62	46	42	30	PTC4	TPM3CH4	$\overline{RSTO}$		
79	63	47	43	31	PTA5	IRQ	TPM1CLK	$\overline{RESET}$	
80	64	48	44	32	PTA4	ACMP1O	BKGD	MS	

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 6. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	
Latch-up	Minimum input voltage limit		– 2.5	V
	Maximum input voltage limit		7.5	V

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	± 2000	—	V
2	Machine model (MM)	V_{MM}	± 200	—	V
3	Charge device model (CDM)	V_{CDM}	± 500	—	V
4	Latch-up current at T_A = 85°C	I_{LAT}	± 100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
18	P	Low-voltage detection threshold — low range[7]	V_{LVDL}	V_{DD} falling V_{DD} rising	1.80 1.86	1.82 1.90	1.91 1.99	V
19	P	Low-voltage warning threshold — high range[7]	V_{LVWH}	V_{DD} falling V_{DD} rising	2.36 2.36	2.46 2.46	2.56 2.56	V
20	P	Low-voltage warning threshold — low range[7]	V_{LVWL}	V_{DD} falling V_{DD} rising	2.11 2.16	2.16 2.21	2.22 2.27	V
21	C	Low-voltage inhibit reset/recover hysteresis[7]	V_{hys}		—	50	—	mV
22	P	Bandgap Voltage Reference[9]	V_{BG}		1.15	1.17	1.18	V

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 Maximum is highest voltage that POR is guaranteed.

7 Low voltage detection and warning limits measured at 1 MHz bus frequency.

8 Run at 1 MHz bus frequency

9 Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

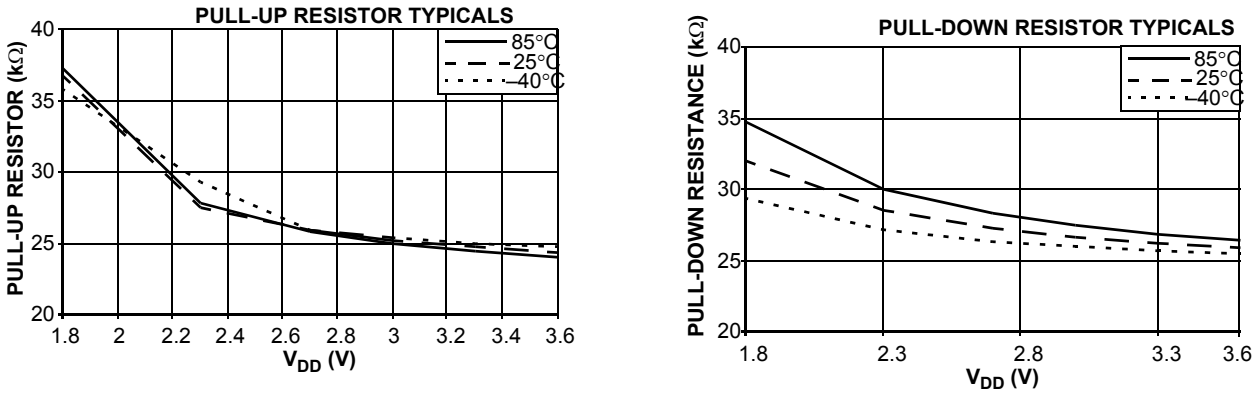


Figure 7. Pull-up and Pull-down Typical Resistor Values

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
6	P	Stop2 mode supply current	$S2I_{DD}$	n/a	3	0.35	0.6	μA	-40 to 25
	C					0.98	2.0		70
	P					2.5	7.5		85
	C				2	0.25	0.5		-40 to 25
	C					1.4	1.9		70
	C					1.91	6.5		85
7	P	Stop3 mode supply current No clocks active	$S3I_{DD}$	n/a	3	0.45	1.0	μA	-40 to 25
	C					1.99	4.2		70
	P					5.0	15.0		85
	C				2	0.35	0.7		-40 to 25
	C					2.9	3.9		70
	C					3.77	13.2		85

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

Table 10. Stop Mode Adders

Num	C	Parameter	Condition	Temperature (°C)				Units
				-40	25	70	85	
1	T	LPO		50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN[1]		63	70	77	81	uA
4	T	RTC	does not include clock source current	50	75	100	150	nA
5	T	LVD[1]	LVDSE = 1	90	100	110	115	uA
6	T	ACMP[1]	not using the bandgap (BGBE = 0)	18	20	22	23	uA
7	T	ADC[1]	ADLPC = ADLSMP = 1 not using the bandgap (BGBE = 0)	95	106	114	120	uA

1 Not available in stop2 mode.

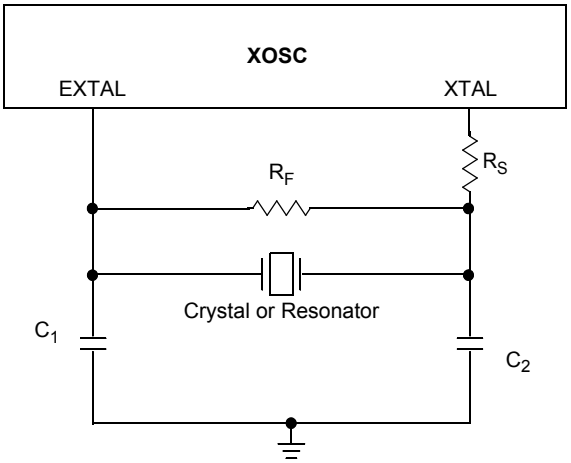


Figure 13. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

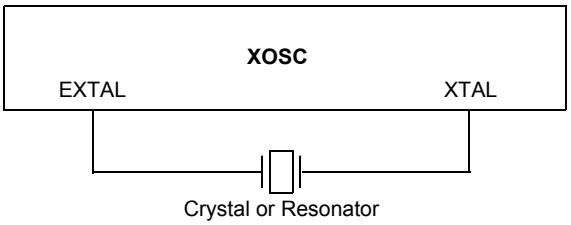


Figure 14. Typical Crystal or Resonator Circuit: Low Range/Low Gain

3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at V_{DD} = 3.6 V and temperature = 25°C		f_{int_ft}	—	32.768	—	kHz
2	P	Internal reference frequency — user trimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time		t_{IRST}	—	60	100	µs
4	P	DCO output frequency range — trimmed [2]	Low range (DRS=00)	f_{dco_u}	16	—	20	MHz
	P		Mid range (DRS=01)		32	—	40	
	P		High range (DRS=10)		48	—	60	
5	P	DCO output frequency [2] Reference = 32768 Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS=01)		—	39.85	—	
	P		High range (DRS=10)		—	59.77	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
8	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 -1.0	± 2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C	Δf_{dco_t}	—	± 0.5	± 1	$\%f_{dco}$
10	C	FLL acquisition time [3]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval) [4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

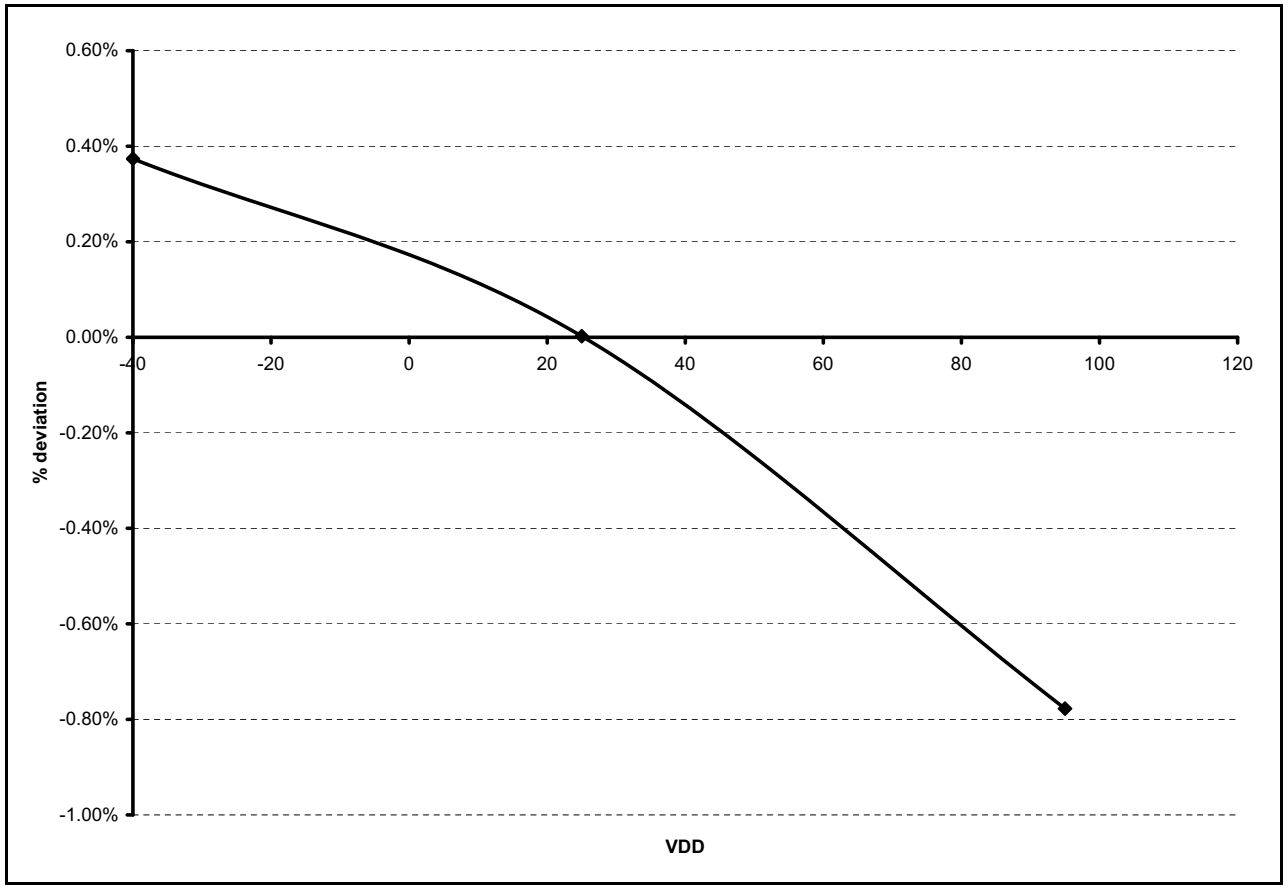


Figure 15. Deviation of DCO Output Across Temperature at V_{DD} = 3.0 V

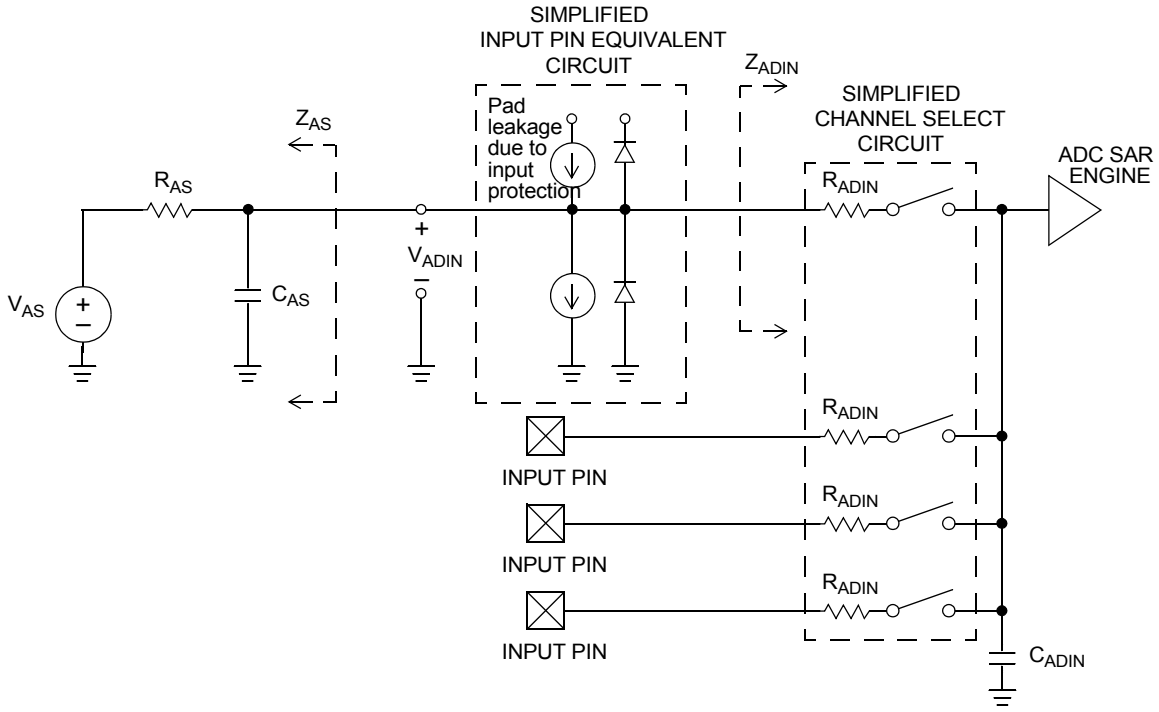


Figure 25. ADC Input Impedance Equivalency Diagram

Table 18. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Supply Current ADLPC=1 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	120	—	μA	
Supply Current ADLPC=1 ADLSMP=0 ADCO=1		T	I_{DDAD}	—	202	—	μA	
Supply Current ADLPC=0 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	288	—	μA	
Supply Current ADLPC=0 ADLSMP=0 ADCO=1		D	I_{DDAD}	—	0.532	1	mA	
Supply Current	Stop, Reset, Module Off	P	I_{DDAD}	—	0.007	0.8	μA	
ADC Asynchronous Clock Source	High Speed (ADLPC=0)	P	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
	Low Power (ADLPC=1)	P		1.25	2	3.3		

4 Ordering Information

This section contains ordering information for MC9S08QE128, MC9S08QE96, and MC9S08QE64 devices.

Table 20. Ordering Information

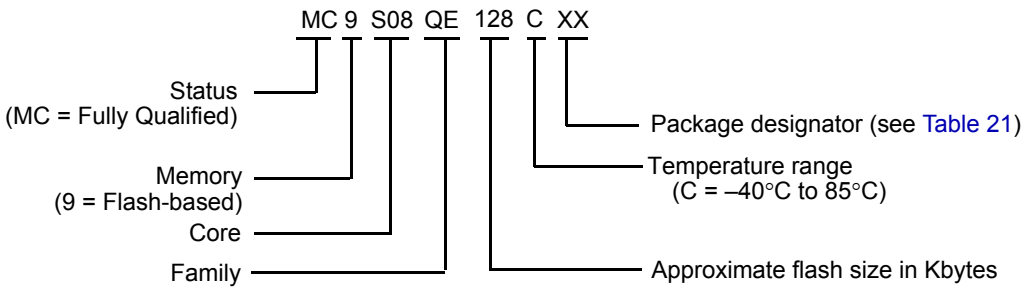
Freescale Part Number[1]	Memory		Temperature range (°C)	Package[2]
	Flash	RAM		
MC9S08QE128CLK	128K	8K	-40 to +85	80 LQFP
MC9S08QE128CLH			-40 to +85	64 LQFP
MC9S08QE128CFT			-40 to +85	48 QFN
MC9S08QE128CLD			-40 to +85	44 LQFP
MC9S08QE96CLK	96K	6K	-40 to +85	80 LQFP
MC9S08QE96CLH			-40 to +85	64 LQFP
MC9S08QE96CFT			-40 to +85	48 QFN
MC9S08QE96CLD			-40 to +85	44 QFP
MC9S08QE64CLH	64K	4K	-40 to +85	64 LQFP
MC9S08QE64CFT			-40 to +85	48 QFN
MC9S08QE64CLD			-40 to +85	44 QFP
MC9S08QE64CLC			-40 to +85	32 LQFP

1 See the reference manual, *MC9S08QE128RM*, for a complete description of modules included on each device.

2 See Table 21 for package information.

4.1 Device Numbering System

Example of the device numbering system:

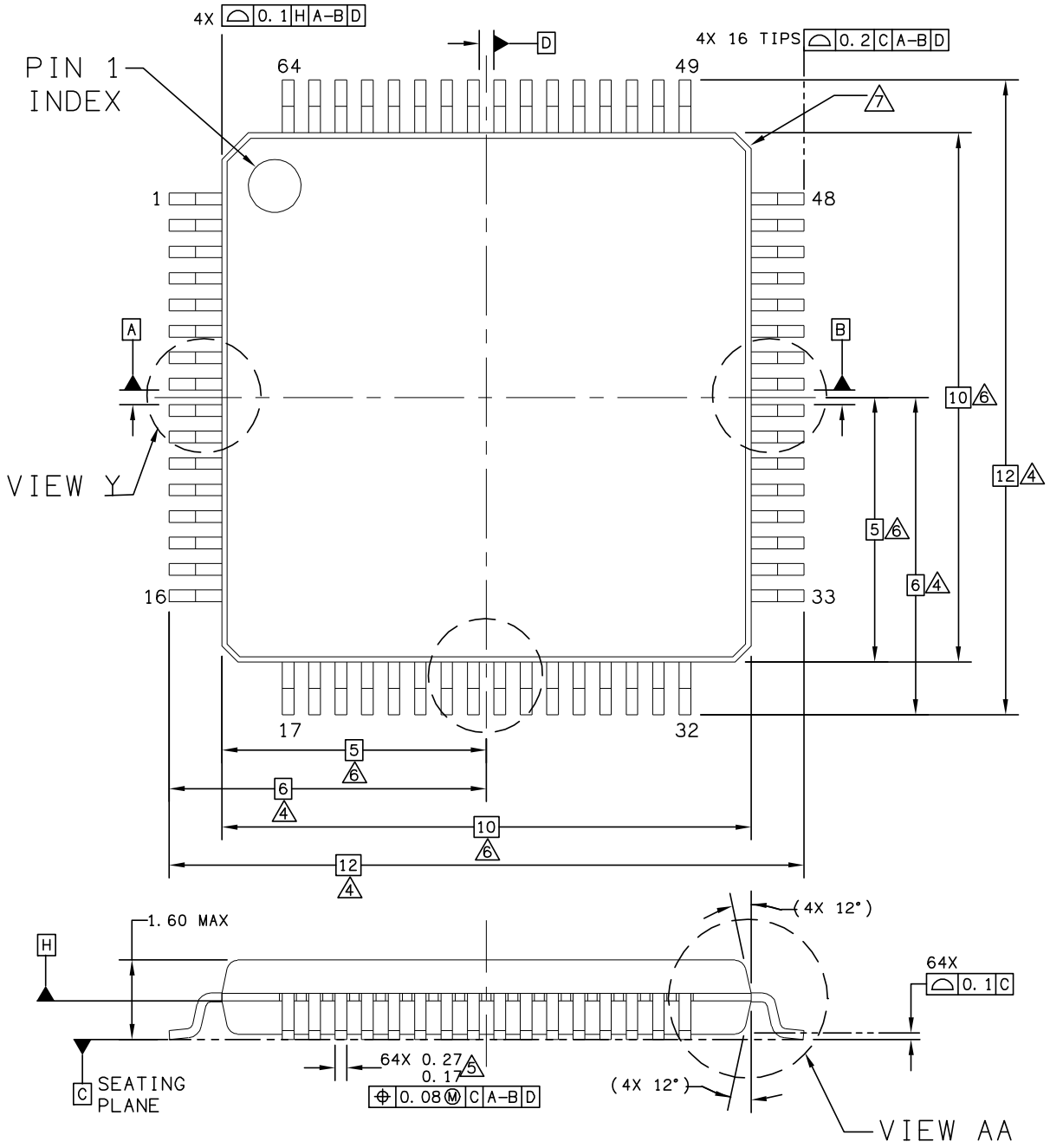


5 Package Information

The below table details the various packages available.

Table 21. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
80	Low Quad Flat Package	LQFP	LK	917A	98ASS23237W
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W
48	Quad Flat No-Leads	QFN	FT	1314	98ARH99048A
44	Low Quad Flat Package	LQFP	LD	824D	98ASS23225W
32	Low Quad Flat Package	LQFP	LC	873A	98ASH70029A



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TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D
	CASE NUMBER: 840F-02	06 APR 2005
	STANDARD: JEDEC MS-026 BCD	

Figure 27. 64-pin LQFP Package Drawing (Case 840F, Doc #98ASS23234W), Sheet 1 of 3

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

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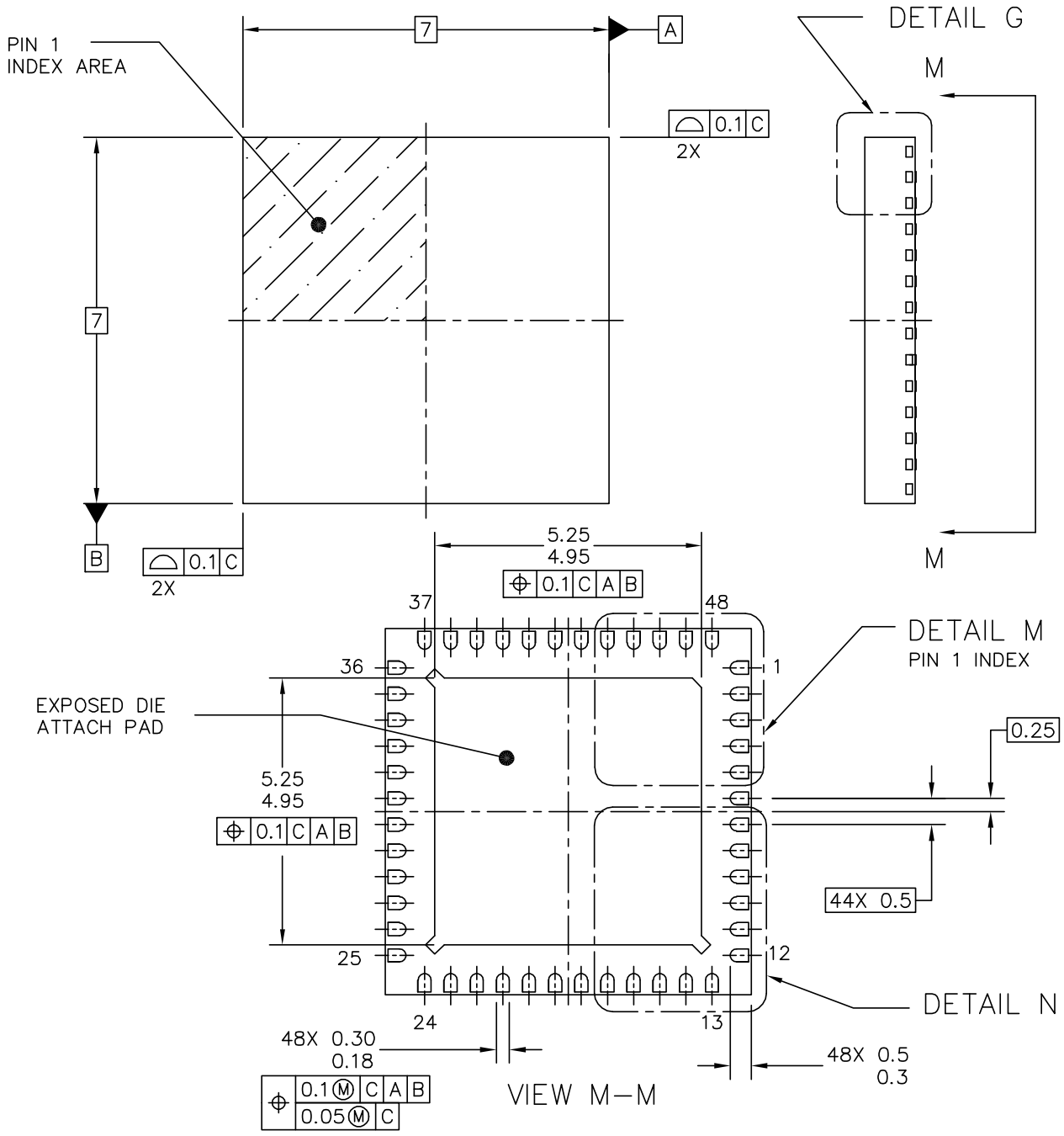
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D	
	CASE NUMBER: 840F-02	06 APR 2005	
	STANDARD: JEDEC MS-026 BCD		

Figure 29. 64-pin LQFP Package Drawing (Case 840F, Doc #98ASS23234W), Sheet 3 of 3



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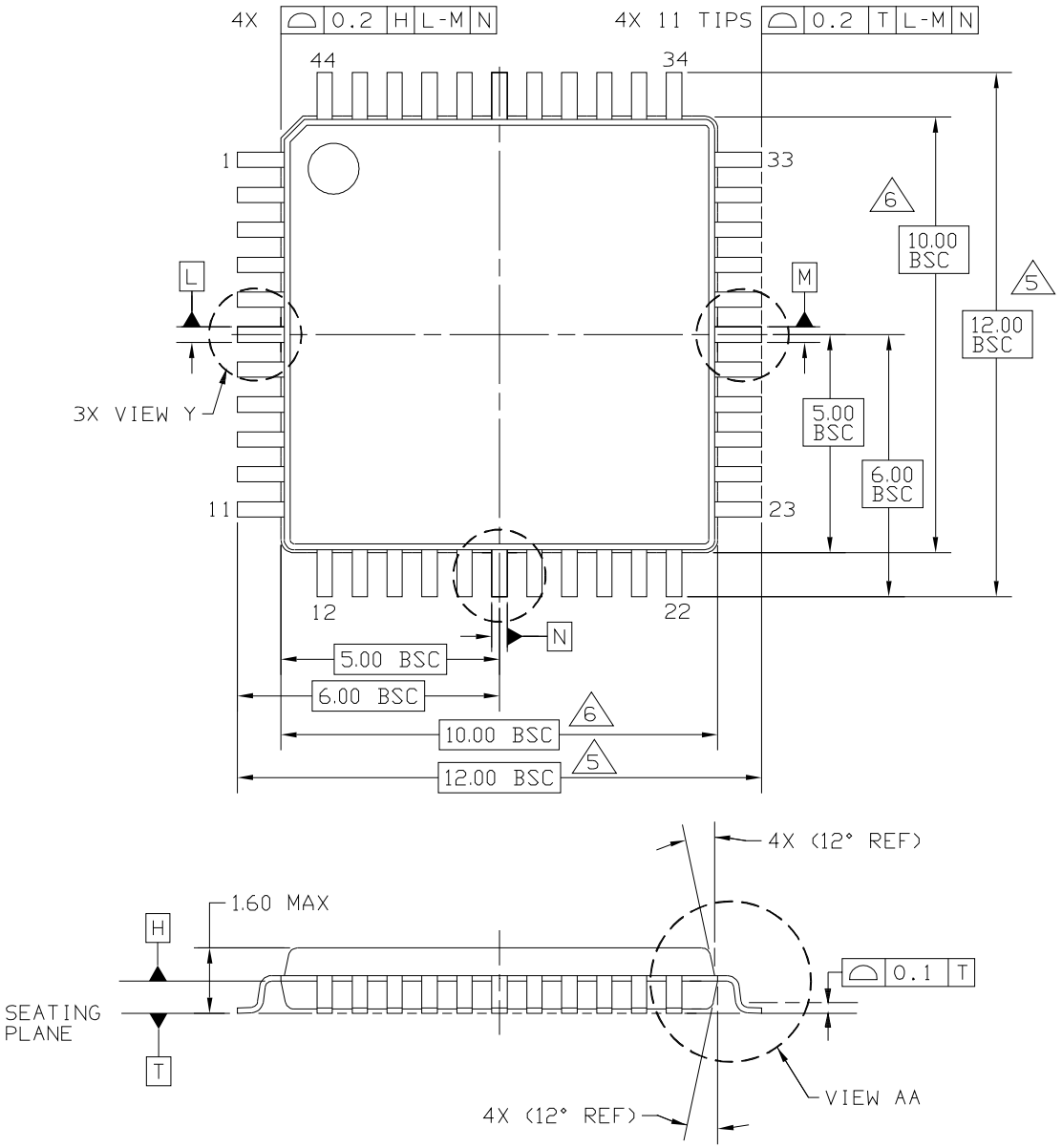
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARH99048A	REV: F
	CASE NUMBER: 1314–05	05 DEC 2005
	STANDARD: JEDEC–MO–220 VKKD–2	

Figure 30. 48-pin QFN Package Drawing (Case 1314, Doc #98ARH99048A), Sheet 1 of 3



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TITLE: 44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23225W	REV: D
	CASE NUMBER: 824D-02	26 FEB 2007
	STANDARD: JEDEC MS-026-BCB	

Figure 33. 44-pin LQFP Package Drawing (Case 824D, Doc #98ASS23225W), Sheet 1 of 3

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: MILLIMETER

3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4. DATUMS L, M AND N TO BE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE T.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE DIMENSION TO EXCEED 0.53. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

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TITLE: 44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23225W	REV: D
	CASE NUMBER: 824D-02	26 FEB 2007
	STANDARD: JEDEC MS-026 BCB	

Figure 35. 44-pin LQFP Package Drawing (Case 824D, Doc #98ASS23225W), Sheet 3 of 3

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