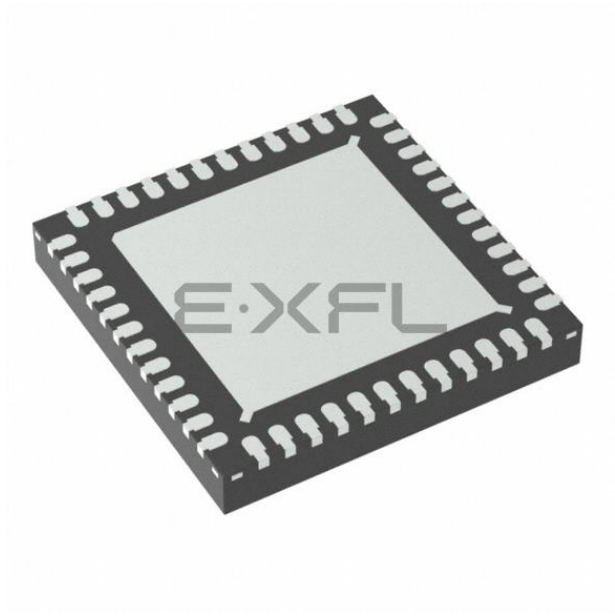

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	50MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	38
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08qe96cftr

Freescale Semiconductor
Data Sheet: Technical Data

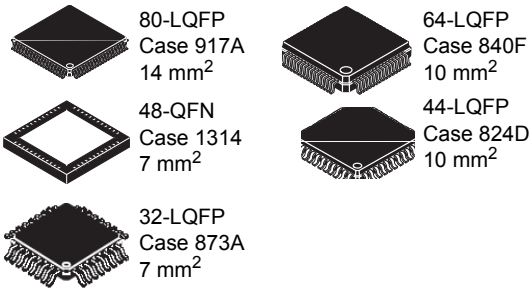
An Energy Efficient Solution by Freescale

Document Number: MC9S08QE128
Rev. 7, 10/2008

MC9S08QE128 Series

Covers: MC9S08QE128, MC9S08QE96, MC9S08QE64

MC9S08QE128



- 8-Bit HCS08 Central Processor Unit (CPU)
  - Up to 50.33-MHz HCS08 CPU above 2.4V, 40-MHz CPU above 2.1V, and 20-MHz CPU above 1.8V, across temperature range
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Flash read/program/erase over full operating voltage and temperature
  - Random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two low power stop modes; reduced power wait mode
  - Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode
  - Very low power external oscillator can be used in stop3 mode to provide accurate clock to active peripherals
  - Very low power real time counter for use in run, wait, and stop modes with internal and external clock sources
  - 6 µs typical wake up time from stop modes
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — FLL controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation; supports CPU freq. from 2 to 50.33 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints)
  - On-chip in-circuit emulator (ICE) debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints.
- ADC — 24-channel, 12-bit resolution; 2.5 µs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6V to 1.8V
- ACMPx — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; outputs can be optionally routed to TPM module; operation in stop3
- SCIx — Two SCIs with full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake up on active edge
- SPIx— Two serial peripheral interfaces with Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; MSB-first or LSB-first shifting
- IICx — Two IICs with; Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10 bit addressing
- TPMx — One 6-channel and two 3-channel; Selectable input capture, output compare, or buffered edge- or center-aligned PWMs on each channel
- RTC — 8-bit modulus counter with binary or decimal based prescaler; External clock source for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components
- Input/Output
  - 70 GPIOs and 1 input-only and 1 output-only pin
  - 16 KBI interrupts with selectable polarity
  - Hysteresis and configurable pull-up device on all input pins; Configurable slew rate and drive strength on all output pins.
  - SET/CLR registers on 16 pins (PTC and PTE)

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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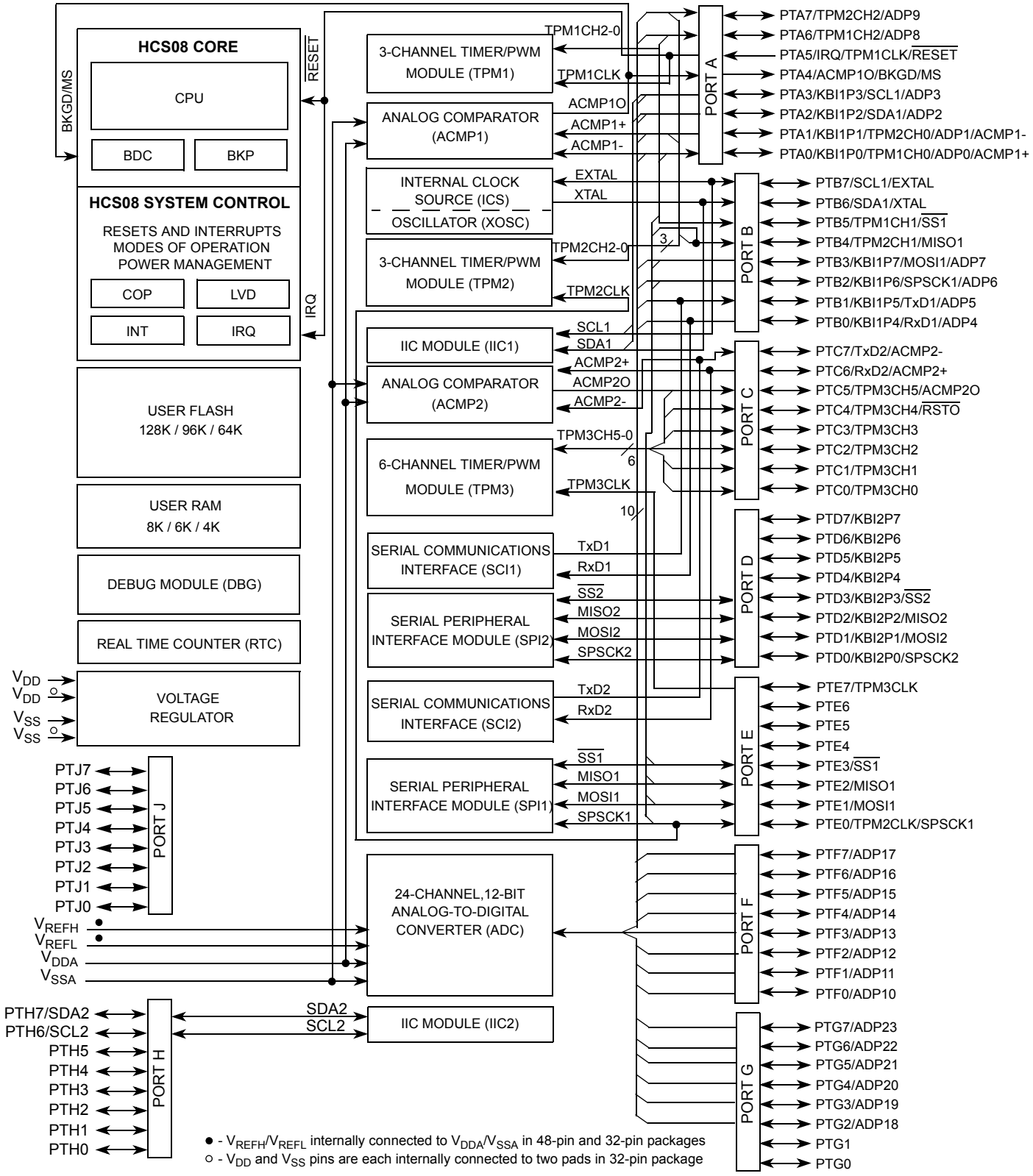


Figure 1. MC9S08QE128 Series Block Diagram

1 MC9S08QE128 Series Comparison

The following table compares the various device derivatives available within the MC9S08QE128 series.

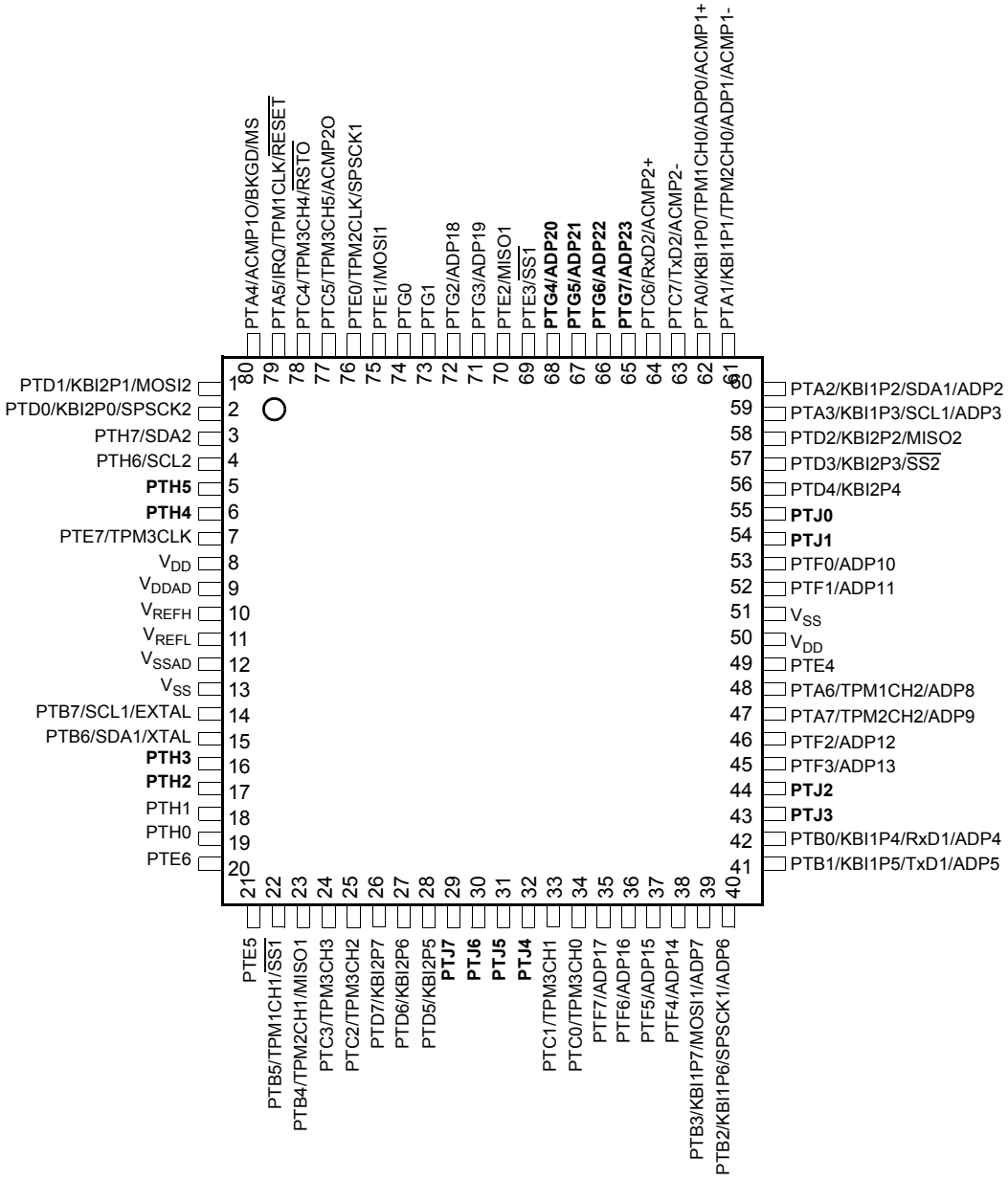
Table 1. MC9S08QE128 Series Features by MCU and Package

Feature	MC9S08QE128				MC9S08QE96				MC9S08QE64			
Flash size (bytes)	131072				98304				65536			
RAM size (bytes)	8064				6016				4096			
Pin quantity	80	64	48	44	80	64	48	44	64	48	44	32
ACMP1	yes											
ACMP2	yes											
ADC channels	24	22	10	10	24	22	10	10	22	10	10	10
DBG	yes											
ICS	yes											
IIC1	yes											
IIC2	yes	yes	no	no	yes	yes	no	no	yes	no	no	no
IRQ	yes											
KBI	16	16	16	16	16	16	16	16	16	16	16	12
Port I/O[1]	70	54	38	34	70	54	38	34	54	38	34	26
RTC	yes											
SCI1	yes											
SCI2	yes											
SPI1	yes											
SPI2	yes											
TPM1 channels	3											
TPM2 channels	3											
TPM3 channels	6											
XOSC	yes											

[1] Port I/O count does not include the input only PTA5/IRQ/TPM1CLK/$\overline{\text{RESET}}$ or the output only PTA4/ACMP1O/BKGD/MS.

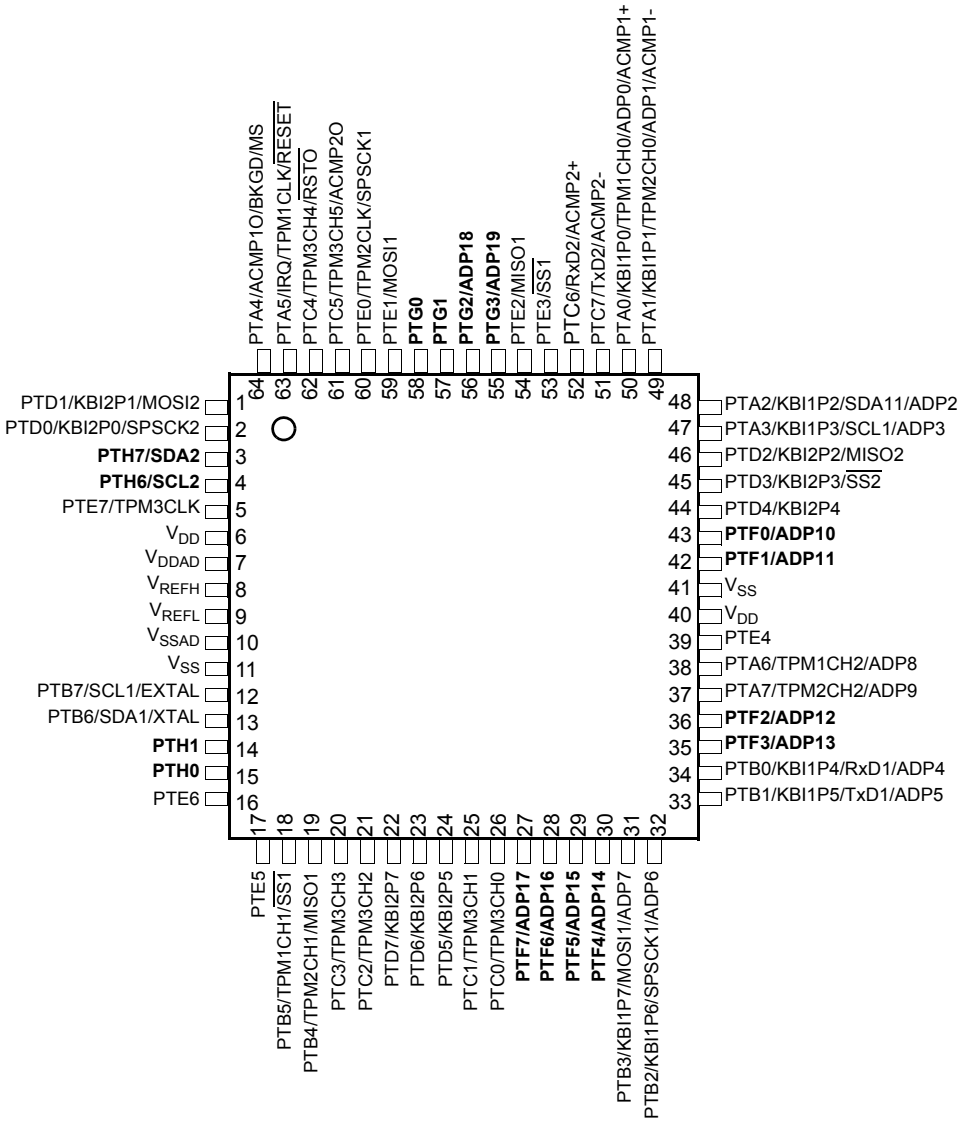
2 Pin Assignments

This section describes the pin assignments for the available packages. See Table 2 for pin availability by package pin-count.



Pins in **bold** are added from the next smaller package.

Figure 2. Pin Assignments in 80-Pin LQFP



Pins in **bold** are added from the next smaller package.

Figure 3. Pin Assignments in 64-Pin LQFP Package

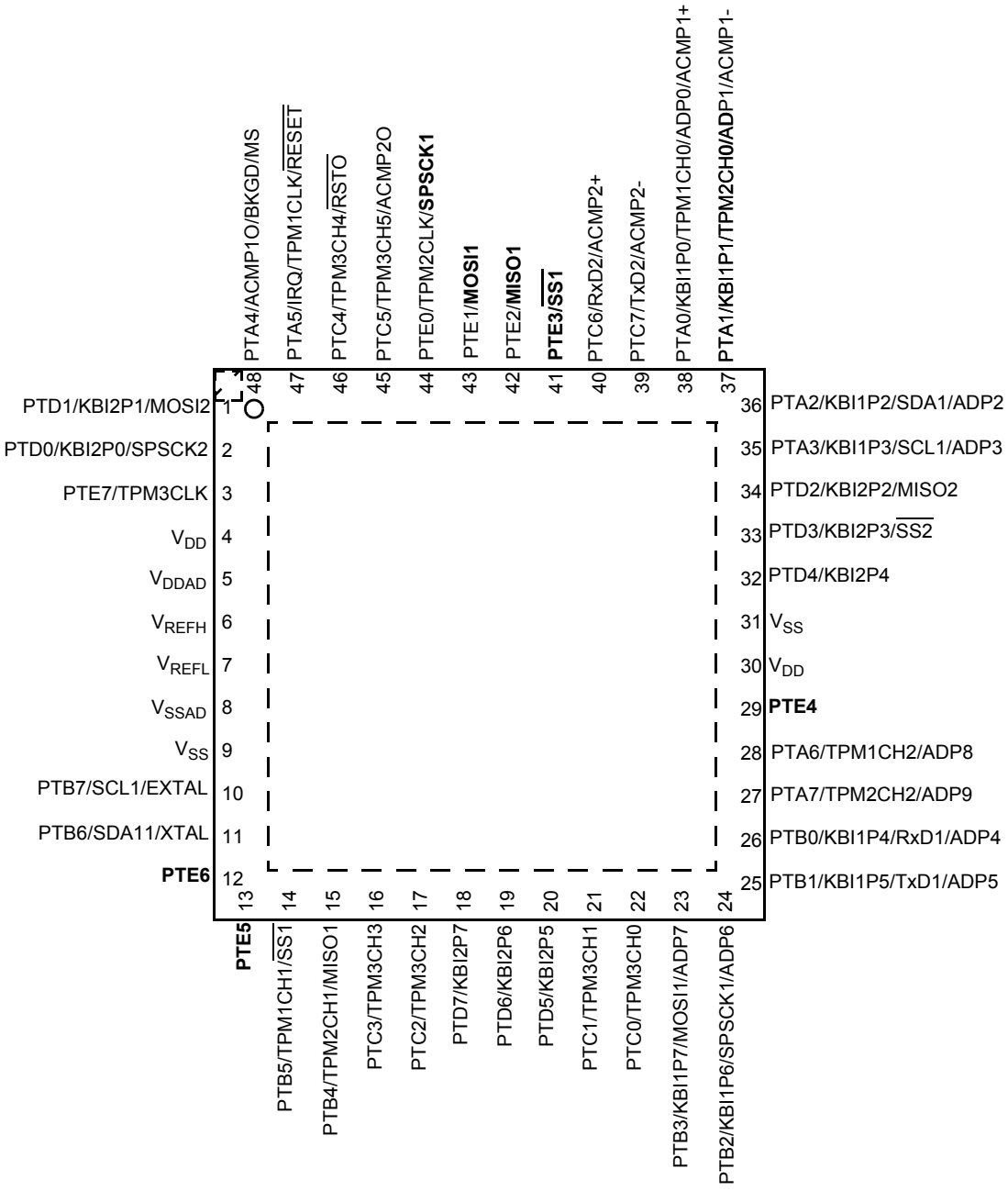


Figure 4. Pin Assignments in 48-Pin QFN Package

Table 2. MC9S08QE128 Series Pin Assignment by Package and Pin Count

Pin Number					Lowest ←		Priority →		Highest
80	**64**	**48**	**44**	**32**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	1	1	1	1	PTD1	KBI2P1	MOSI2		
2	2	2	2	2	PTD0	KBI2P0	SPSCK2		
3	3	—	—	—	PTH7	SDA2			
4	4	—	—	—	PTH6	SCL2			
5	—	—	—	—	PTH5				
6	—	—	—	—	PTH4				
7	5	3	3	—	PTE7	TPM3CLK			
8	6	4	4	3					V_{DD}
9	7	5	5	4					V_{DDA}
10	8	6	6	—					V_{REFH}
11	9	7	7	—					V_{REFL}
12	10	8	8	5					V_{SSA}
13	11	9	9	6					V_{SS}
14	12	10	10	7	PTB7	SCL1			EXTAL
15	13	11	11	8	PTB6	SDA1			XTAL
16	—	—	—	—	PTH3				
17	—	—	—	—	PTH2				
18	14	—	—	—	PTH1				
19	15	—	—	—	PTH0				
20	16	12	—	—	PTE6				
21	17	13	—	—	PTE5				
22	18	14	12	9	PTB5	TPM1CH1	$\overline{SS1}$		
23	19	15	13	10	PTB4	TPM2CH1	MISO1		
24	20	16	14	11	PTC3	TPM3CH3			
25	21	17	15	12	PTC2	TPM3CH2			
26	22	18	16	—	PTD7	KBI2P7			
27	23	19	17	—	PTD6	KBI2P6			
28	24	20	18	—	PTD5	KBI2P5			
29	—	—	—	—	PTJ7				
30	—	—	—	—	PTJ6				
31	—	—	—	—	PTJ5				
32	—	—	—	—	PTJ4				
33	25	21	19	13	PTC1	TPM3CH1			
34	26	22	20	14	PTC0	TPM3CH0			
35	27	—	—	—	PTF7				ADP17
36	28	—	—	—	PTF6				ADP16
37	29	—	—	—	PTF5				ADP15
38	30	—	—	—	PTF4				ADP14
39	31	23	21	15	PTB3	KBI1P7	MOSI1		ADP7
40	32	24	22	16	PTB2	KBI1P6	SPSCK1		ADP6

Table 2. MC9S08QE128 Series Pin Assignment by Package and Pin Count (continued)

Pin Number					Lowest ← Priority → Highest				
80	**64**	**48**	**44**	**32**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
41	33	25	23	17	PTB1	KBI1P5	TxD1		ADP5
42	34	26	24	18	PTB0	KBI1P4	RxD1		ADP4
43	—	—	—	—	PTJ3				
44	—	—	—	—	PTJ2				
45	35	—	—	—	PTF3				ADP13
46	36	—	—	—	PTF2				ADP12
47	37	27	25	19	PTA7	TPM2CH2			ADP9
48	38	28	26	20	PTA6	TPM1CH2			ADP8
49	39	29	—	—	PTE4				
50	40	30	27	—					V_{DD}
51	41	31	28	—					V_{SS}
52	42	—	—	—	PTF1				ADP11
53	43	—	—	—	PTF0				ADP10
54	—	—	—	—	PTJ1				
55	—	—	—	—	PTJ0				
56	44	32	29	—	PTD4	KBI2P4			
57	45	33	30	21	PTD3	KBI2P3	$\overline{SS2}$		
58	46	34	31	22	PTD2	KBI2P2	MISO2		
59	47	35	32	23	PTA3	KBI1P3	SCL1		ADP3
60	48	36	33	24	PTA2	KBI1P2	SDA1		ADP2
61	49	37	34	25	PTA1	KBI1P1	TPM2CH0	ADP1	ACMP1-
62	50	38	35	26	PTA0	KBI1P0	TPM1CH0	ADP0	ACMP1+
63	51	39	36	27	PTC7	TxD2			ACMP2-
64	52	40	37	28	PTC6	RxD2			ACMP2+
65	—	—	—	—	PTG7				ADP23
66	—	—	—	—	PTG6				ADP22
67	—	—	—	—	PTG5				ADP21
68	—	—	—	—	PTG4				ADP20
69	53	41	—	—	PTE3	$\overline{SS1}$			
70	54	42	38	—	PTE2	MISO1			
71	55	—	—	—	PTG3				ADP19
72	56	—	—	—	PTG2				ADP18
73	57	—	—	—	PTG1				
74	58	—	—	—	PTG0				
75	59	43	39	—	PTE1	MOSI1			
76	60	44	40	—	PTE0	TPM2CLK	SPSCK1		
77	61	45	41	29	PTC5	TPM3CH5			ACMP2O
78	62	46	42	30	PTC4	TPM3CH4	$\overline{RSTO}$		
79	63	47	43	31	PTA5	IRQ	TPM1CLK	$\overline{RESET}$	
80	64	48	44	32	PTA4	ACMP1O	BKGD	MS	

[3] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	–40 to 85	°C
Maximum junction temperature	T_{JM}	95	°C
Thermal resistance Single-layer board			
32-pin LQFP	θ_{JA}	82	°C/W
44-pin LQFP		68	
48-pin QFN		81	
64-pin LQFP	θ_{JA}	69	°C/W
80-pin LQFP		60	
Thermal resistance Four-layer board			
32-pin LQFP	θ_{JA}	54	°C/W
44-pin LQFP		46	
48-pin QFN		26	
64-pin LQFP	θ_{JA}	50	°C/W
80-pin LQFP		47	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
18	P	Low-voltage detection threshold — low range[7]	V_{LVDL}	V_{DD} falling V_{DD} rising	1.80 1.86	1.82 1.90	1.91 1.99	V
19	P	Low-voltage warning threshold — high range[7]	V_{LVWH}	V_{DD} falling V_{DD} rising	2.36 2.36	2.46 2.46	2.56 2.56	V
20	P	Low-voltage warning threshold — low range[7]	V_{LVWL}	V_{DD} falling V_{DD} rising	2.11 2.16	2.16 2.21	2.22 2.27	V
21	C	Low-voltage inhibit reset/recover hysteresis[7]	V_{hys}		—	50	—	mV
22	P	Bandgap Voltage Reference[9]	V_{BG}		1.15	1.17	1.18	V

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 Maximum is highest voltage that POR is guaranteed.

7 Low voltage detection and warning limits measured at 1 MHz bus frequency.

8 Run at 1 MHz bus frequency

9 Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

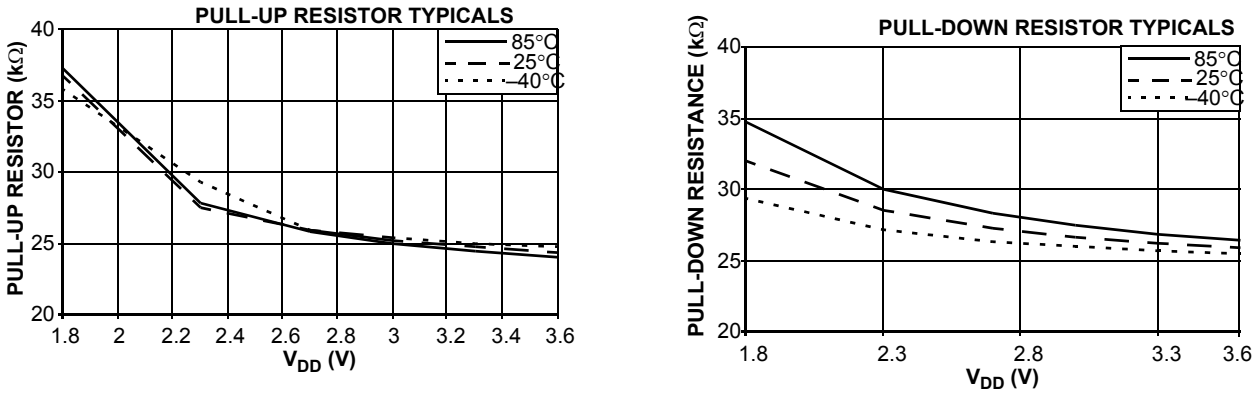


Figure 7. Pull-up and Pull-down Typical Resistor Values

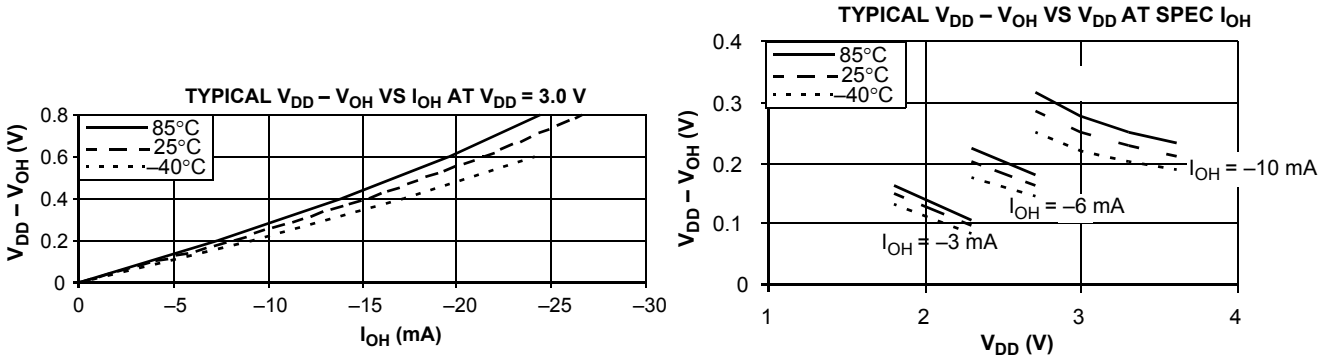


Figure 11. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	25.165 MHz	3	16	18	mA	–40 to 25
	P					16	20		85
	T			20 MHz		14.4	—		–40 to 85
	T			8 MHz		6.5	—		
	T			1 MHz		1.4	—		
2	C	Run supply current FEI mode, all modules off	RI_{DD}	25.165 MHz	3	11.5	12.3	mA	–40 to 85
	T			20 MHz		9.5	—		
	T			8 MHz		4.6	—		
	T			1 MHz		1.0	—		
3	T	Run supply current LPS=0, all modules off	RI_{DD}	16 kHz FBILP	3	152	—	µA	–40 to 85
	T			16 kHz FBELP		115	—		
4	T	Run supply current LPS=1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3	21.9	—	µA	0 to 70
							—		–40 to 85
	T	Run supply current LPS=1, all modules off, running from RAM				7.3	—		0 to 70
							—		–40 to 85
5	C	Wait mode supply current FEI mode, all modules off	WI_{DD}	25.165 MHz	3	5.74	6	mA	–-40 to 85
	T			20 MHz		4.57	—		
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		

3.8 External Oscillator (XOSC) Characteristics

Reference Figure 13 and Figure 14 for crystal or resonator circuits.

Table 11. XOSC and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1,C_2	See Note[2] See Note[3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, High Gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 0 100 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high power High range, low power High range, high power	 t_{CSTL} t_{CSTH} 	 — — — —	 200 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode FBELP mode	f_{extal}	0.03125 0	— —	40.0 50.33	MHz MHz

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

3 See crystal or resonator manufacturer's recommendation.

4 Proper PC board layout procedures must be followed to achieve specifications.

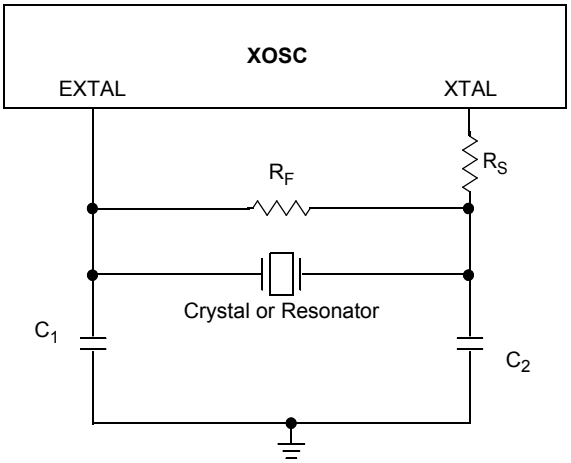


Figure 13. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

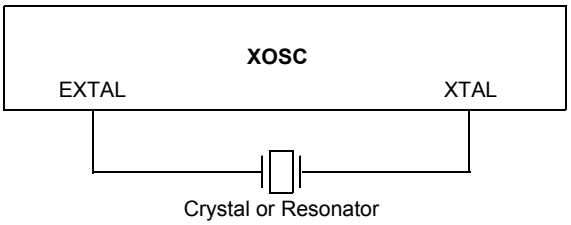


Figure 14. Typical Crystal or Resonator Circuit: Low Range/Low Gain

3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at V_{DD} = 3.6 V and temperature = 25°C		f_{int_ft}	—	32.768	—	kHz
2	P	Internal reference frequency — user trimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time		t_{IRST}	—	60	100	µs
4	P	DCO output frequency range — trimmed [2]	Low range (DRS=00)	f_{dco_u}	16	—	20	MHz
	P		Mid range (DRS=01)		32	—	40	
	P		High range (DRS=10)		48	—	60	
5	P	DCO output frequency [2] Reference = 32768 Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS=01)		—	39.85	—	
	P		High range (DRS=10)		—	59.77	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$

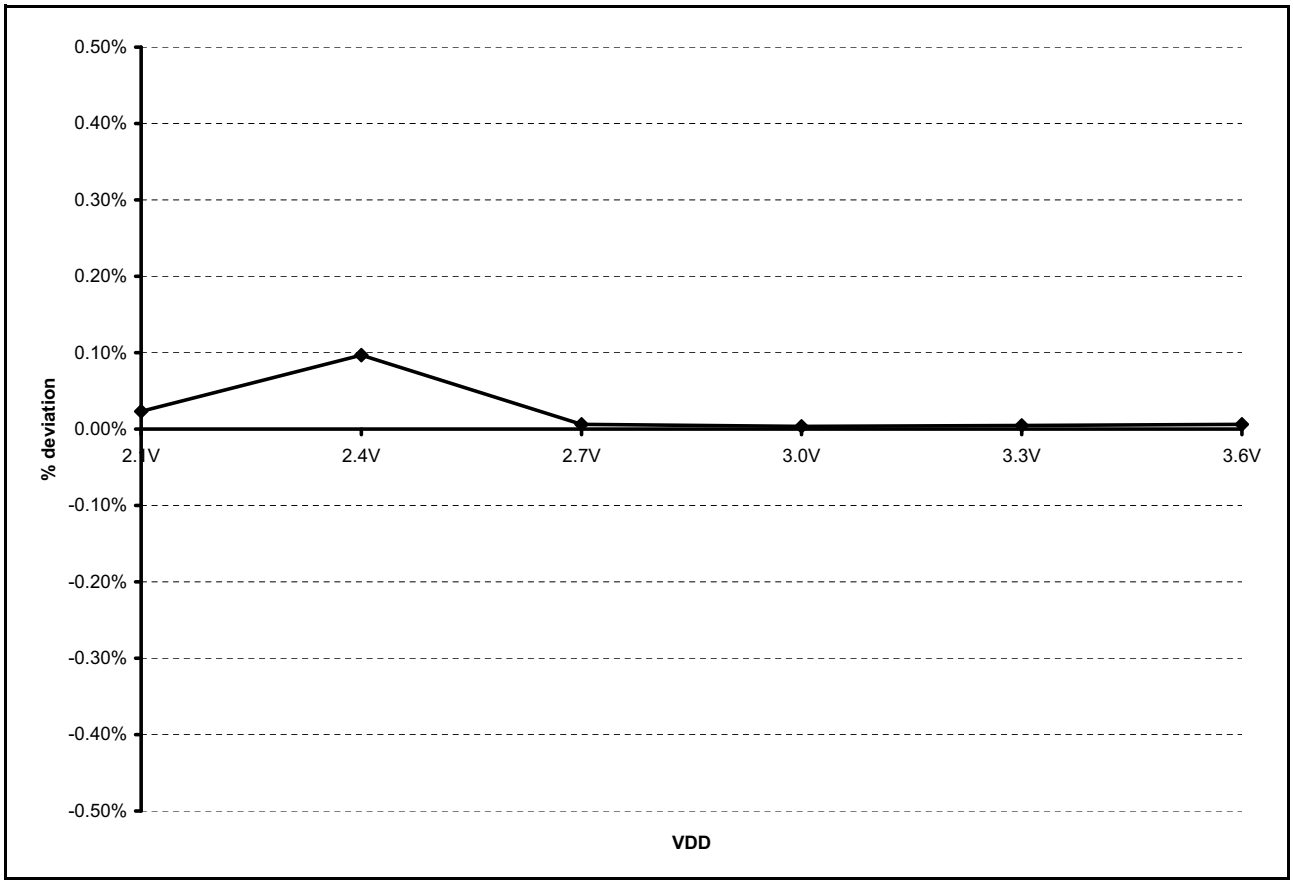


Figure 16. Deviation of DCO Output Across V_{DD} at 25°C

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 13. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus}) $V_{DD} \geq 1.8V$ $V_{DD} > 2.1V$ $V_{DD} > 2.4V$	f_{Bus}	dc	— — —	10 20 25.165	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	34 x t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	µs

3.10.3 SPI Timing

Table 15 and Figure 21 through Figure 24 describe the timing requirements for the SPI system.

Table 15. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	 $f_{Bus}/2048$ 0	 $f_{Bus}/2$ $f_{Bus}/4$	 Hz Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	 15 15	 — —	 ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	 0 25	 — —	 ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	 — —	 25 25	 ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns
11	D	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns
12	D	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns

4 Ordering Information

This section contains ordering information for MC9S08QE128, MC9S08QE96, and MC9S08QE64 devices.

Table 20. Ordering Information

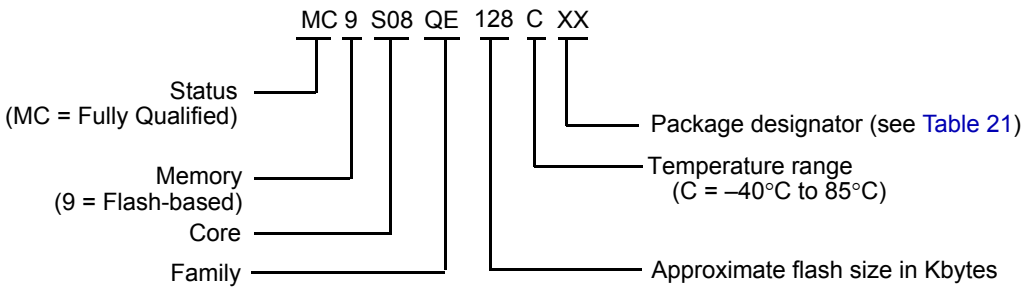
Freescale Part Number[1]	Memory		Temperature range (°C)	Package[2]
	Flash	RAM		
MC9S08QE128CLK	128K	8K	-40 to +85	80 LQFP
MC9S08QE128CLH			-40 to +85	64 LQFP
MC9S08QE128CFT			-40 to +85	48 QFN
MC9S08QE128CLD			-40 to +85	44 LQFP
MC9S08QE96CLK	96K	6K	-40 to +85	80 LQFP
MC9S08QE96CLH			-40 to +85	64 LQFP
MC9S08QE96CFT			-40 to +85	48 QFN
MC9S08QE96CLD			-40 to +85	44 QFP
MC9S08QE64CLH	64K	4K	-40 to +85	64 LQFP
MC9S08QE64CFT			-40 to +85	48 QFN
MC9S08QE64CLD			-40 to +85	44 QFP
MC9S08QE64CLC			-40 to +85	32 LQFP

1 See the reference manual, *MC9S08QE128RM*, for a complete description of modules included on each device.

2 See Table 21 for package information.

4.1 Device Numbering System

Example of the device numbering system:

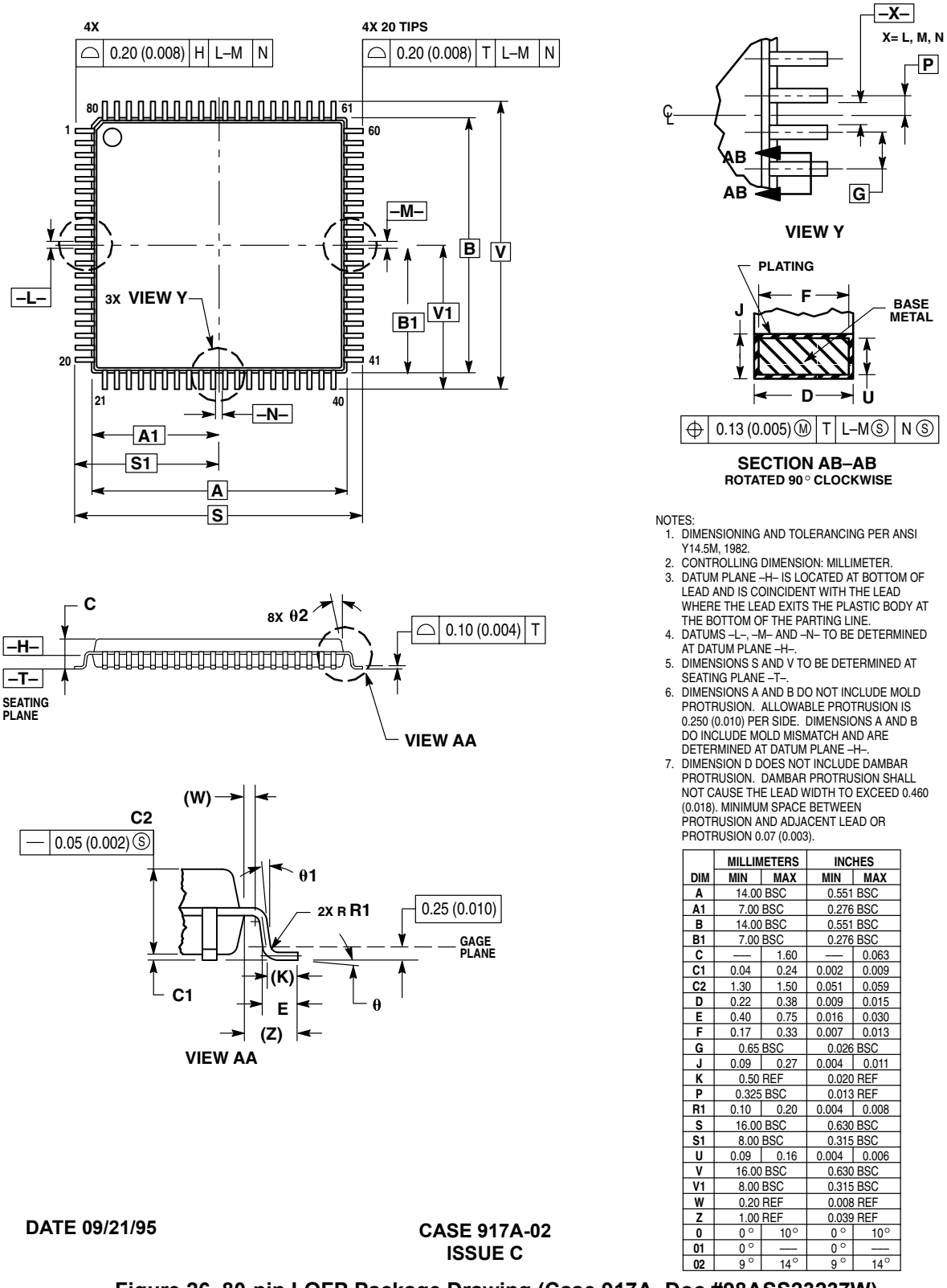


5 Package Information

The below table details the various packages available.

Table 21. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
80	Low Quad Flat Package	LQFP	LK	917A	98ASS23237W
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W
48	Quad Flat No-Leads	QFN	FT	1314	98ARH99048A
44	Low Quad Flat Package	LQFP	LD	824D	98ASS23225W
32	Low Quad Flat Package	LQFP	LC	873A	98ASH70029A



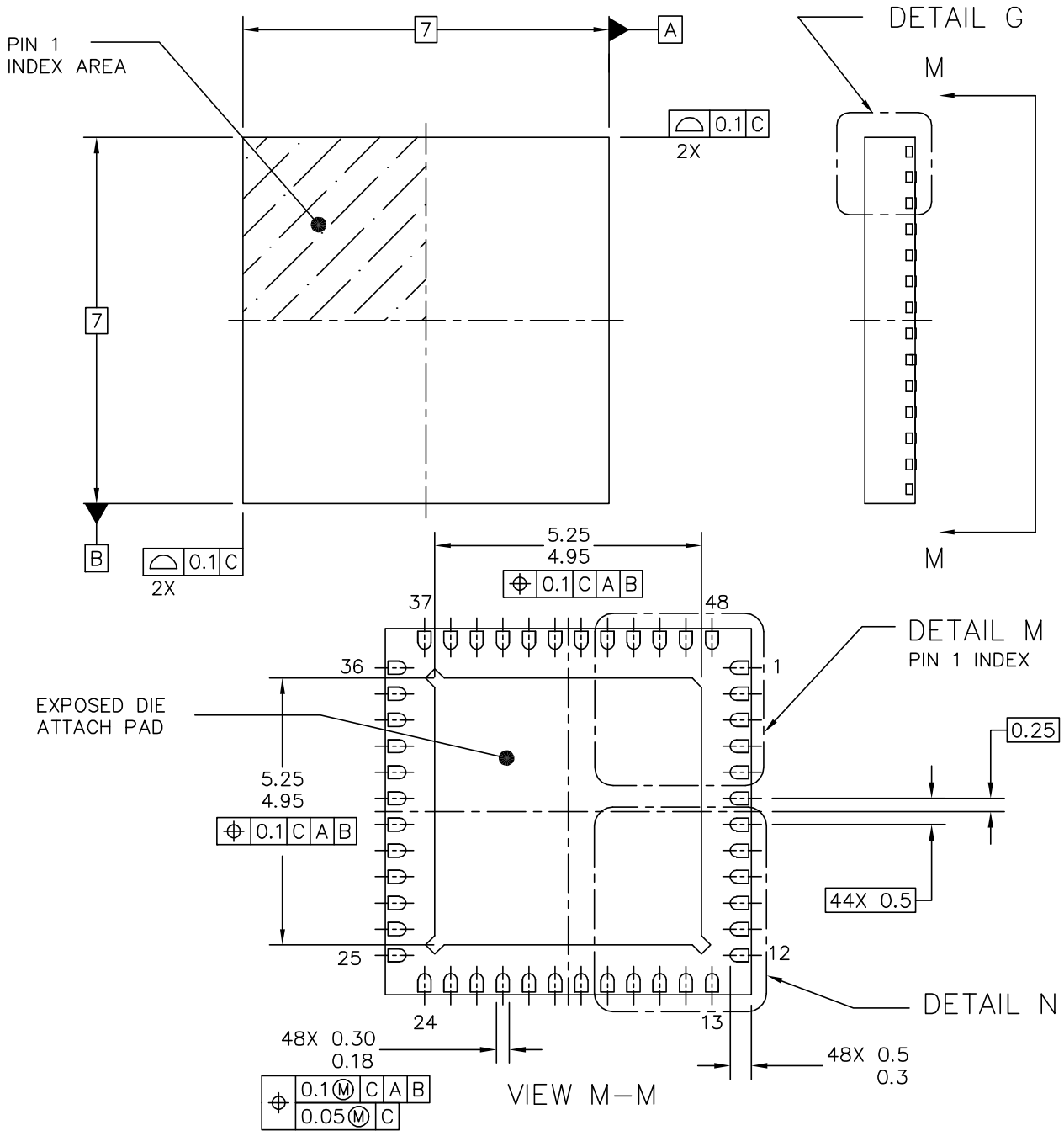
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.460 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
A1	7.00 BSC		0.276 BSC	
B	14.00 BSC		0.551 BSC	
B1	7.00 BSC		0.276 BSC	
C	—	1.60	—	0.063
C1	0.04	0.24	0.002	0.009
C2	1.30	1.50	0.051	0.059
D	0.22	0.38	0.009	0.015
E	0.40	0.75	0.016	0.030
F	0.17	0.33	0.007	0.013
G	0.65 BSC		0.026 BSC	
J	0.09	0.27	0.004	0.011
K	0.50 REF		0.020 REF	
P	0.325 BSC		0.013 REF	
R1	0.10	0.20	0.004	0.008
S	16.00 BSC		0.630 BSC	
S1	8.00 BSC		0.315 BSC	
U	0.09	0.16	0.004	0.006
V	16.00 BSC		0.630 BSC	
V1	8.00 BSC		0.315 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	10°	0°	10°
θ1	0°	—	0°	—
θ2	9°	14°	9°	14°

DATE 09/21/95

CASE 917A-02
ISSUE C

Figure 26. 80-pin LQFP Package Drawing (Case 917A, Doc #98ASS23237W)



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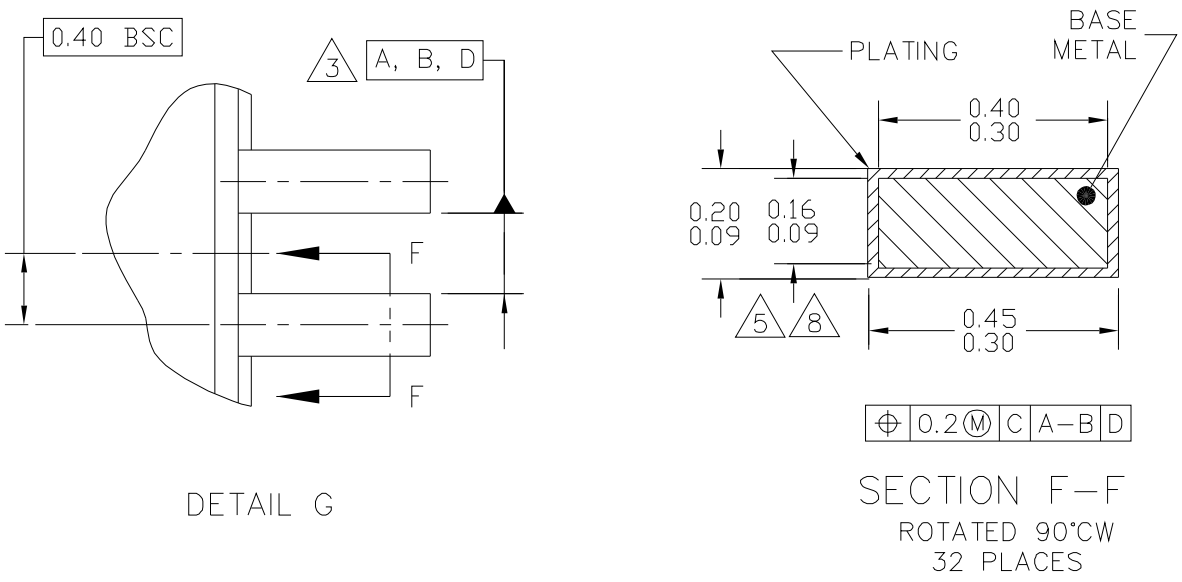
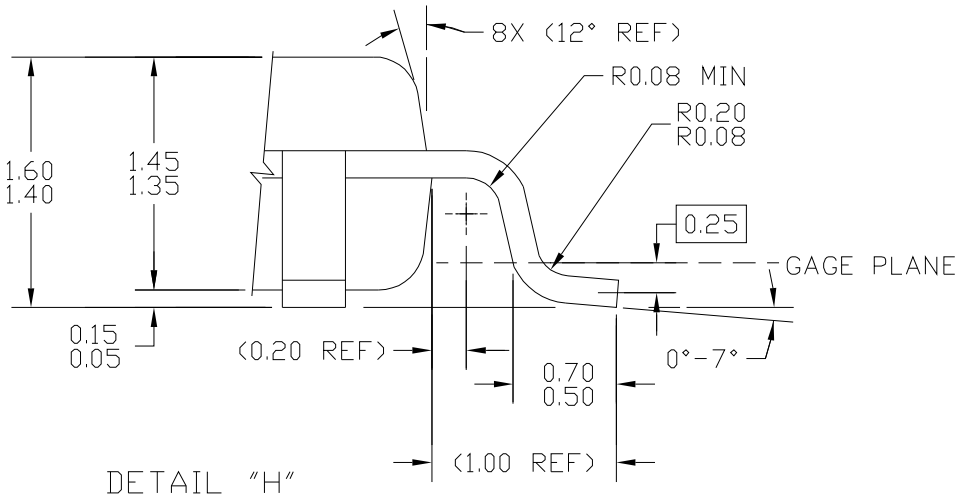
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARH99048A	REV: F
	CASE NUMBER: 1314–05	05 DEC 2005
	STANDARD: JEDEC–MO–220 VKKD–2	

Figure 30. 48-pin QFN Package Drawing (Case 1314, Doc #98ARH99048A), Sheet 1 of 3





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TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A	REV: D
	CASE NUMBER: 873A-03	19 MAY 2005
	STANDARD: JEDEC MS-026 BBA	

Figure 37. 32-pin LQFP Package Drawing (Case 873A, Doc #98ASH70029A), Sheet 2 of 3

6 Product Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9S08QE128RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

7 Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web are the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com

The following revision history table summarizes changes contained in this document.

Table 22. Revision History

Revision	Date	Description of Changes
4	9 Nov 2007	Replaced 44 QFP package with 44 LQFP package.
		Changed ACMP electricals, V_{AIO} specification's test category from P to C.
5	28 May 2008	Updated the tables **Thermal Characteristics**, **DC Characteristics**, **Supply Current Characteristics**, **XOSC and ICS Specifications (Temperature Range = –40 to 85°C Ambient)**, **ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)**, **Control Timing**, and **Analog Comparator Electrical Specifications**, **12-bit ADC Characteristics (VREFH = VDDAD, VREFL = VSSAD)** Updated the figures **Typical Run IDD for FBE and FEI, IDD vs. VDD (ACMP and ADC off, All Other Modules Enabled)**, **Deviation of DCO Output from Trimmed Frequency (50.33 MHz, 3.0 V)**, and **Deviation of DCO Output from Trimmed Frequency (50.33 MHz, 25°C)**
6	24 Jun 2008	Updated the table **Thermal Characteristics** Updated the row corresponding to Num 18 in the table **DC Characteristics** Updated the tables MC9S08**QE128 Series Features by MCU and Package**, **DC Characteristics**, **Supply Current Characteristics**, **Thermal Characteristics**, **Control Timing**, and **Ordering Information** Updated the figures **Typical Run IDD for FBE and FEI, IDD vs. VDD (ADC off, All Other Modules Enabled)**, **Deviation of DCO Output Across Temperature at VDD = 3.0 V**, and **Deviation of DCO Output Across VDD at 25×C**
7	2 Oct 2008	Updated the Stop2 and Stop3 mode supply current in the Supply Current Characteristics table. Replaced the stop mode adders section from the Supply Current Characteristics with its own Stop Mode Adders table with new specifications.