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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	50MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	34
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08qe96cld

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

Freescale Semiconductor
Data Sheet: Technical Data

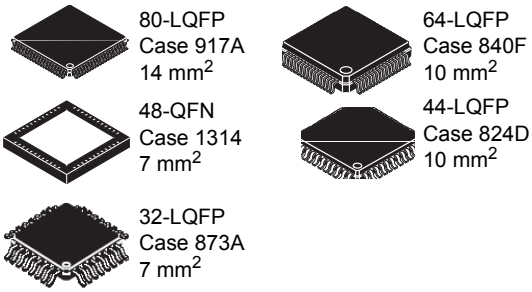
An Energy Efficient Solution by Freescale

Document Number: MC9S08QE128
Rev. 7, 10/2008

MC9S08QE128 Series

Covers: MC9S08QE128, MC9S08QE96, MC9S08QE64

MC9S08QE128



- 8-Bit HCS08 Central Processor Unit (CPU)
  - Up to 50.33-MHz HCS08 CPU above 2.4V, 40-MHz CPU above 2.1V, and 20-MHz CPU above 1.8V, across temperature range
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Flash read/program/erase over full operating voltage and temperature
  - Random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two low power stop modes; reduced power wait mode
  - Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode
  - Very low power external oscillator can be used in stop3 mode to provide accurate clock to active peripherals
  - Very low power real time counter for use in run, wait, and stop modes with internal and external clock sources
  - 6 µs typical wake up time from stop modes
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — FLL controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation; supports CPU freq. from 2 to 50.33 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints)
  - On-chip in-circuit emulator (ICE) debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints.
- ADC — 24-channel, 12-bit resolution; 2.5 µs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6V to 1.8V
- ACMPx — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; outputs can be optionally routed to TPM module; operation in stop3
- SCIx — Two SCIs with full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake up on active edge
- SPIx— Two serial peripheral interfaces with Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; MSB-first or LSB-first shifting
- IICx — Two IICs with; Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10 bit addressing
- TPMx — One 6-channel and two 3-channel; Selectable input capture, output compare, or buffered edge- or center-aligned PWMs on each channel
- RTC — 8-bit modulus counter with binary or decimal based prescaler; External clock source for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components
- Input/Output
  - 70 GPIOs and 1 input-only and 1 output-only pin
  - 16 KBI interrupts with selectable polarity
  - Hysteresis and configurable pull-up device on all input pins; Configurable slew rate and drive strength on all output pins.
  - SET/CLR registers on 16 pins (PTC and PTE)

Table of Contents

1 MC9S08QE128 Series Comparison

The following table compares the various device derivatives available within the MC9S08QE128 series.

Table 1. MC9S08QE128 Series Features by MCU and Package

Feature	MC9S08QE128				MC9S08QE96				MC9S08QE64			
Flash size (bytes)	131072				98304				65536			
RAM size (bytes)	8064				6016				4096			
Pin quantity	80	64	48	44	80	64	48	44	64	48	44	32
ACMP1	yes											
ACMP2	yes											
ADC channels	24	22	10	10	24	22	10	10	22	10	10	10
DBG	yes											
ICS	yes											
IIC1	yes											
IIC2	yes	yes	no	no	yes	yes	no	no	yes	no	no	no
IRQ	yes											
KBI	16	16	16	16	16	16	16	16	16	16	16	12
Port I/O[1]	70	54	38	34	70	54	38	34	54	38	34	26
RTC	yes											
SCI1	yes											
SCI2	yes											
SPI1	yes											
SPI2	yes											
TPM1 channels	3											
TPM2 channels	3											
TPM3 channels	6											
XOSC	yes											

[1] Port I/O count does not include the input only PTA5/IRQ/TPM1CLK/$\overline{\text{RESET}}$ or the output only PTA4/ACMP1O/BKGD/MS.

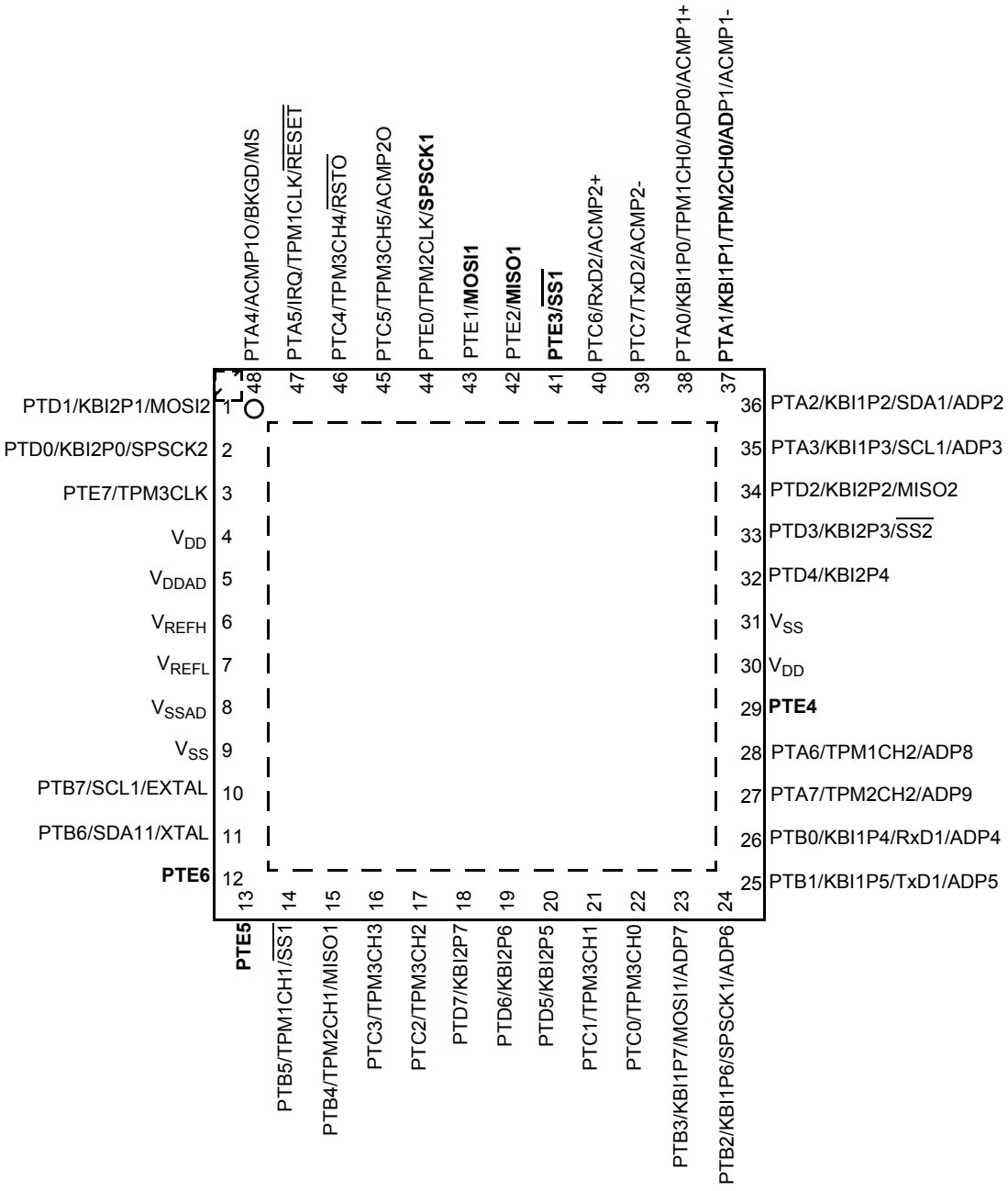


Figure 4. Pin Assignments in 48-Pin QFN Package

[3] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	–40 to 85	°C
Maximum junction temperature	T_{JM}	95	°C
Thermal resistance Single-layer board			
32-pin LQFP	θ_{JA}	82	°C/W
44-pin LQFP		68	
48-pin QFN		81	
64-pin LQFP	θ_{JA}	69	°C/W
80-pin LQFP		60	
Thermal resistance Four-layer board			
32-pin LQFP	θ_{JA}	54	°C/W
44-pin LQFP		46	
48-pin QFN		26	
64-pin LQFP	θ_{JA}	50	°C/W
80-pin LQFP		47	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
18	P	Low-voltage detection threshold — low range[7]	V_{LVDL}	V_{DD} falling V_{DD} rising	1.80 1.86	1.82 1.90	1.91 1.99	V
19	P	Low-voltage warning threshold — high range[7]	V_{LVWH}	V_{DD} falling V_{DD} rising	2.36 2.36	2.46 2.46	2.56 2.56	V
20	P	Low-voltage warning threshold — low range[7]	V_{LVWL}	V_{DD} falling V_{DD} rising	2.11 2.16	2.16 2.21	2.22 2.27	V
21	C	Low-voltage inhibit reset/recover hysteresis[7]	V_{hys}		—	50	—	mV
22	P	Bandgap Voltage Reference[9]	V_{BG}		1.15	1.17	1.18	V

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 Maximum is highest voltage that POR is guaranteed.

7 Low voltage detection and warning limits measured at 1 MHz bus frequency.

8 Run at 1 MHz bus frequency

9 Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

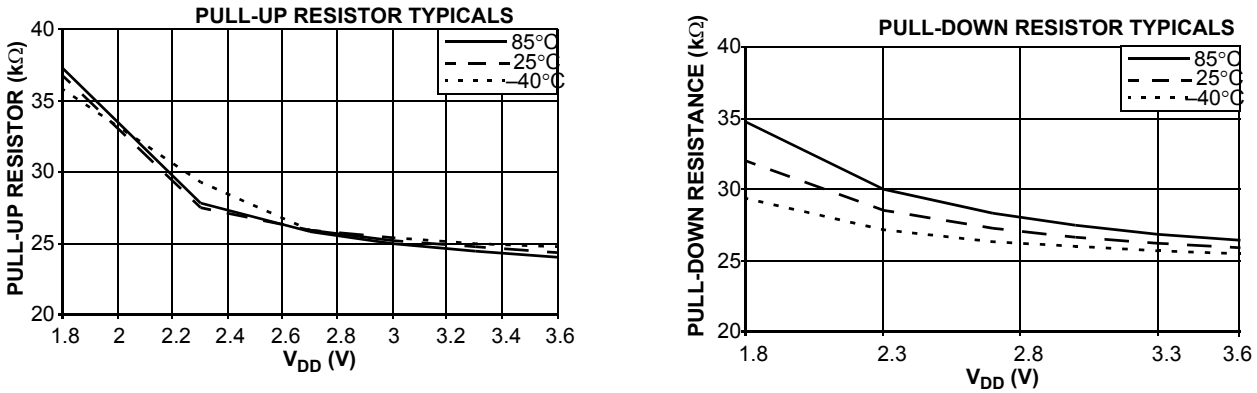


Figure 7. Pull-up and Pull-down Typical Resistor Values

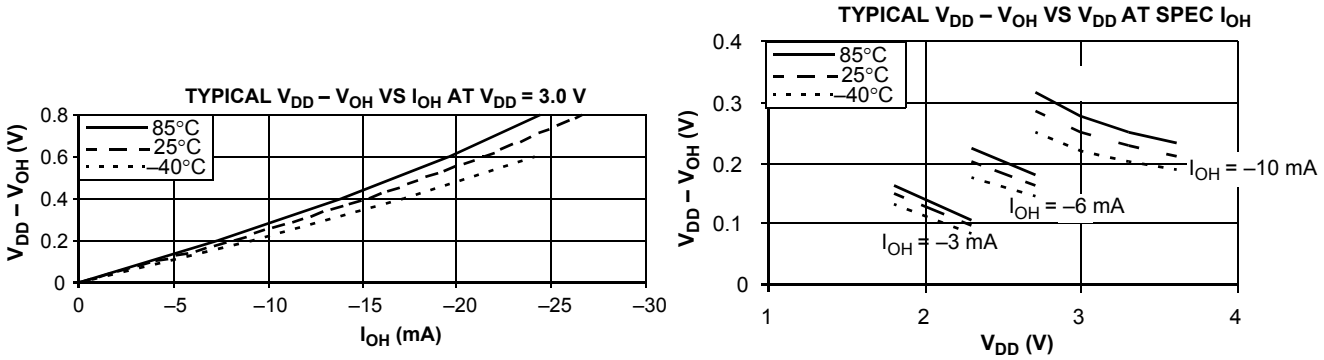


Figure 11. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	25.165 MHz	3	16	18	mA	–40 to 25
	P					16	20		85
	T			20 MHz		14.4	—		–40 to 85
	T			8 MHz		6.5	—		
	T			1 MHz		1.4	—		
2	C	Run supply current FEI mode, all modules off	RI_{DD}	25.165 MHz	3	11.5	12.3	mA	–40 to 85
	T			20 MHz		9.5	—		
	T			8 MHz		4.6	—		
	T			1 MHz		1.0	—		
3	T	Run supply current LPS=0, all modules off	RI_{DD}	16 kHz FBILP	3	152	—	µA	–40 to 85
	T			16 kHz FBELP		115	—		
4	T	Run supply current LPS=1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3	21.9	—	µA	0 to 70
							—		–40 to 85
	T	Run supply current LPS=1, all modules off, running from RAM				7.3	—		0 to 70
							—		–40 to 85
5	C	Wait mode supply current FEI mode, all modules off	WI_{DD}	25.165 MHz	3	5.74	6	mA	–-40 to 85
	T			20 MHz		4.57	—		
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		

Table 13. Control Timing (continued)

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	— —	— —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	— —	— —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	8 31	— —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	7 24	— —	ns
10		Voltage regulator recovery time	t_{VRR}	—	4	—	µs

1 Typical values are based on characterization data at V_{DD} = 3.0V, 25°C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset or interrupt pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

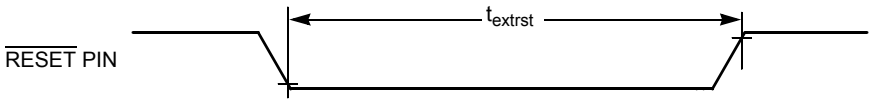


Figure 17. Reset Timing

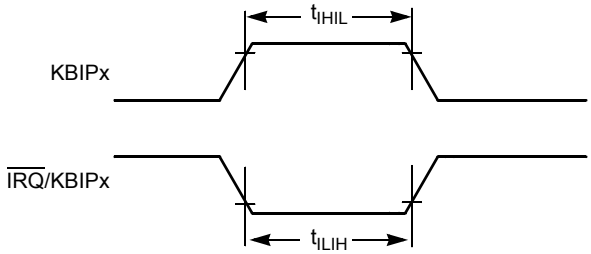


Figure 18. IRQ/KBIPx Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

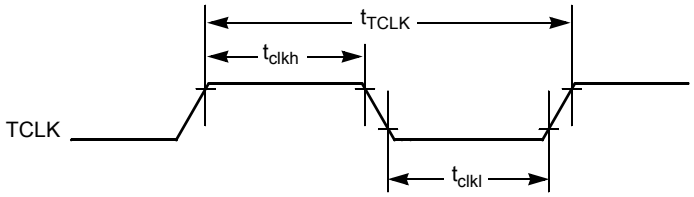


Figure 19. Timer External Clock

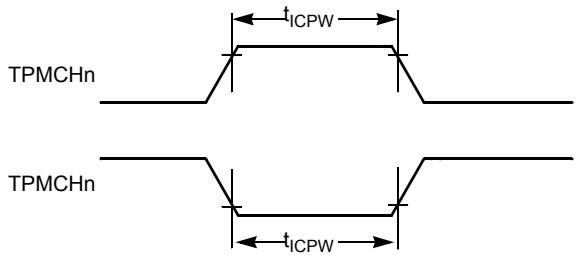
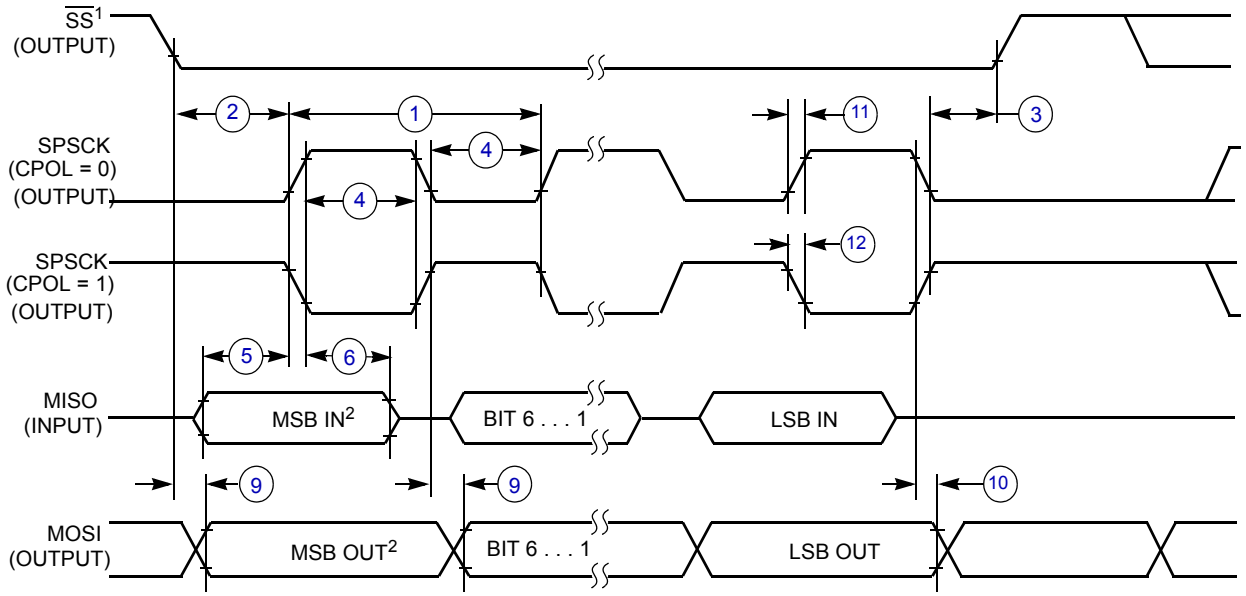
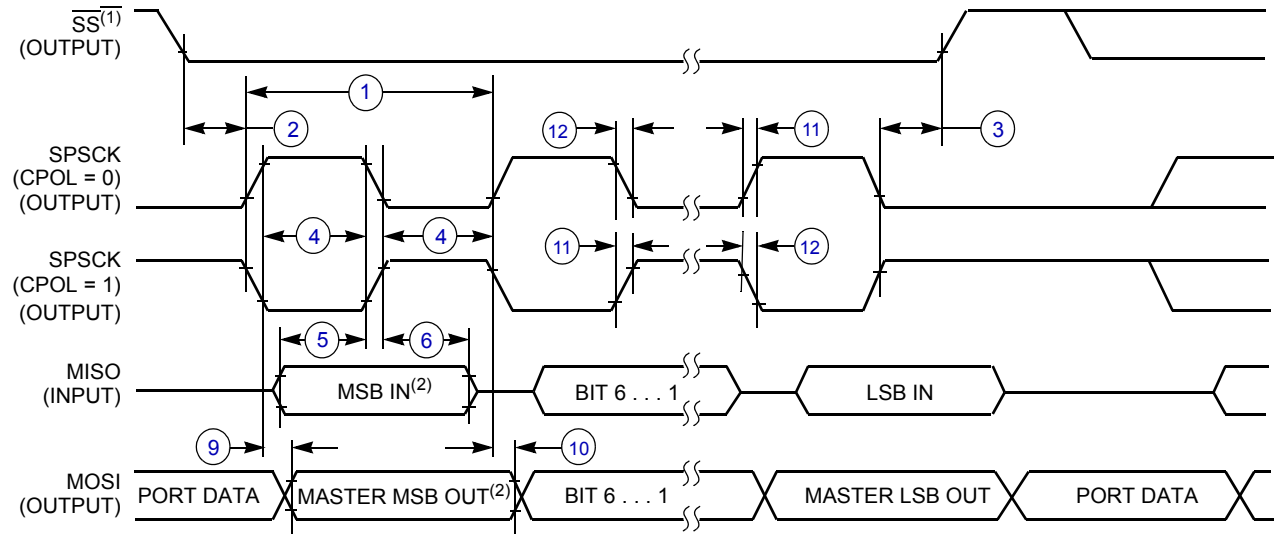


Figure 20. Timer Input Capture Pulse



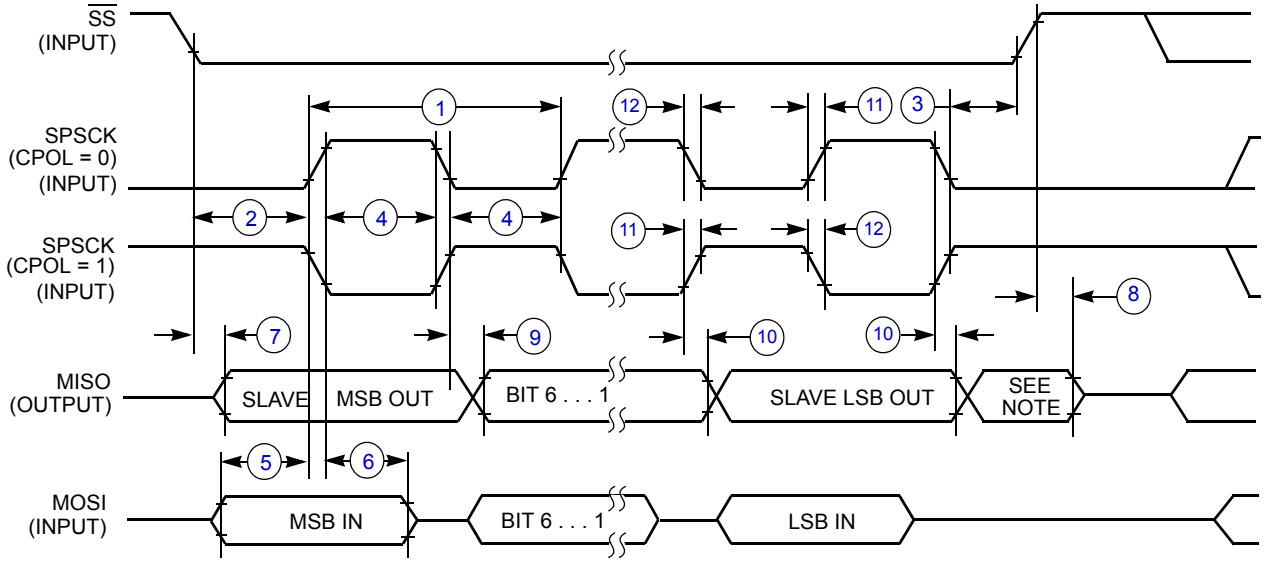
NOTES:
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 21. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

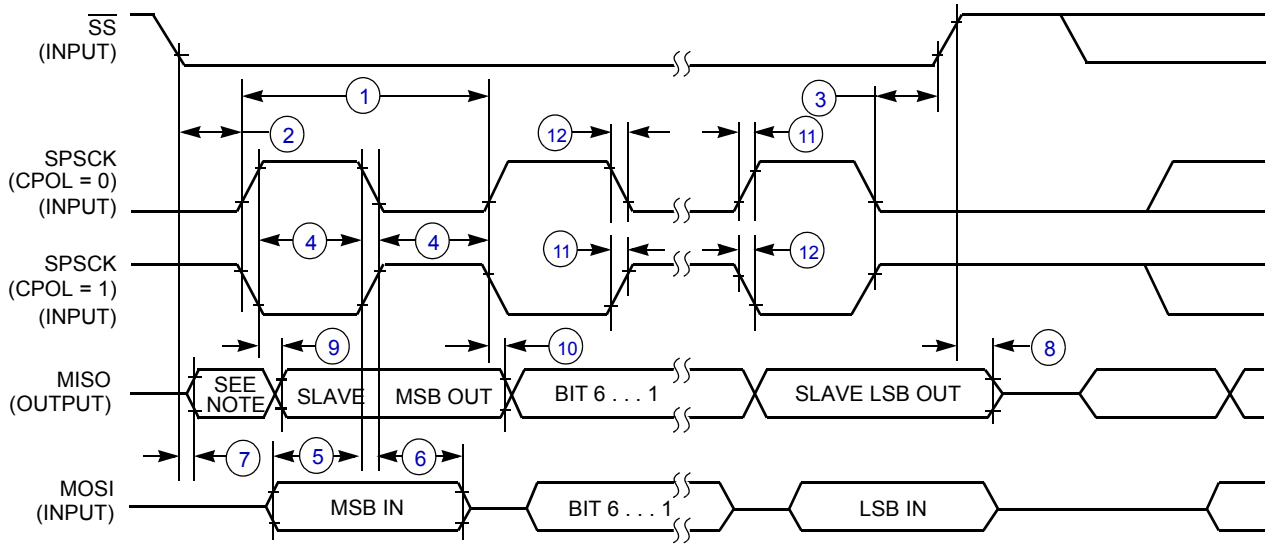
Figure 22. SPI Master Timing (CPHA =1)



NOTE:

1. Not defined but normally MSB of character just received

Figure 23. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 24. SPI Slave Timing (CPHA = 1)

3.11 Analog Comparator (ACMP) Electricals

Table 16. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DD}	1.80	—	3.6	V
C	Supply current (active)	I_{DDAC}	—	20	35	µA
D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
C	Analog input offset voltage	V_{AIO}		20	40	mV
C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
P	Analog input leakage current	I_{ALKG}	—	—	1.0	µA
C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	µs

3.12 ADC Characteristics

Table 17. 12-bit ADC Operating Conditions

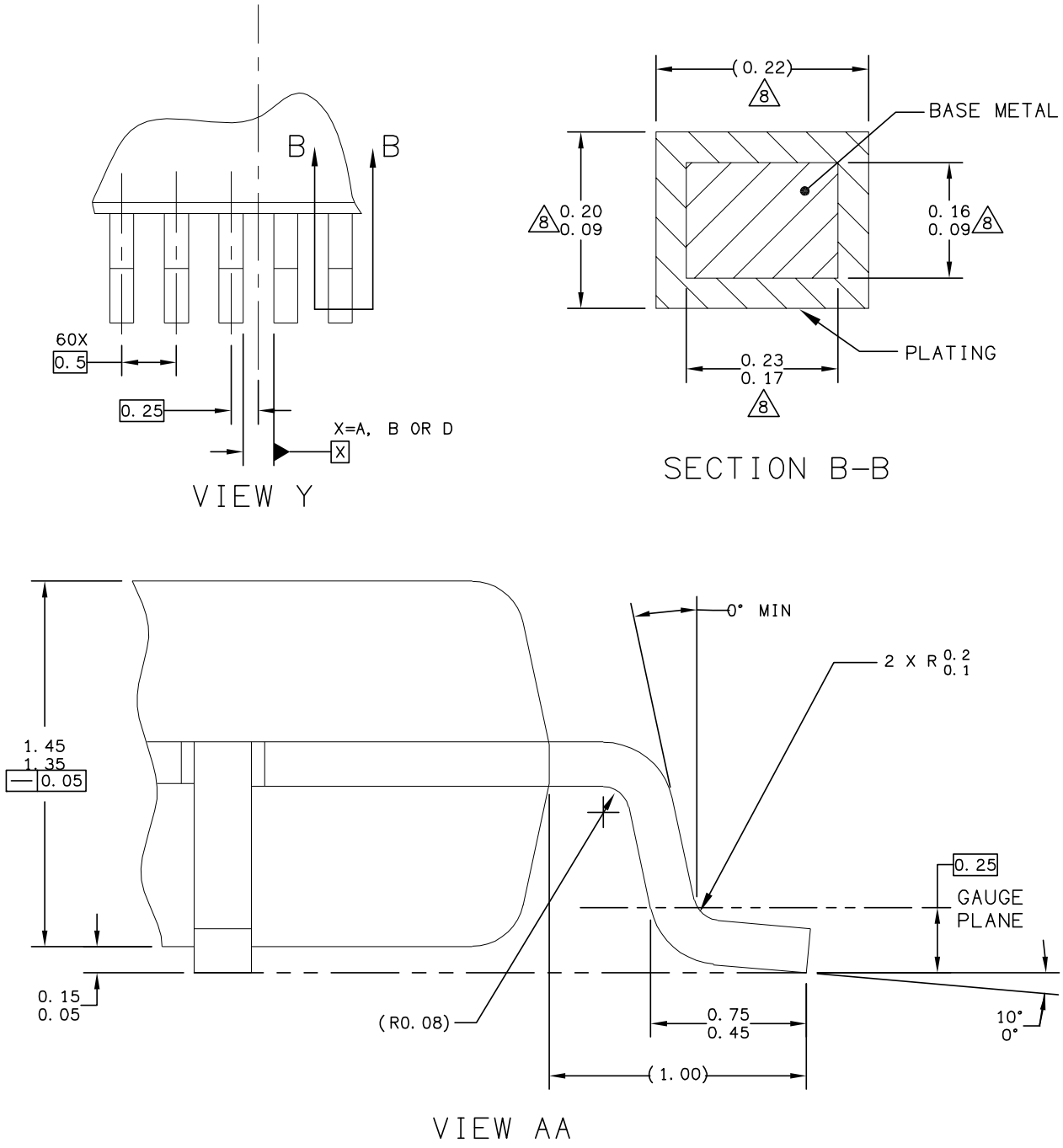
C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
D	Supply voltage	Absolute	V_{DDAD}	1.8	—	3.6	V	
		Delta to V_{DD} (V_{DD}-V_{DDAD})[2]	ΔV_{DDAD}	-100	0	+100	mV	
D	Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSAD})[2]	ΔV_{SSAD}	-100	0	+100	mV	
D	Ref Voltage High		V_{REFH}	1.8	V_{DDAD}	V_{DDAD}	V	
D	Ref Voltage Low		V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	
D	Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
C	Input Capacitance		C_{ADIN}	—	4.5	5.5	pF	
C	Input Resistance		R_{ADIN}	—	5	7	kΩ	
C	Analog Source Resistance	12 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
		10 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz		 — —	 — —	 5 10		
		8 bit mode (all valid f_{ADCK})		—	—	10		
D	ADC Conversion Clock Freq.	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
		Low Power (ADLPC=1)		0.4	—	4.0		

1 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

5.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 21. For the latest available drawings please visit our web site (http://www.freescale.com) and enter the package's document number into the keyword search box.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D
	CASE NUMBER: 840F-02	06 APR 2005
	STANDARD: JEDEC MS-026 BCD	

Figure 28. 64-pin LQFP Package Drawing (Case 840F, Doc #98ASS23234W), Sheet 2 of 3

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

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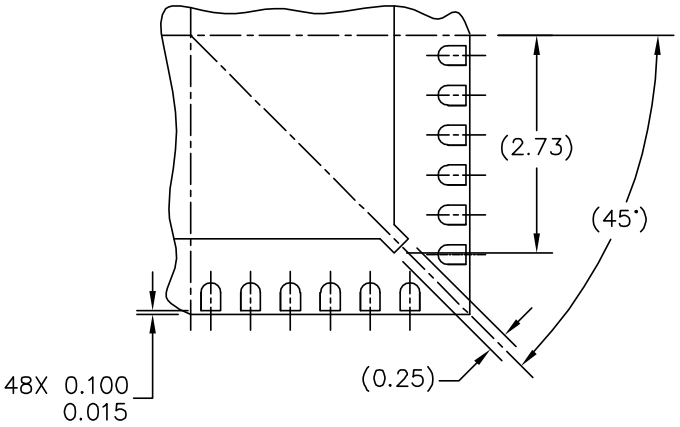
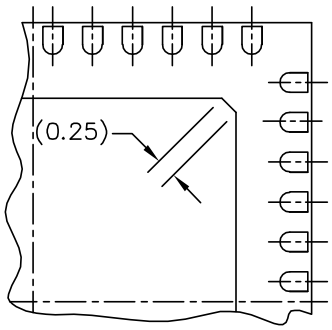
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D	
	CASE NUMBER: 840F-02	06 APR 2005	
	STANDARD: JEDEC MS-026 BCD		

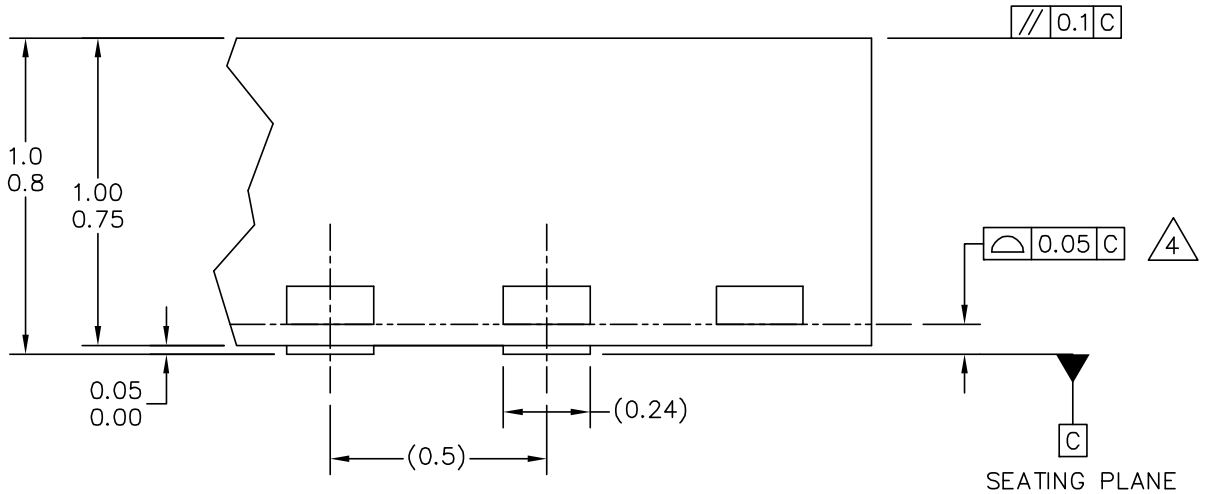
Figure 29. 64-pin LQFP Package Drawing (Case 840F, Doc #98ASS23234W), Sheet 3 of 3



DETAIL N
PREFERRED CORNER CONFIGURATION



DETAIL M
PREFERED PIN 1 BACKSIDE IDENTIFIER



DETAIL G
VIEW ROTATED 90° CW

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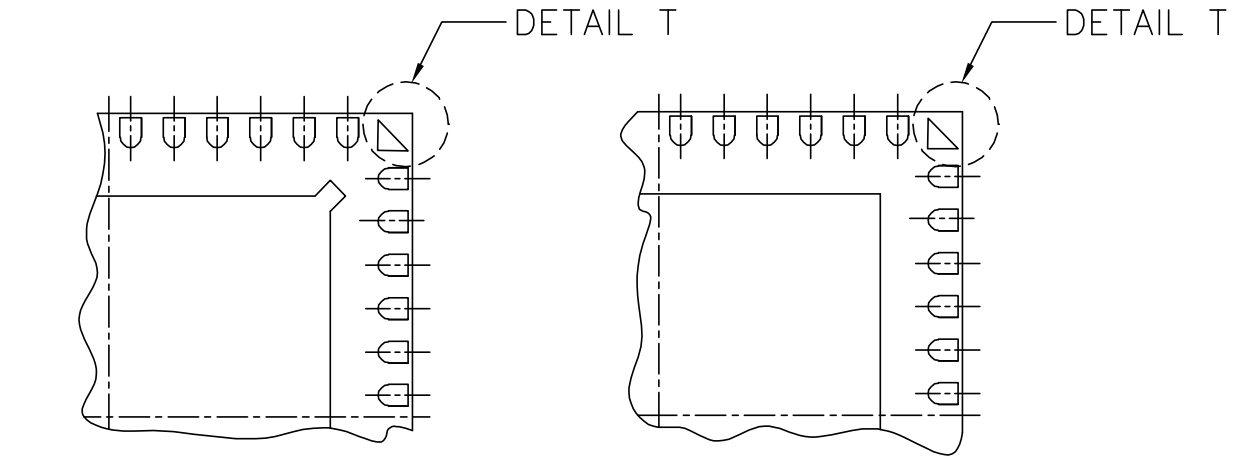
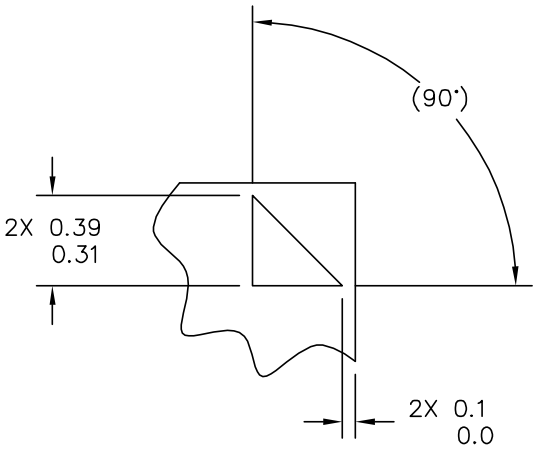
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARH99048A	REV: F
	CASE NUMBER: 1314–05	05 DEC 2005
	STANDARD: JEDEC–MO–220 VKKD–2	

Figure 31. 48-pin QFN Package Drawing (Case 1314, Doc #98ARH99048A), Sheet 2 of 3





NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.

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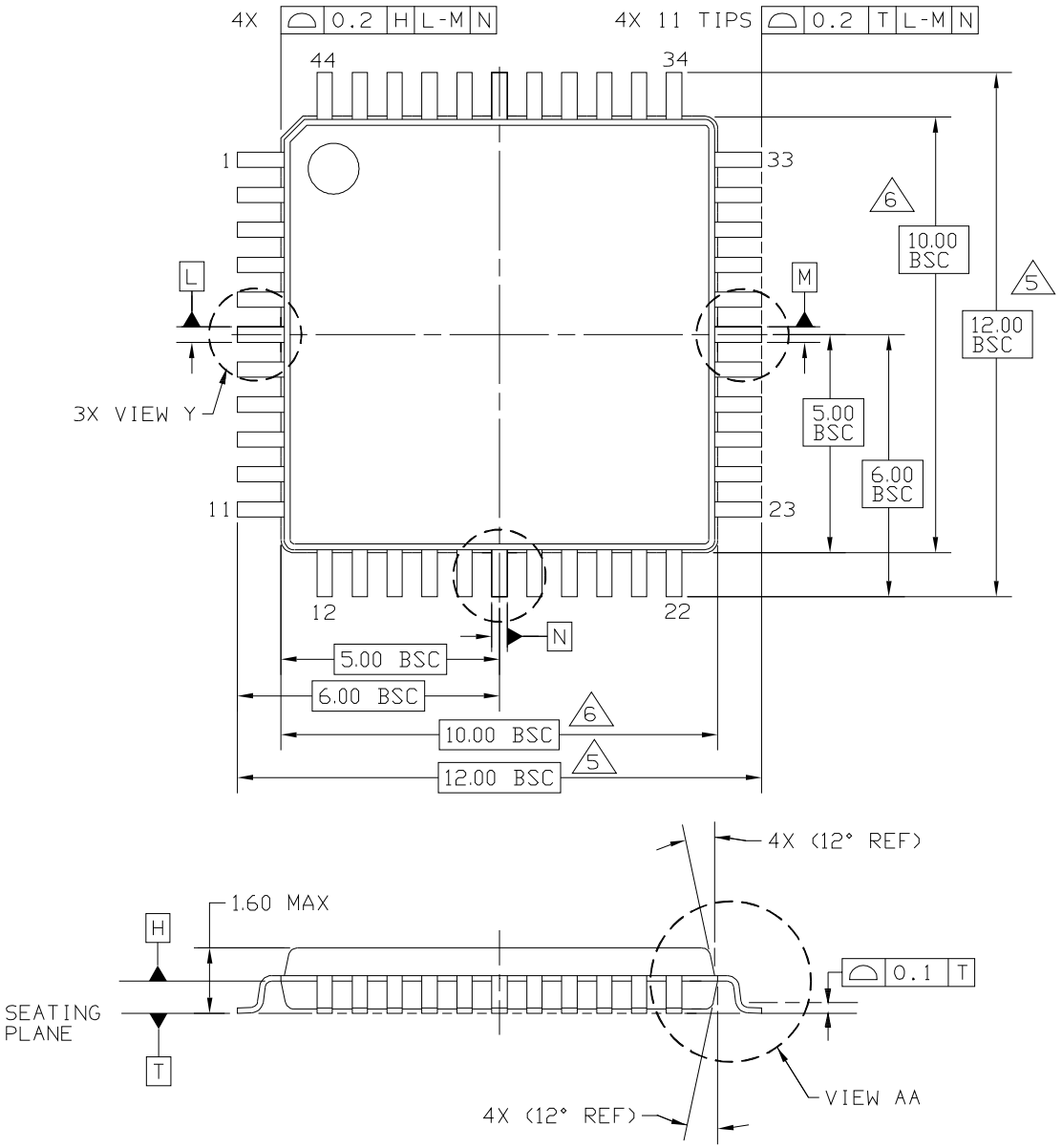
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARH99048A	REV: F
	CASE NUMBER: 1314–05	05 DEC 2005
	STANDARD: JEDEC–MO–220 VKKD–2	

Figure 32. 48-pin QFN Package Drawing (Case 1314, Doc #98ARH99048A), Sheet 3 of 3



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TITLE: 44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23225W	REV: D
	CASE NUMBER: 824D-02	26 FEB 2007
	STANDARD: JEDEC MS-026-BCB	

Figure 33. 44-pin LQFP Package Drawing (Case 824D, Doc #98ASS23225W), Sheet 1 of 3

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.

3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

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TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A	REV: D
	CASE NUMBER: 873A-03	19 MAY 2005
	STANDARD: JEDEC MS-026 BBA	

Figure 38. 32-pin LQFP Package Drawing (Case 873A, Doc #98ASH70029A), Sheet 3 of 3