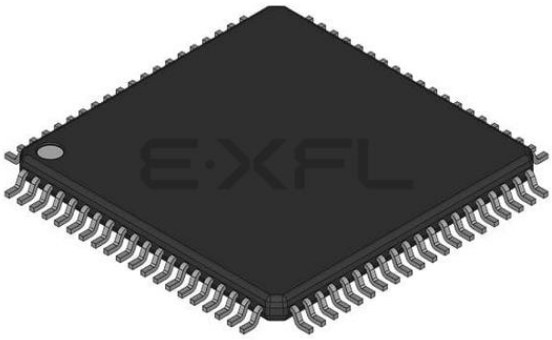

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	50MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	70
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08qe96clk

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

1 MC9S08QE128 Series Comparison

The following table compares the various device derivatives available within the MC9S08QE128 series.

Table 1. MC9S08QE128 Series Features by MCU and Package

Feature	MC9S08QE128				MC9S08QE96				MC9S08QE64			
Flash size (bytes)	131072				98304				65536			
RAM size (bytes)	8064				6016				4096			
Pin quantity	80	64	48	44	80	64	48	44	64	48	44	32
ACMP1	yes											
ACMP2	yes											
ADC channels	24	22	10	10	24	22	10	10	22	10	10	10
DBG	yes											
ICS	yes											
IIC1	yes											
IIC2	yes	yes	no	no	yes	yes	no	no	yes	no	no	no
IRQ	yes											
KBI	16	16	16	16	16	16	16	16	16	16	16	12
Port I/O[1]	70	54	38	34	70	54	38	34	54	38	34	26
RTC	yes											
SCI1	yes											
SCI2	yes											
SPI1	yes											
SPI2	yes											
TPM1 channels	3											
TPM2 channels	3											
TPM3 channels	6											
XOSC	yes											

[1] Port I/O count does not include the input only PTA5/IRQ/TPM1CLK/$\overline{\text{RESET}}$ or the output only PTA4/ACMP1O/BKGD/MS.

Table 2. MC9S08QE128 Series Pin Assignment by Package and Pin Count (continued)

Pin Number					Lowest ← Priority → Highest				
80	**64**	**48**	**44**	**32**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
41	33	25	23	17	PTB1	KBI1P5	TxD1		ADP5
42	34	26	24	18	PTB0	KBI1P4	RxD1		ADP4
43	—	—	—	—	PTJ3				
44	—	—	—	—	PTJ2				
45	35	—	—	—	PTF3				ADP13
46	36	—	—	—	PTF2				ADP12
47	37	27	25	19	PTA7	TPM2CH2			ADP9
48	38	28	26	20	PTA6	TPM1CH2			ADP8
49	39	29	—	—	PTE4				
50	40	30	27	—					V_{DD}
51	41	31	28	—					V_{SS}
52	42	—	—	—	PTF1				ADP11
53	43	—	—	—	PTF0				ADP10
54	—	—	—	—	PTJ1				
55	—	—	—	—	PTJ0				
56	44	32	29	—	PTD4	KBI2P4			
57	45	33	30	21	PTD3	KBI2P3	$\overline{SS2}$		
58	46	34	31	22	PTD2	KBI2P2	MISO2		
59	47	35	32	23	PTA3	KBI1P3	SCL1		ADP3
60	48	36	33	24	PTA2	KBI1P2	SDA1		ADP2
61	49	37	34	25	PTA1	KBI1P1	TPM2CH0	ADP1	ACMP1-
62	50	38	35	26	PTA0	KBI1P0	TPM1CH0	ADP0	ACMP1+
63	51	39	36	27	PTC7	TxD2			ACMP2-
64	52	40	37	28	PTC6	RxD2			ACMP2+
65	—	—	—	—	PTG7				ADP23
66	—	—	—	—	PTG6				ADP22
67	—	—	—	—	PTG5				ADP21
68	—	—	—	—	PTG4				ADP20
69	53	41	—	—	PTE3	$\overline{SS1}$			
70	54	42	38	—	PTE2	MISO1			
71	55	—	—	—	PTG3				ADP19
72	56	—	—	—	PTG2				ADP18
73	57	—	—	—	PTG1				
74	58	—	—	—	PTG0				
75	59	43	39	—	PTE1	MOSI1			
76	60	44	40	—	PTE0	TPM2CLK	SPSCK1		
77	61	45	41	29	PTC5	TPM3CH5			ACMP2O
78	62	46	42	30	PTC4	TPM3CH4	$\overline{RSTO}$		
79	63	47	43	31	PTA5	IRQ	TPM1CLK	$\overline{RESET}$	
80	64	48	44	32	PTA4	ACMP1O	BKGD	MS	

[3] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	–40 to 85	°C
Maximum junction temperature	T_{JM}	95	°C
Thermal resistance Single-layer board			
32-pin LQFP	θ_{JA}	82	°C/W
44-pin LQFP		68	
48-pin QFN		81	
64-pin LQFP	θ_{JA}	69	°C/W
80-pin LQFP		60	
Thermal resistance Four-layer board			
32-pin LQFP	θ_{JA}	54	°C/W
44-pin LQFP		46	
48-pin QFN		26	
64-pin LQFP	θ_{JA}	50	°C/W
80-pin LQFP		47	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

3.8 External Oscillator (XOSC) Characteristics

Reference Figure 13 and Figure 14 for crystal or resonator circuits.

Table 11. XOSC and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1,C_2	See Note[2] See Note[3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, High Gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 0 100 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high power High range, low power High range, high power	 t_{CSTL} t_{CSTH} 	 — — — —	 200 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode FBELP mode	f_{extal}	0.03125 0	— —	40.0 50.33	MHz MHz

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

3 See crystal or resonator manufacturer's recommendation.

4 Proper PC board layout procedures must be followed to achieve specifications.

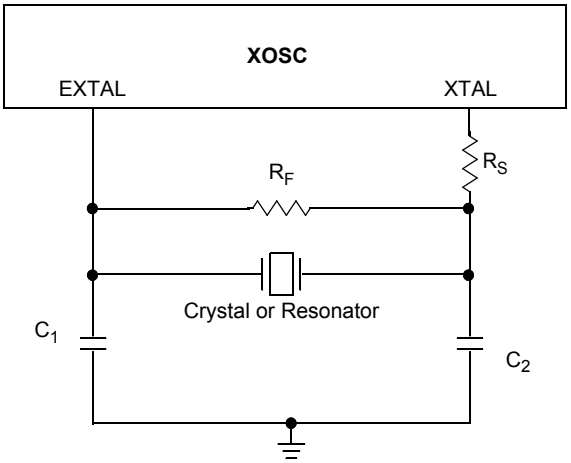


Figure 13. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

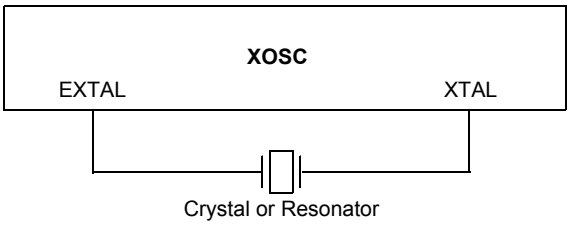


Figure 14. Typical Crystal or Resonator Circuit: Low Range/Low Gain

3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at V_{DD} = 3.6 V and temperature = 25°C		f_{int_ft}	—	32.768	—	kHz
2	P	Internal reference frequency — user trimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time		t_{IRST}	—	60	100	µs
4	P	DCO output frequency range — trimmed [2]	Low range (DRS=00)	f_{dco_u}	16	—	20	MHz
	P		Mid range (DRS=01)		32	—	40	
	P		High range (DRS=10)		48	—	60	
5	P	DCO output frequency [2] Reference = 32768 Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS=01)		—	39.85	—	
	P		High range (DRS=10)		—	59.77	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$

Table 13. Control Timing (continued)

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	— —	— —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	— —	— —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	8 31	— —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	7 24	— —	ns
10		Voltage regulator recovery time	t_{VRR}	—	4	—	µs

1 Typical values are based on characterization data at V_{DD} = 3.0V, 25°C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset or interrupt pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

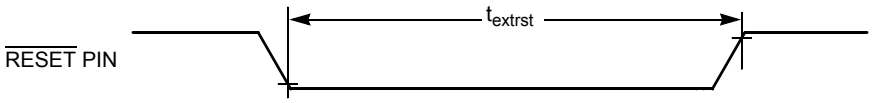


Figure 17. Reset Timing

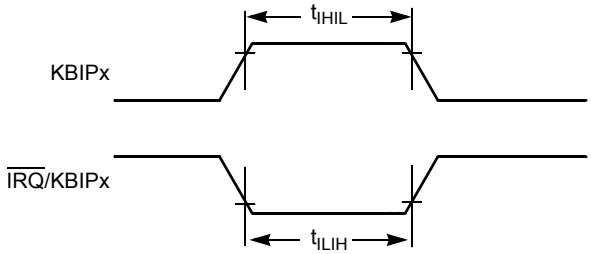


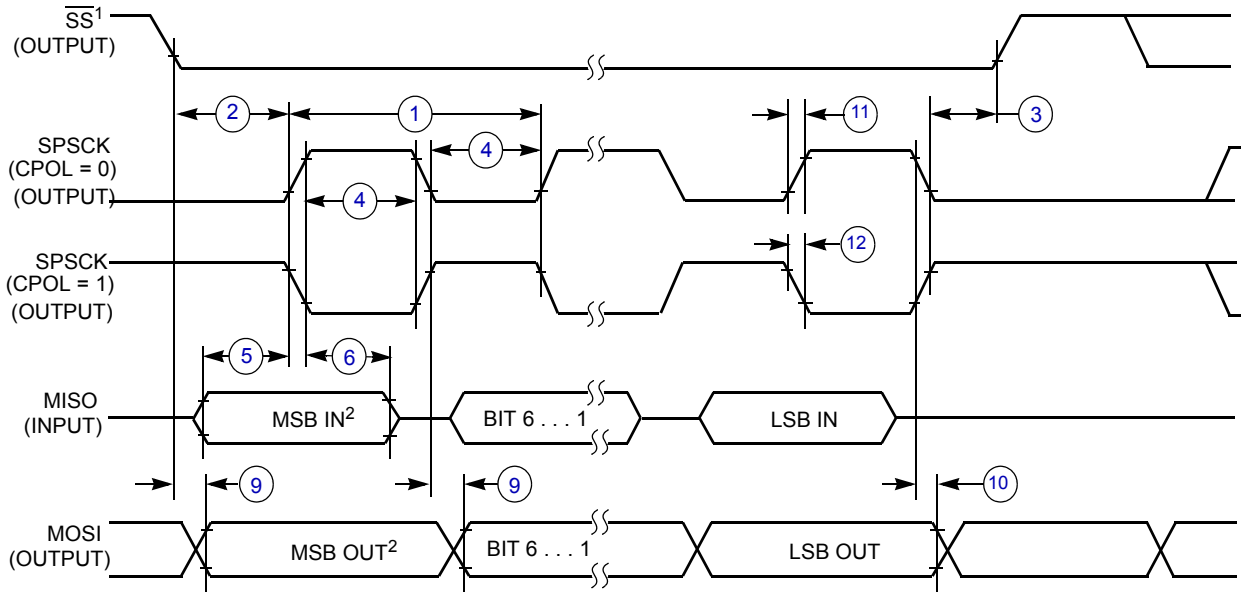
Figure 18. IRQ/KBIPx Timing

3.10.3 SPI Timing

Table 15 and Figure 21 through Figure 24 describe the timing requirements for the SPI system.

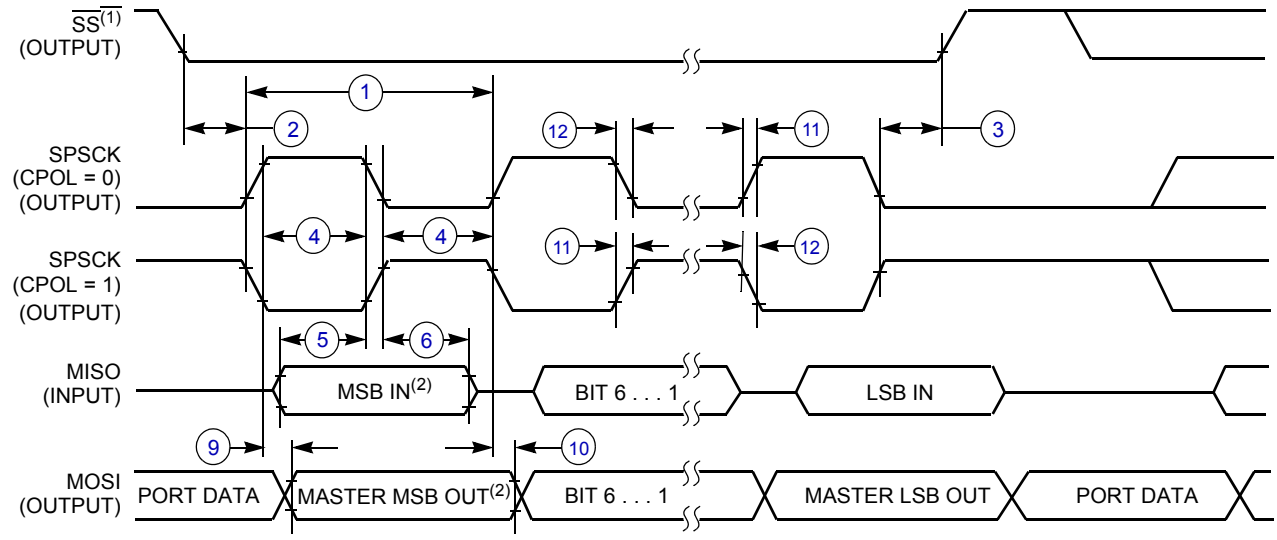
Table 15. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	 $f_{Bus}/2048$ 0	 $f_{Bus}/2$ $f_{Bus}/4$	 Hz Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	 15 15	 — —	 ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	 0 25	 — —	 ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	 — —	 25 25	 ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns
11	D	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns
12	D	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns



NOTES:
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 21. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 22. SPI Master Timing (CPHA =1)

3.11 Analog Comparator (ACMP) Electricals

Table 16. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DD}	1.80	—	3.6	V
C	Supply current (active)	I_{DDAC}	—	20	35	µA
D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
C	Analog input offset voltage	V_{AIO}		20	40	mV
C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
P	Analog input leakage current	I_{ALKG}	—	—	1.0	µA
C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	µs

3.12 ADC Characteristics

Table 17. 12-bit ADC Operating Conditions

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
D	Supply voltage	Absolute	V_{DDAD}	1.8	—	3.6	V	
		Delta to V_{DD} (V_{DD}-V_{DDAD})[2]	ΔV_{DDAD}	-100	0	+100	mV	
D	Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSAD})[2]	ΔV_{SSAD}	-100	0	+100	mV	
D	Ref Voltage High		V_{REFH}	1.8	V_{DDAD}	V_{DDAD}	V	
D	Ref Voltage Low		V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	
D	Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
C	Input Capacitance		C_{ADIN}	—	4.5	5.5	pF	
C	Input Resistance		R_{ADIN}	—	5	7	kΩ	
C	Analog Source Resistance	12 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
		10 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz		 — —	 — —	 5 10		
		8 bit mode (all valid f_{ADCK})		—	—	10		
D	ADC Conversion Clock Freq.	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
		Low Power (ADLPC=1)		0.4	—	4.0		

1 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

Table 18. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	P	t_{ADC}	—	20	—	ADCK cycles	See the ADC chapter in the MC9S08*QE128 Reference Manual* for conversion time variances
	Long Sample (ADLSMP=1)	C		—	40	—		
Sample Time	Short Sample (ADLSMP=0)	P	t_{ADS}	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP=1)	C		—	23.5	—		
Total Unadjusted Error	12 bit mode	T	E_{TUE}	—	±3.0	—	LSB[2]	Includes Quantization
	10 bit mode	P		—	±1	±2.5		
	8 bit mode	T		—	±0.5	±1.0		
Differential Non-Linearity	12 bit mode	T	DNL	—	±1.75	—	LSB[2]	
	10 bit mode[3]	P		—	±0.5	±1.0		
	8 bit mode[3]	T		—	±0.3	±0.5		
Integral Non-Linearity	12 bit mode	T	INL	—	±1.5	—	LSB[2]	
	10 bit mode	T		—	±0.5	±1.0		
	8 bit mode	T		—	±0.3	±0.5		
Zero-Scale Error	12 bit mode	T	E_{ZS}	—	±1.5	—	LSB[2]	V_{ADIN} = V_{SSAD}
	10 bit mode	P		—	±0.5	±1.5		
	8 bit mode	T		—	±0.5	±0.5		
Full-Scale Error	12 bit mode	T	E_{FS}	—	±1.0	—	LSB[2]	V_{ADIN} = V_{DDAD}
	10 bit mode	P		—	±0.5	±1		
	8 bit mode	T		—	±0.5	±0.5		
Quantization Error	12 bit mode	D	E_Q	—	-1 to 0	—	LSB[2]	
	10 bit mode			—	—	±0.5		
	8 bit mode			—	—	±0.5		
Input Leakage Error	12 bit mode	D	E_{IL}	—	±2	—	LSB[2]	Pad leakage[4] * R_{AS}
	10 bit mode			—	±0.2	±4		
	8 bit mode			—	±0.1	±1.2		
Temp Sensor Slope	-40°C to 25°C	D	m	—	1.646	—	mV/°C	
	25°C to 85°C			—	1.769	—		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	701.2	—	mV	

1 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10 bit and 8 bit modes

4 Based on input pad leakage current. Refer to pad electricals.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section of the *MC9S08QE128 Reference Manual*.

Table 19. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase -40°C to 85°C	$V_{prog/erase}$	1.8		3.6	V
D	Supply voltage for read operation	V_{Read}	1.8		3.6	V
D	Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
P	Byte program time (random location)(2)	t_{prog}		9		t_{Fcyc}
P	Byte program time (burst mode)(2)	t_{Burst}		4		t_{Fcyc}
P	Page erase time[2]	t_{Page}		4000		t_{Fcyc}
P	Mass erase time(2)	t_{Mass}		20,000		t_{Fcyc}
	Byte program current[3]	R_{IDDBP}	—	4	—	mA
	Page erase current[3]	R_{IDDPE}	—	6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40°C to + 85°C T = 25°C		10,000 —	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

4 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

4 Ordering Information

This section contains ordering information for MC9S08QE128, MC9S08QE96, and MC9S08QE64 devices.

Table 20. Ordering Information

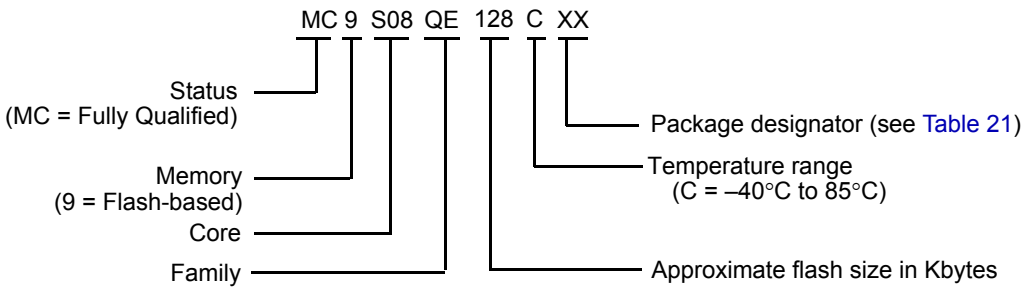
Freescale Part Number[1]	Memory		Temperature range (°C)	Package[2]
	Flash	RAM		
MC9S08QE128CLK	128K	8K	-40 to +85	80 LQFP
MC9S08QE128CLH			-40 to +85	64 LQFP
MC9S08QE128CFT			-40 to +85	48 QFN
MC9S08QE128CLD			-40 to +85	44 LQFP
MC9S08QE96CLK	96K	6K	-40 to +85	80 LQFP
MC9S08QE96CLH			-40 to +85	64 LQFP
MC9S08QE96CFT			-40 to +85	48 QFN
MC9S08QE96CLD			-40 to +85	44 QFP
MC9S08QE64CLH	64K	4K	-40 to +85	64 LQFP
MC9S08QE64CFT			-40 to +85	48 QFN
MC9S08QE64CLD			-40 to +85	44 QFP
MC9S08QE64CLC			-40 to +85	32 LQFP

1 See the reference manual, *MC9S08QE128RM*, for a complete description of modules included on each device.

2 See Table 21 for package information.

4.1 Device Numbering System

Example of the device numbering system:

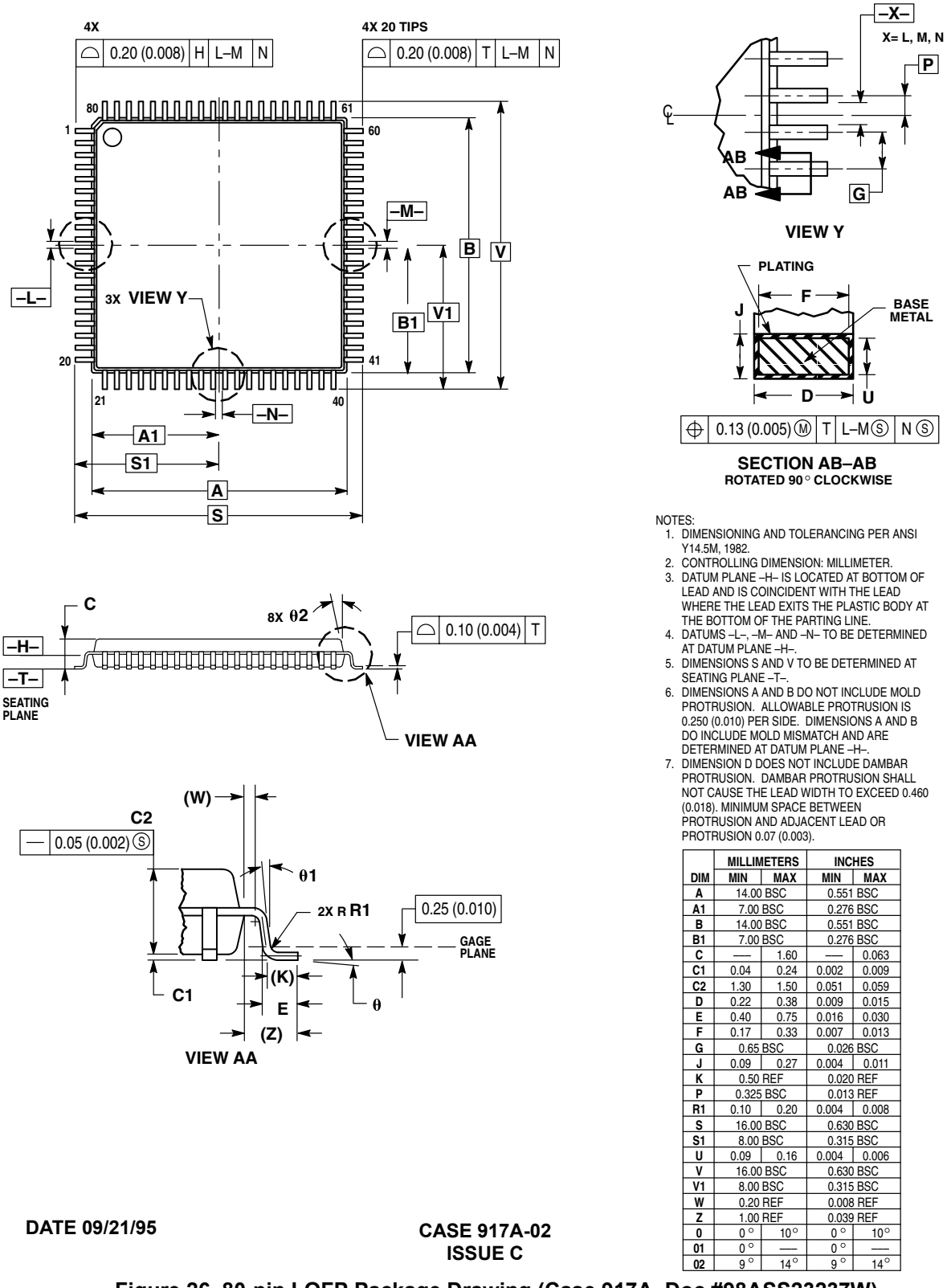


5 Package Information

The below table details the various packages available.

Table 21. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
80	Low Quad Flat Package	LQFP	LK	917A	98ASS23237W
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W
48	Quad Flat No-Leads	QFN	FT	1314	98ARH99048A
44	Low Quad Flat Package	LQFP	LD	824D	98ASS23225W
32	Low Quad Flat Package	LQFP	LC	873A	98ASH70029A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.460 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
A1	7.00 BSC		0.276 BSC	
B	14.00 BSC		0.551 BSC	
B1	7.00 BSC		0.276 BSC	
C	—	1.60	—	0.063
C1	0.04	0.24	0.002	0.009
C2	1.30	1.50	0.051	0.059
D	0.22	0.38	0.009	0.015
E	0.40	0.75	0.016	0.030
F	0.17	0.33	0.007	0.013
G	0.65 BSC		0.026 BSC	
J	0.09	0.27	0.004	0.011
K	0.50 REF		0.020 REF	
P	0.325 BSC		0.013 REF	
R1	0.10	0.20	0.004	0.008
S	16.00 BSC		0.630 BSC	
S1	8.00 BSC		0.315 BSC	
U	0.09	0.16	0.004	0.006
V	16.00 BSC		0.630 BSC	
V1	8.00 BSC		0.315 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	10°	0°	10°
θ1	0°	—	0°	—
θ2	9°	14°	9°	14°

DATE 09/21/95

CASE 917A-02
ISSUE C

Figure 26. 80-pin LQFP Package Drawing (Case 917A, Doc #98ASS23237W)

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

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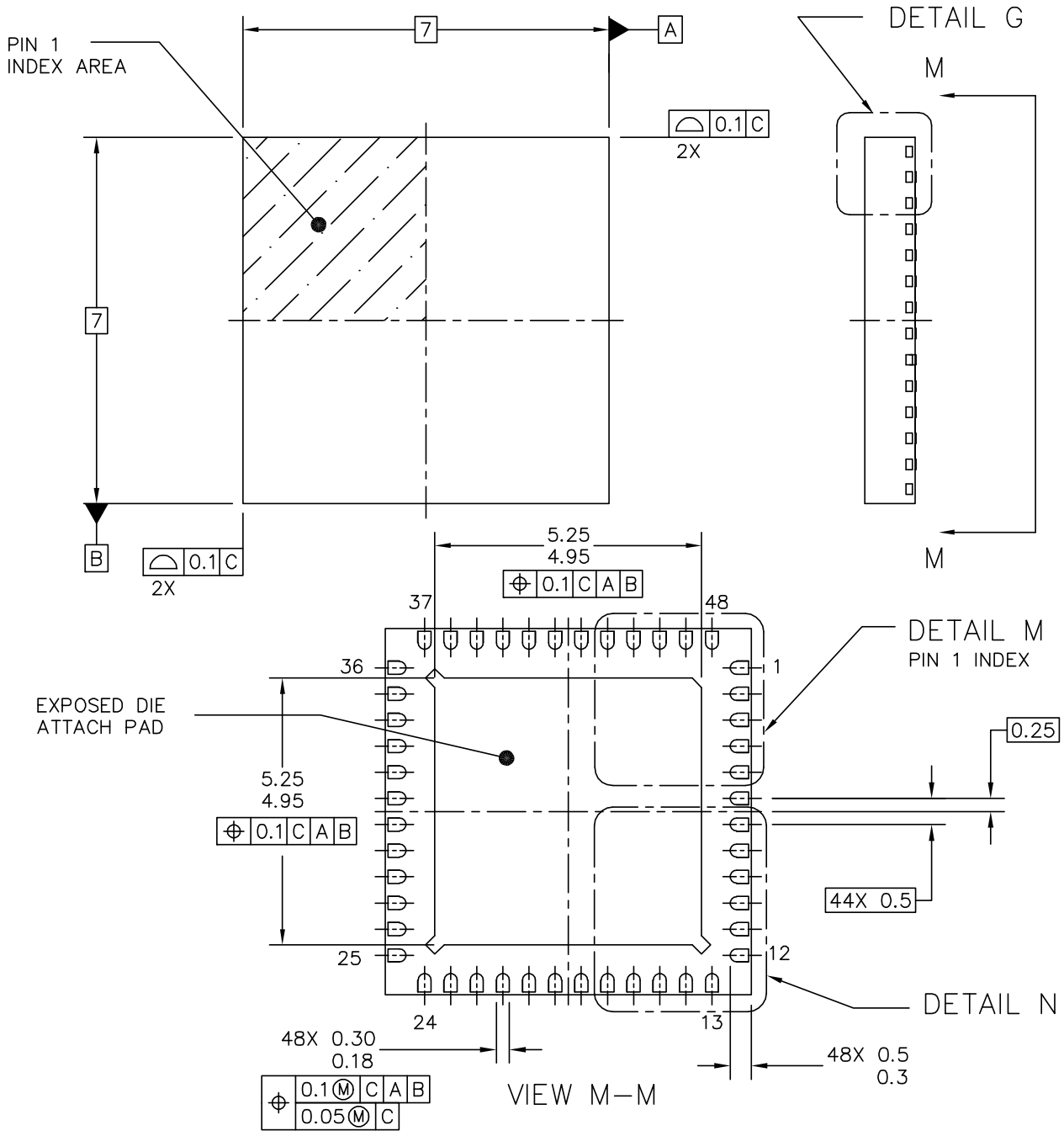
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D	
	CASE NUMBER: 840F-02	06 APR 2005	
	STANDARD: JEDEC MS-026 BCD		

Figure 29. 64-pin LQFP Package Drawing (Case 840F, Doc #98ASS23234W), Sheet 3 of 3



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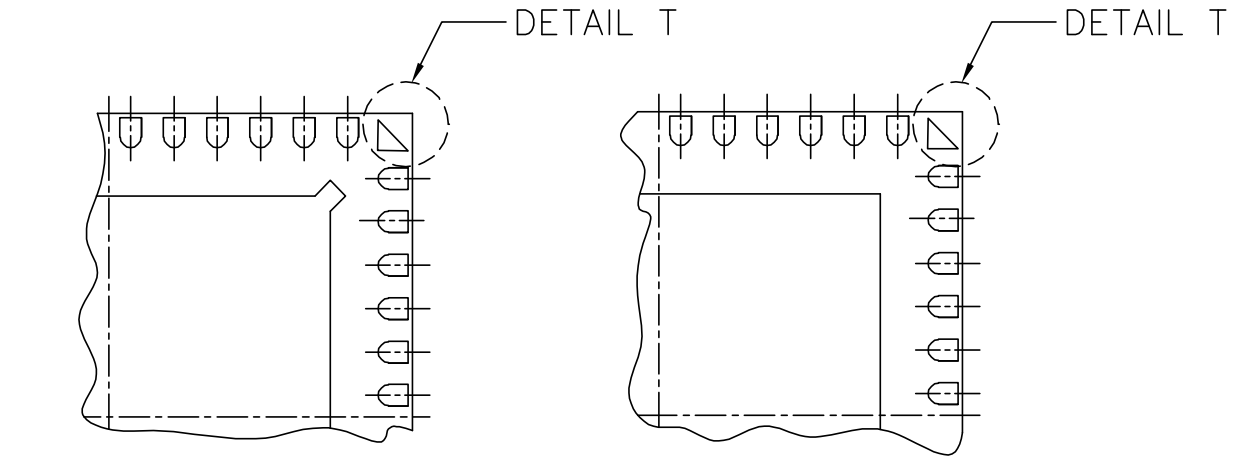
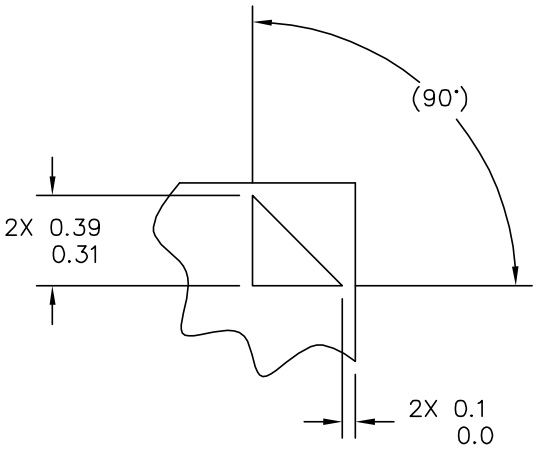
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARH99048A	REV: F
	CASE NUMBER: 1314–05	05 DEC 2005
	STANDARD: JEDEC–MO–220 VKKD–2	

Figure 30. 48-pin QFN Package Drawing (Case 1314, Doc #98ARH99048A), Sheet 1 of 3





NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.

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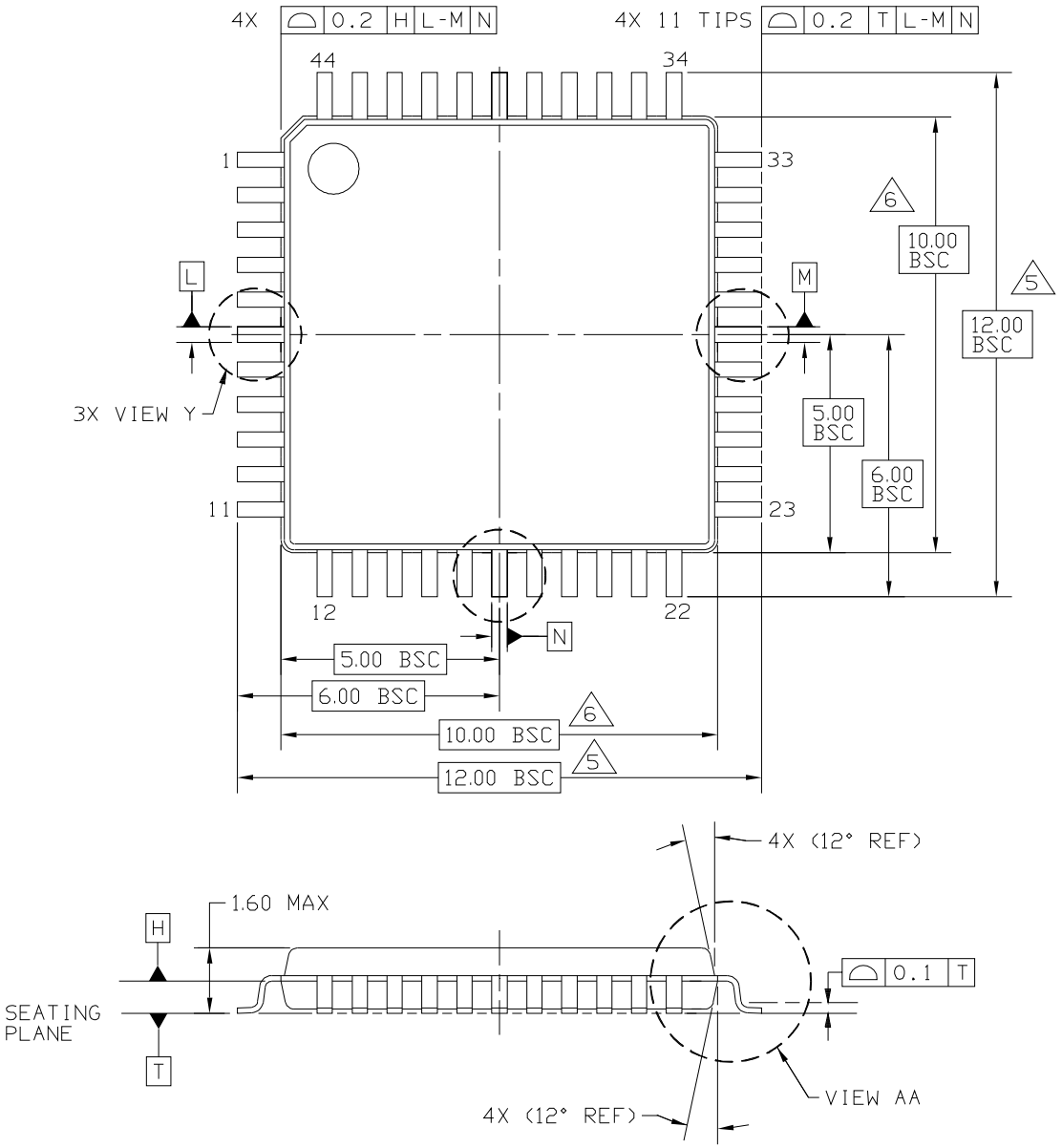
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARH99048A	REV: F
	CASE NUMBER: 1314–05	05 DEC 2005
	STANDARD: JEDEC–MO–220 VKKD–2	

Figure 32. 48-pin QFN Package Drawing (Case 1314, Doc #98ARH99048A), Sheet 3 of 3



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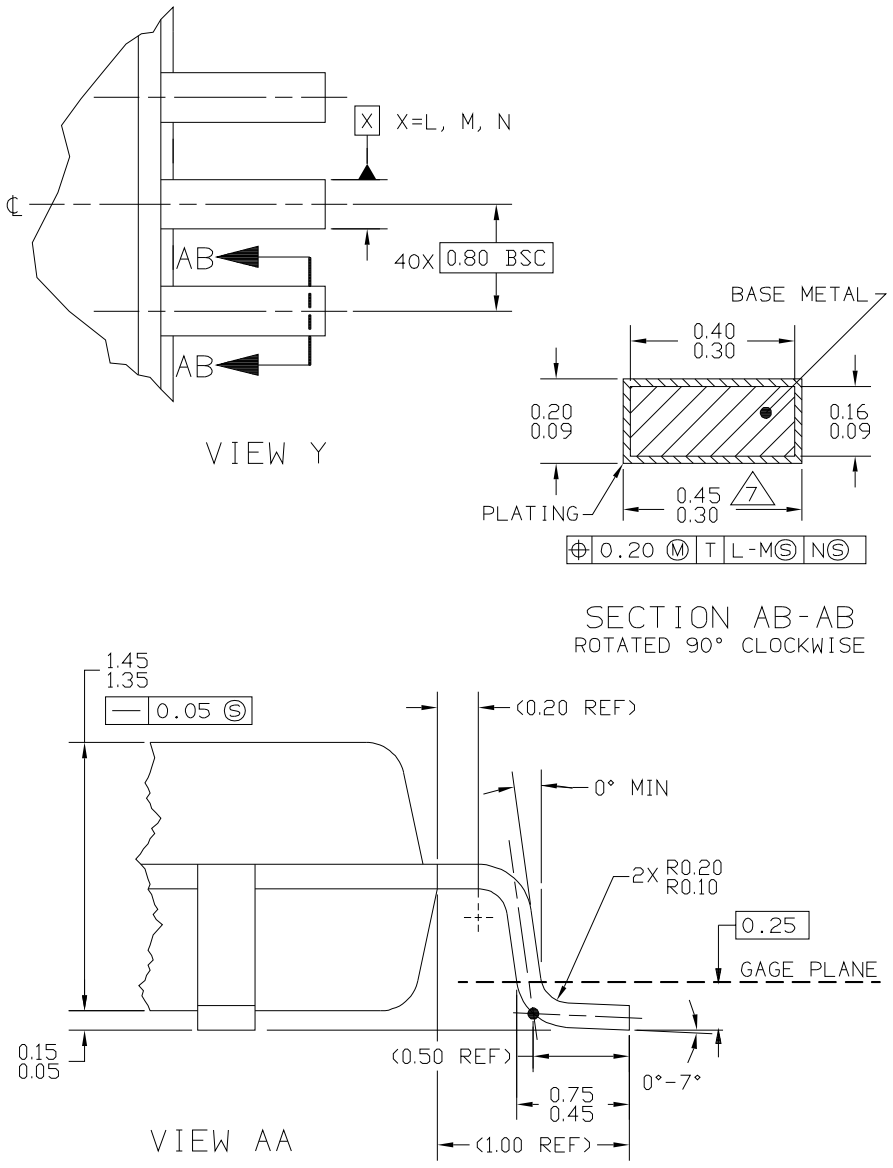
TITLE: 44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23225W	REV: D
	CASE NUMBER: 824D-02	26 FEB 2007
	STANDARD: JEDEC MS-026-BCB	

Figure 33. 44-pin LQFP Package Drawing (Case 824D, Doc #98ASS23225W), Sheet 1 of 3



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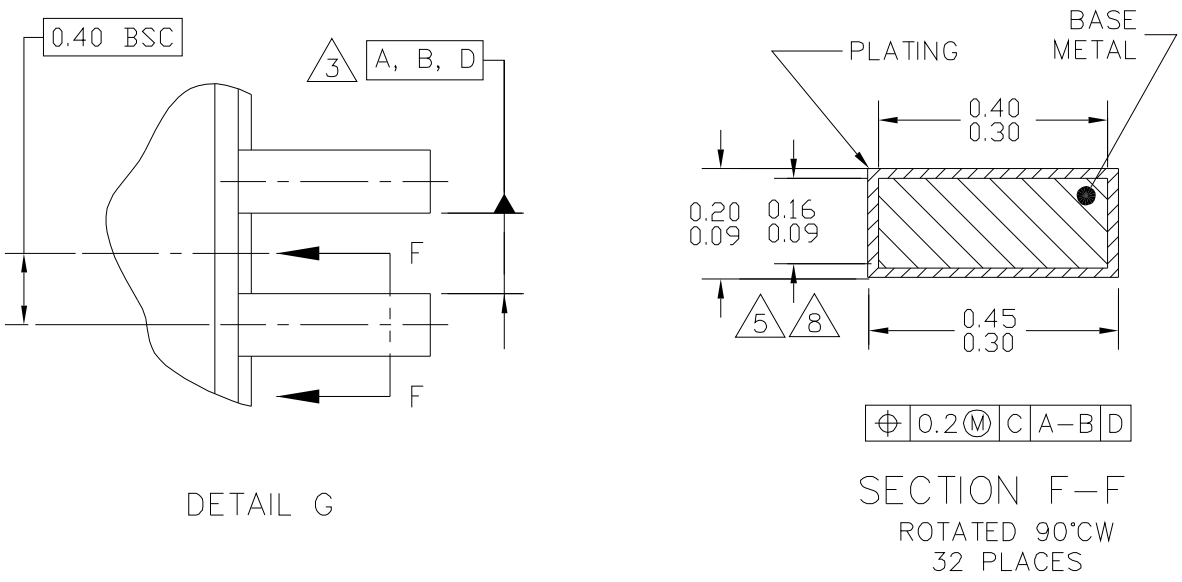
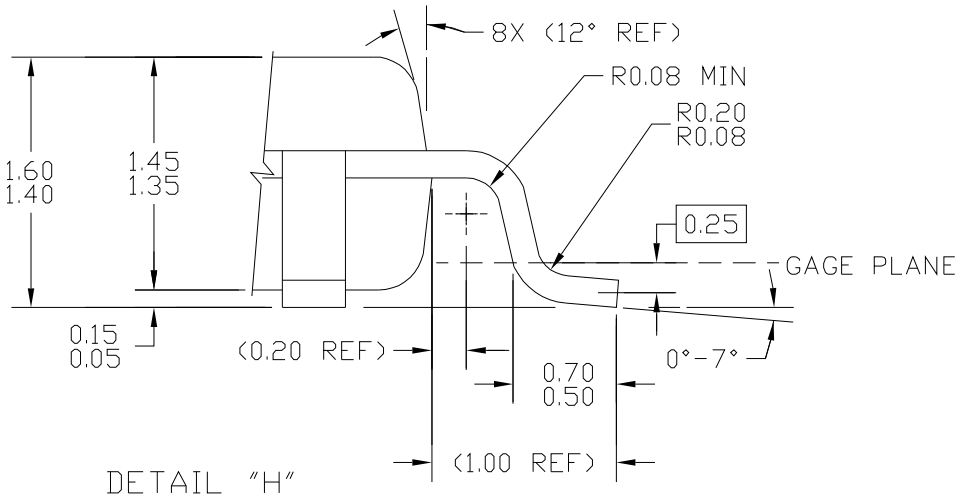
TITLE: 44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23225W	REV: D
	CASE NUMBER: 824D-02	26 FEB 2007
	STANDARD: JEDEC MS-026 BCB	

Figure 34. 44-pin LQFP Package Drawing (Case 824D, Doc #98ASS23225W), Sheet 2 of 3





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TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A	REV: D
	CASE NUMBER: 873A-03	19 MAY 2005
	STANDARD: JEDEC MS-026 BBA	

Figure 37. 32-pin LQFP Package Drawing (Case 873A, Doc #98ASH70029A), Sheet 2 of 3