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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	S08
Core Size	8-Bit
Speed	50MHz
Connectivity	I <sup>2</sup> C, LINbus, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 22x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/pc9s08qe64clh">https://www.e-xfl.com/product-detail/nxp-semiconductors/pc9s08qe64clh</a>

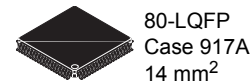
Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

## MC9S08QE128 Series

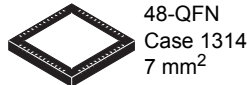
Covers: MC9S08QE128, MC9S08QE96, MC9S08QE64

- 8-Bit HCS08 Central Processor Unit (CPU)
  - Up to 50.33-MHz HCS08 CPU above 2.4V, 40-MHz CPU above 2.1V, and 20-MHz CPU above 1.8V, across temperature range
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Flash read/program/erase over full operating voltage and temperature
  - Random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two low power stop modes; reduced power wait mode
  - Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode
  - Very low power external oscillator can be used in stop3 mode to provide accurate clock to active peripherals
  - Very low power real time counter for use in run, wait, and stop modes with internal and external clock sources
  - 6  $\mu$ s typical wake up time from stop modes
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — FLL controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation; supports CPU freq. from 2 to 50.33 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints)
  - On-chip in-circuit emulator (ICE) debug module containing two comparators and nine trigger modes.

## MC9S08QE128



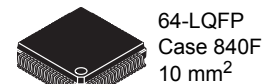
80-LQFP  
Case 917A  
14 mm<sup>2</sup>



48-QFN  
Case 1314  
7 mm<sup>2</sup>



32-LQFP  
Case 873A  
7 mm<sup>2</sup>



64-LQFP  
Case 840F  
10 mm<sup>2</sup>



44-LQFP  
Case 824D  
10 mm<sup>2</sup>

Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints.

- ADC — 24-channel, 12-bit resolution; 2.5  $\mu$ s conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6V to 1.8V
- ACMPx — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; outputs can be optionally routed to TPM module; operation in stop3
- SCIx — Two SCIs with full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake up on active edge
- SPIx — Two serial peripheral interfaces with Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; MSB-first or LSB-first shifting
- IICx — Two IICs with; Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10 bit addressing
- TPMx — One 6-channel and two 3-channel; Selectable input capture, output compare, or buffered edge- or center-aligned PWMs on each channel
- RTC — 8-bit modulus counter with binary or decimal based prescaler; External clock source for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components
- Input/Output
  - 70 GPIOs and 1 input-only and 1 output-only pin
  - 16 KBI interrupts with selectable polarity
  - Hysteresis and configurable pull-up device on all input pins; Configurable slew rate and drive strength on all output pins.
  - SET/CLR registers on 16 pins (PTC and PTE)

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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# 1 MC9S08QE128 Series Comparison

The following table compares the various device derivatives available within the MC9S08QE128 series.

**Table 1. MC9S08QE128 Series Features by MCU and Package**

Feature	MC9S08QE128				MC9S08QE96				MC9S08QE64			
Flash size (bytes)	131072				98304				65536			
RAM size (bytes)	8064				6016				4096			
Pin quantity	80	64	48	44	80	64	48	44	64	48	44	32
ACMP1	yes											
ACMP2	yes											
ADC channels	24	22	10	10	24	22	10	10	22	10	10	10
DBG	yes											
ICS	yes											
IIC1	yes											
IIC2	yes	yes	no	no	yes	yes	no	no	yes	no	no	no
IRQ	yes											
KBI	16	16	16	16	16	16	16	16	16	16	16	12
Port I/O <sup>1</sup>	70	54	38	34	70	54	38	34	54	38	34	26
RTC	yes											
SCI1	yes											
SCI2	yes											
SPI1	yes											
SPI2	yes											
TPM1 channels	3											
TPM2 channels	3											
TPM3 channels	6											
XOSC	yes											

<sup>1</sup> Port I/O count does not include the input only PTA5/IRQ/TPM1CLK/RESET or the output only PTA4/ACMP1O/BKGD/MS.

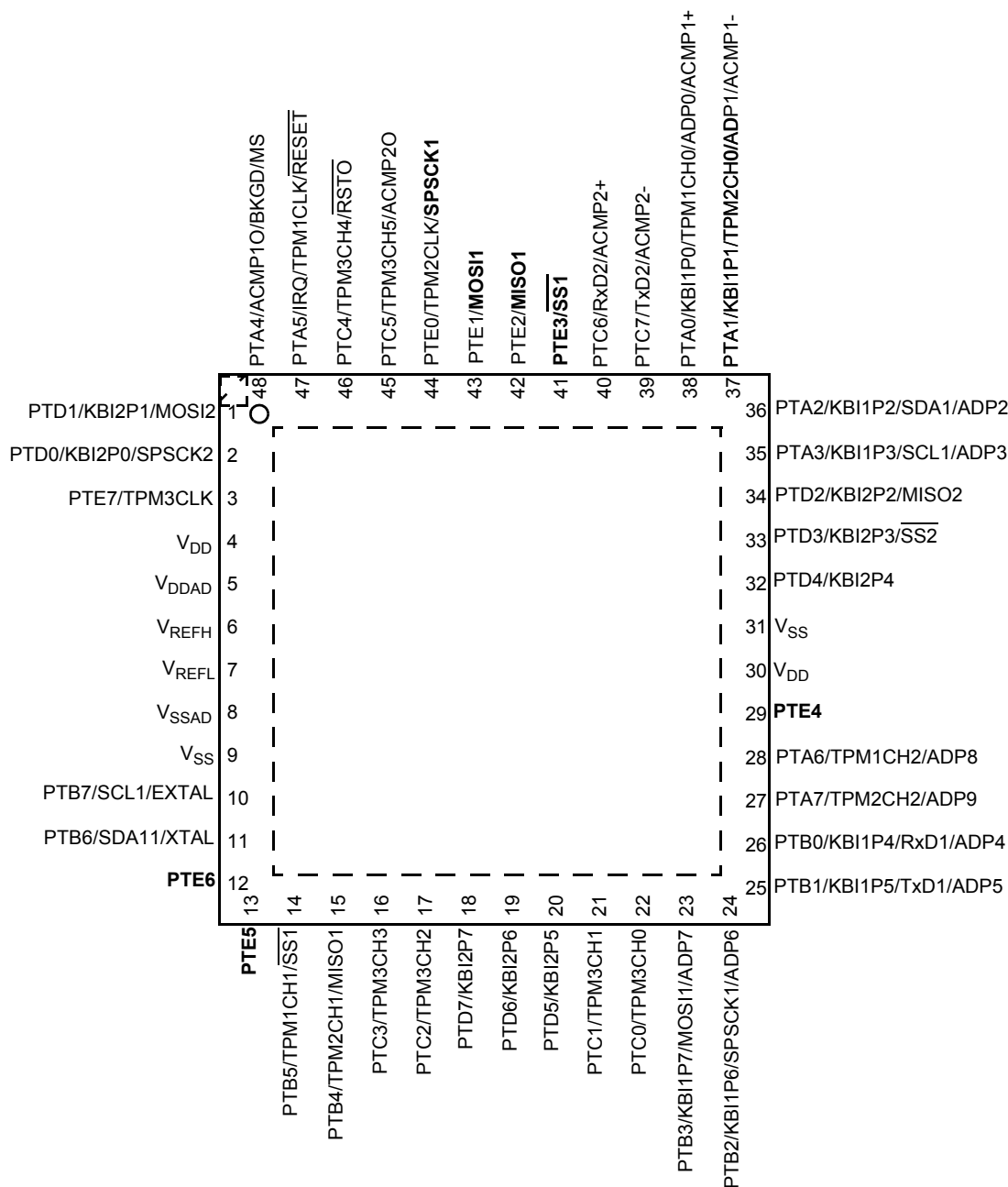


Figure 4. Pin Assignments in 48-Pin QFN Package

## 3 Electrical Characteristics

### 3.1 Introduction

This section contains electrical and timing specifications for the MC9S08QE128 series of microcontrollers available at the time of publication.

### 3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

**Table 3. Parameter Classifications**

<b>P</b>	Those parameters are guaranteed during production testing on each individual device.
<b>C</b>	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
<b>T</b>	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
<b>D</b>	Those parameters are derived mainly from simulations.

#### NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

### 3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either  $V_{SS}$  or  $V_{DD}$ ) or the programmable pull-up resistor associated with the pin is enabled.

**Table 4. Absolute Maximum Ratings**

Rating	Symbol	Value	Unit
Supply voltage	$V_{DD}$	−0.3 to +3.8	V
Maximum current into $V_{DD}$	$I_{DD}$	120	mA
Digital input voltage	$V_{In}$	−0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) <sup>1, 2, 3</sup>	$I_D$	± 25	mA
Storage temperature range	$T_{stg}$	−55 to 150	°C

<sup>1</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive ( $V_{DD}$ ) and negative ( $V_{SS}$ ) clamp voltages, then use the larger of the two resistance values.

<sup>2</sup> All functional non-supply pins are internally clamped to  $V_{SS}$  and  $V_{DD}$ .

## Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ <sup>1</sup>	Max	Unit
18	P	Low-voltage detection threshold — low range <sup>7</sup>	$V_{LVDL}$	$V_{DD}$ falling $V_{DD}$ rising	1.80 1.86	1.82 1.90	1.91 1.99	V
19	P	Low-voltage warning threshold — high range <sup>7</sup>	$V_{LVWH}$	$V_{DD}$ falling $V_{DD}$ rising	2.36 2.36	2.46 2.46	2.56 2.56	V
20	P	Low-voltage warning threshold — low range <sup>7</sup>	$V_{LVWL}$	$V_{DD}$ falling $V_{DD}$ rising	2.11 2.16	2.16 2.21	2.22 2.27	V
21	C	Low-voltage inhibit reset/recover hysteresis <sup>7</sup>	$V_{hys}$		—	50	—	mV
22	P	Bandgap Voltage Reference <sup>9</sup>	$V_{BG}$		1.15	1.17	1.18	V

<sup>1</sup> Typical values are measured at 25°C. Characterized, not tested

<sup>2</sup> As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above  $V_{LVDL}$ .

<sup>3</sup> All functional non-supply pins are internally clamped to  $V_{SS}$  and  $V_{DD}$ .

<sup>4</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

<sup>5</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{in} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

<sup>6</sup> Maximum is highest voltage that POR is guaranteed.

<sup>7</sup> Low voltage detection and warning limits measured at 1 MHz bus frequency.

<sup>8</sup> Run at 1 MHz bus frequency

<sup>9</sup> Factory trimmed at  $V_{DD} = 3.0$  V, Temp = 25°C

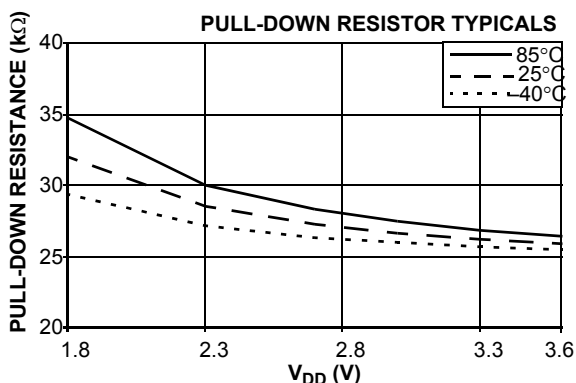
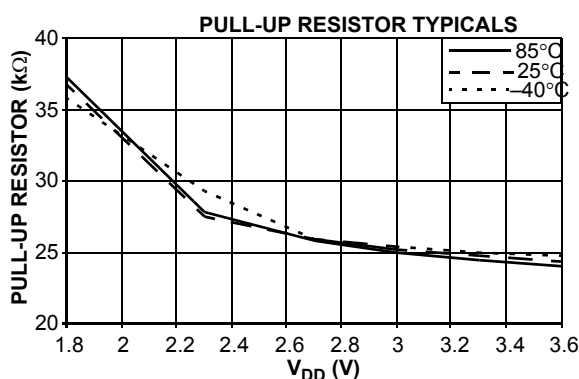
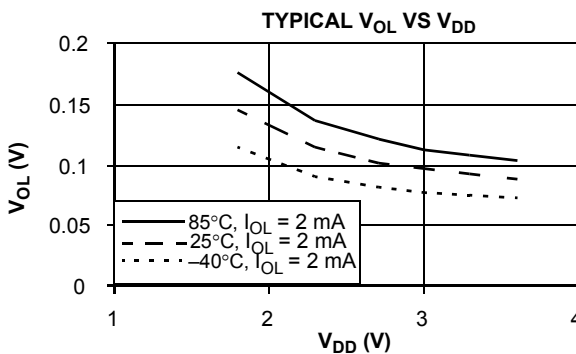
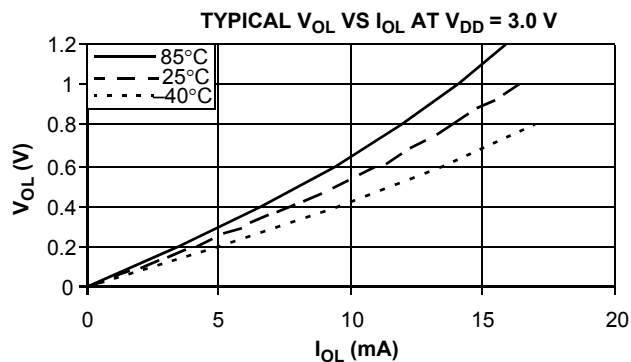
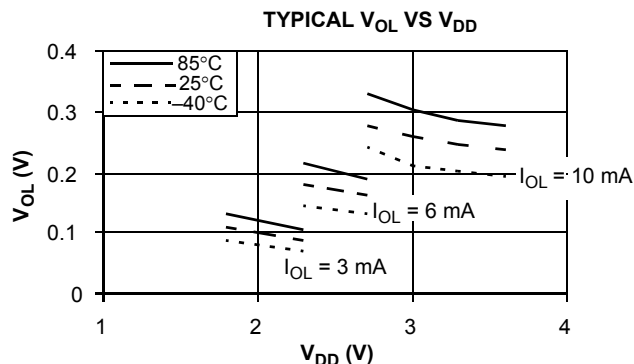
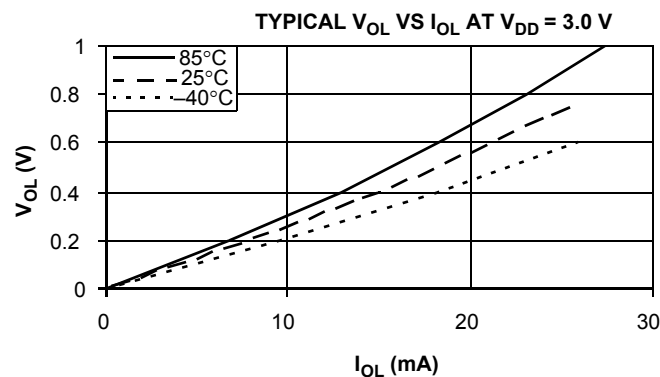


Figure 7. Pull-up and Pull-down Typical Resistor Values

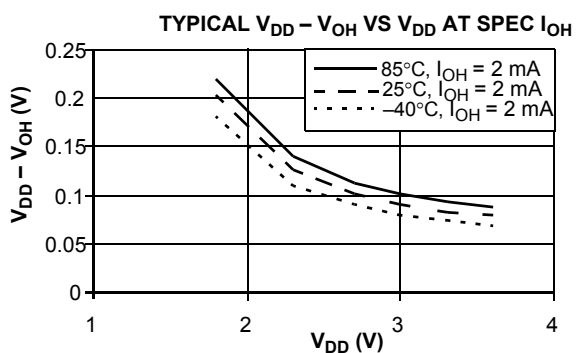
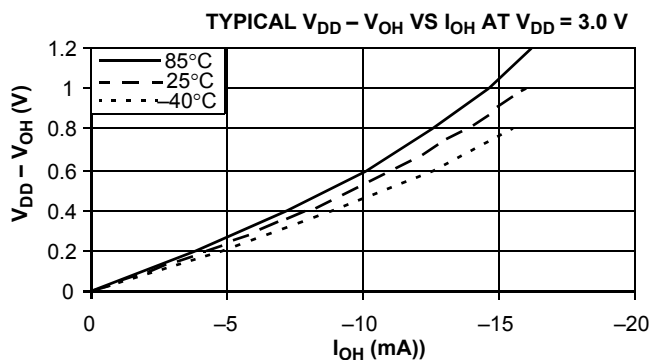




**Figure 8. Typical Low-Side Driver (Sink) Characteristics — Low Drive ( $PTxDSn = 0$ )**



**Figure 9. Typical Low-Side Driver (Sink) Characteristics — High Drive ( $PTxDSn = 1$ )**



**Figure 10. Typical High-Side (Source) Characteristics — Low Drive ( $PTxDSn = 0$ )**

## 3.8 External Oscillator (XOSC) Characteristics

Reference Figure 13 and Figure 14 for crystal or resonator circuits.

**Table 11. XOSC and ICS Specifications (Temperature Range = -40 to 85°C Ambient)**

Num	C	Characteristic	Symbol	Min	Typ <sup>1</sup>	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)					
		Low range (RANGE = 0)	$f_{lo}$	32	—	38.4	kHz
		High range (RANGE = 1), high gain (HGO = 1)	$f_{hi}$	1	—	16	MHz
		High range (RANGE = 1), low power (HGO = 0)	$f_{hi}$	1	—	8	MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	$C_1, C_2$	See Note <sup>2</sup> See Note <sup>3</sup>			
3	D	Feedback resistor	$R_F$				
		Low range, low power (RANGE=0, HGO=0) <sup>2</sup>		—	—	—	MΩ
		Low range, High Gain (RANGE=0, HGO=1)		—	10	—	
		High range (RANGE=1, HGO=X)		—	1	—	
4	D	Series resistor —	$R_S$				kΩ
		Low range, low power (RANGE = 0, HGO = 0) <sup>2</sup>		—	—	—	
		Low range, high gain (RANGE = 0, HGO = 1)		—	0	—	
		High range, low power (RANGE = 1, HGO = 0)		—	100	—	
		High range, high gain (RANGE = 1, HGO = 1)					
		≥ 8 MHz		—	0	0	
		4 MHz		—	0	10	
		1 MHz		—	0	20	
5	C	Crystal start-up time <sup>4</sup>					ms
		Low range, low power	$t_{CSTL}$	—	200	—	
		Low range, high power		—	400	—	
		High range, low power	$t_{CSTH}$	—	5	—	
		High range, high power		—	15	—	
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)					
		FEE or FBE mode	$f_{extal}$	0.03125	—	40.0	MHz
		FBELP mode		0	—	50.33	MHz

<sup>1</sup> Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

<sup>2</sup> Load capacitors ( $C_1, C_2$ ), feedback resistor ( $R_F$ ) and series resistor ( $R_S$ ) are incorporated internally when RANGE=HGO=0.

<sup>3</sup> See crystal or resonator manufacturer's recommendation.

<sup>4</sup> Proper PC board layout procedures must be followed to achieve specifications.

**Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)**

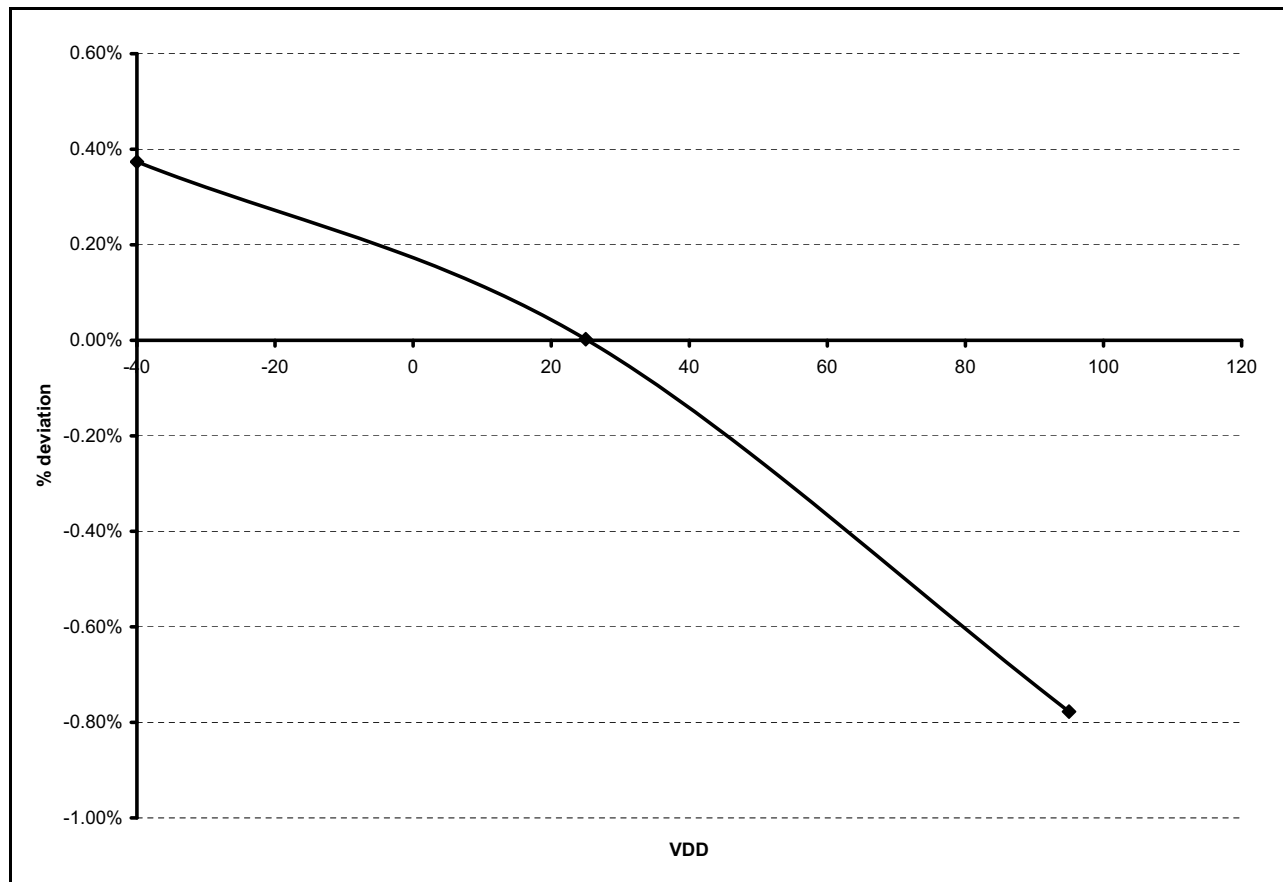
Num	C	Characteristic	Symbol	Min	Typ <sup>1</sup>	Max	Unit
8	C	Total deviation of trimmed DCO output frequency over voltage and temperature	$\Delta f_{\text{dco\_t}}$	—	+ 0.5 –1.0	± 2	% $f_{\text{dco}}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C	$\Delta f_{\text{dco\_t}}$	—	± 0.5	± 1	% $f_{\text{dco}}$
10	C	FLL acquisition time <sup>3</sup>	$t_{\text{Acquire}}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval) <sup>4</sup>	$C_{\text{Jitter}}$	—	0.02	0.2	% $f_{\text{dco}}$

<sup>1</sup> Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

<sup>2</sup> The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

<sup>3</sup> This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

<sup>4</sup> Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum  $f_{\text{Bus}}$ . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via  $V_{\text{DD}}$  and  $V_{\text{SS}}$  and variation in crystal oscillator frequency increase the  $C_{\text{Jitter}}$  percentage for a given interval.


**Figure 15. Deviation of DCO Output Across Temperature at  $V_{\text{DD}} = 3.0 \text{ V}$**

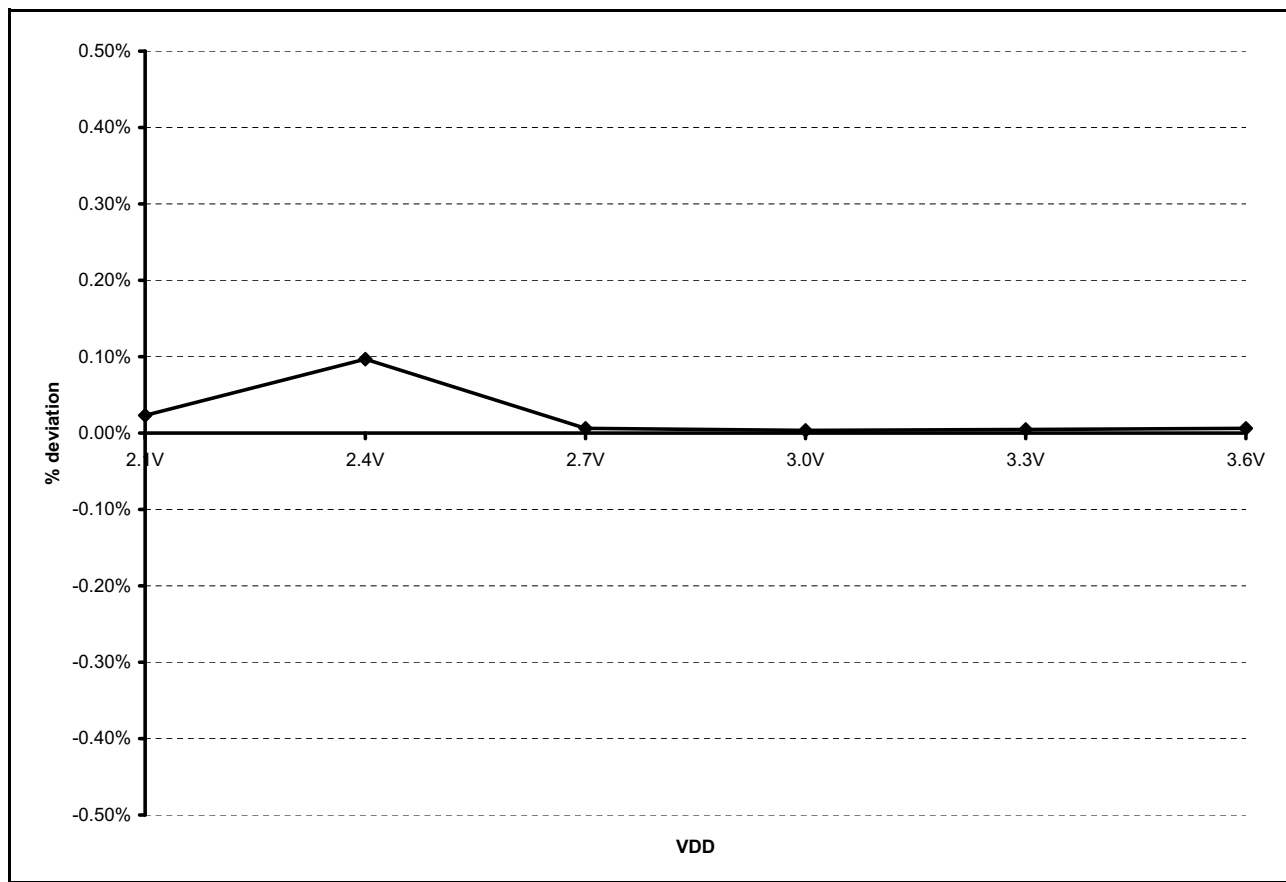


Figure 16. Deviation of DCO Output Across  $V_{DD}$  at 25°C

## 3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

### 3.10.1 Control Timing

Table 13. Control Timing

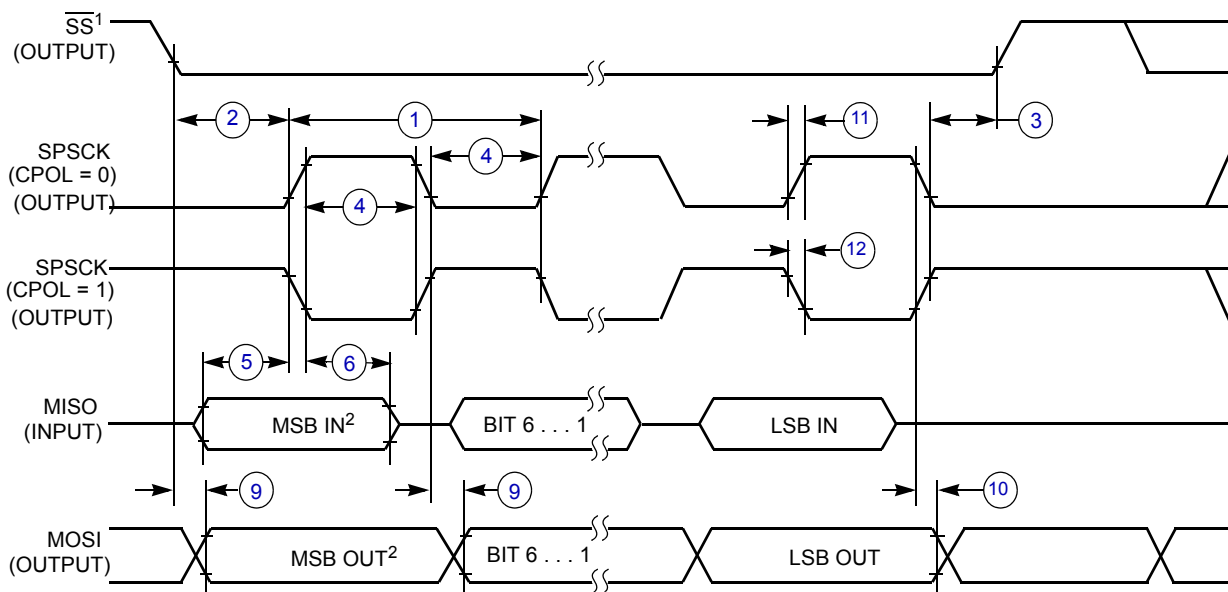
Num	C	Rating	Symbol	Min	Typ <sup>1</sup>	Max	Unit
1	D	Bus frequency ( $t_{cyc} = 1/f_{Bus}$ ) $V_{DD} \geq 1.8V$ $V_{DD} > 2.1V$ $V_{DD} > 2.4V$	$f_{Bus}$	dc	— — —	10 20 25.165	MHz
2	D	Internal low power oscillator period	$t_{LPO}$	700	—	1300	$\mu s$
3	D	External reset pulse width <sup>2</sup>	$t_{extrst}$	100	—	—	ns
4	D	Reset low drive	$t_{rstdrv}$	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	$t_{MSSU}$	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes <sup>3</sup>	$t_{MSH}$	100	—	—	$\mu s$

### 3.10.3 SPI Timing

Table 15 and Figure 21 through Figure 24 describe the timing requirements for the SPI system.

**Table 15. SPI Timing**

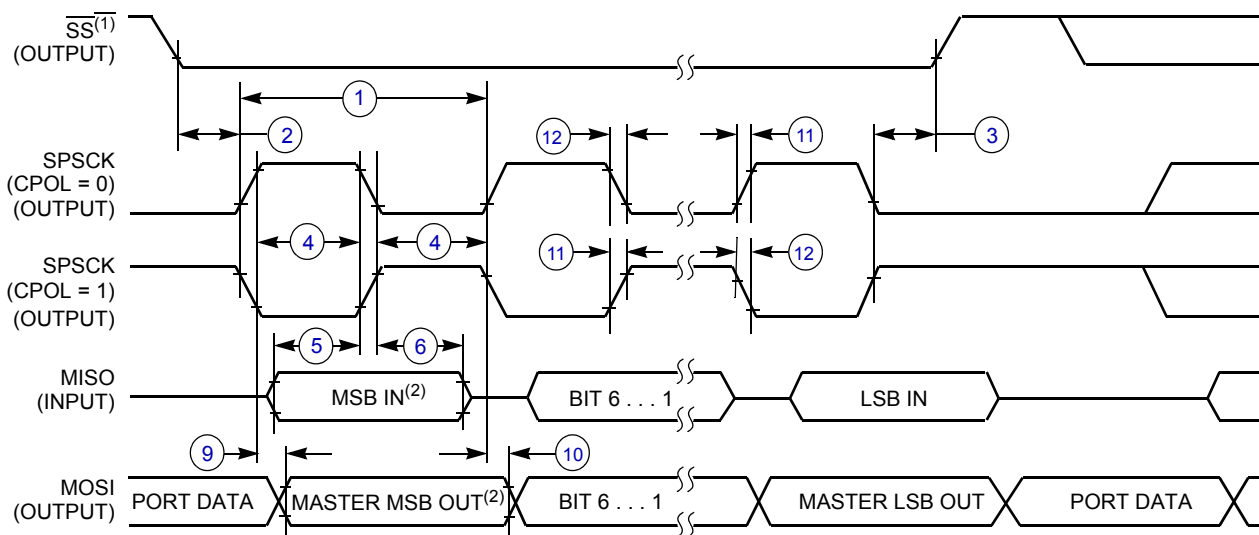
No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	$f_{op}$	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz Hz
1	D	SPSCK period Master Slave	$t_{SPSCK}$	2 4	2048 —	$t_{cyc}$ $t_{cyc}$
2	D	Enable lead time Master Slave	$t_{Lead}$	1/2 1	— —	$t_{SPSCK}$ $t_{cyc}$
3	D	Enable lag time Master Slave	$t_{Lag}$	1/2 1	— —	$t_{SPSCK}$ $t_{cyc}$
4	D	Clock (SPSCK) high or low time Master Slave	$t_{WSPSCK}$	$t_{cyc} - 30$ $t_{cyc} - 30$	$1024 t_{cyc}$ —	ns ns
5	D	Data setup time (inputs) Master Slave	$t_{SU}$	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	$t_{HI}$	0 25	— —	ns ns
7	D	Slave access time	$t_a$	—	1	$t_{cyc}$
8	D	Slave MISO disable time	$t_{dis}$	—	1	$t_{cyc}$
9	D	Data valid (after SPSCK edge) Master Slave	$t_v$	— —	25 25	ns ns
10	D	Data hold time (outputs) Master Slave	$t_{HO}$	0 0	— —	ns ns
11	D	Rise time Input Output	$t_{RI}$ $t_{RO}$	— —	$t_{cyc} - 25$ 25	ns ns
12	D	Fall time Input Output	$t_{FI}$ $t_{FO}$	— —	$t_{cyc} - 25$ 25	ns ns



## NOTES:

1.  $\overline{SS}$  output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

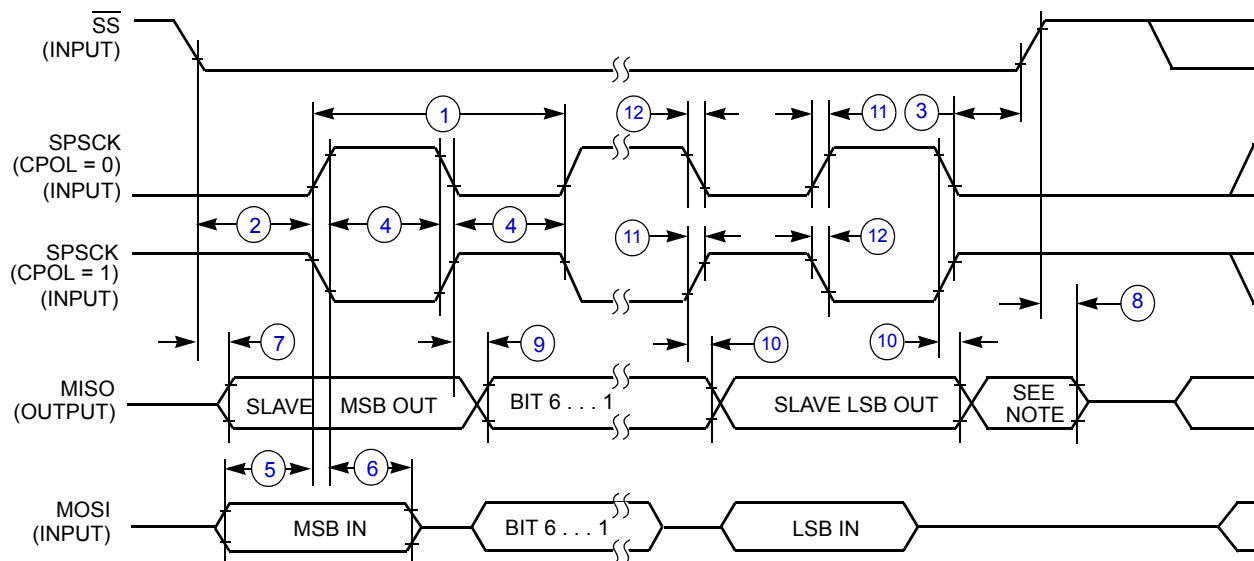
**Figure 21. SPI Master Timing (CPHA = 0)**



## NOTES:

1.  $\overline{SS}$  output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

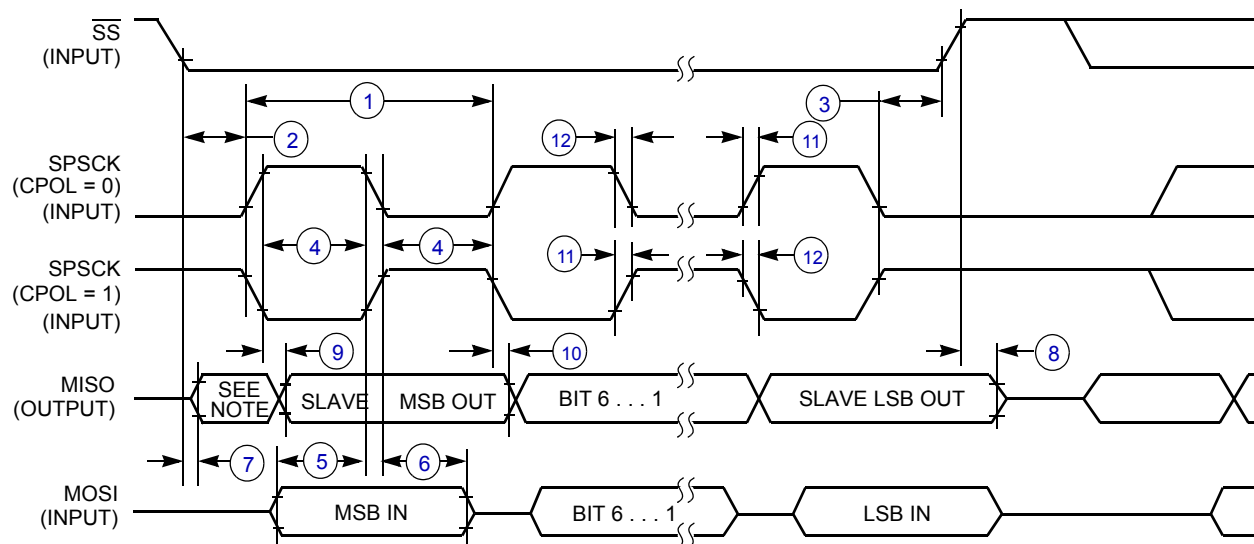
**Figure 22. SPI Master Timing (CPHA = 1)**



NOTE:

1. Not defined but normally MSB of character just received

**Figure 23. SPI Slave Timing (CPHA = 0)**



NOTE:

1. Not defined but normally LSB of character just received

**Figure 24. SPI Slave Timing (CPHA = 1)**

### 3.11 Analog Comparator (ACMP) Electricals

Table 16. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	$V_{DD}$	1.80	—	3.6	V
C	Supply current (active)	$I_{DDAC}$	—	20	35	$\mu A$
D	Analog input voltage	$V_{AIN}$	$V_{SS} - 0.3$	—	$V_{DD}$	V
C	Analog input offset voltage	$V_{AIO}$		20	40	mV
C	Analog comparator hysteresis	$V_H$	3.0	9.0	15.0	mV
P	Analog input leakage current	$I_{ALKG}$	—	—	1.0	$\mu A$
C	Analog comparator initialization delay	$t_{AINIT}$	—	—	1.0	$\mu s$

### 3.12 ADC Characteristics

Table 17. 12-bit ADC Operating Conditions

C	Characteristic	Conditions	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
D	Supply voltage	Absolute	$V_{DDAD}$	1.8	—	3.6	V	
		Delta to $V_{DD}$ ( $V_{DD} - V_{DDAD}$ ) <sup>2</sup>	$\Delta V_{DDAD}$	-100	0	+100	mV	
D	Ground voltage	Delta to $V_{SS}$ ( $V_{SS} - V_{SSAD}$ ) <sup>2</sup>	$\Delta V_{SSAD}$	-100	0	+100	mV	
D	Ref Voltage High		$V_{REFH}$	1.8	$V_{DDAD}$	$V_{DDAD}$	V	
D	Ref Voltage Low		$V_{REFL}$	$V_{SSAD}$	$V_{SSAD}$	$V_{SSAD}$	V	
D	Input Voltage		$V_{ADIN}$	$V_{REFL}$	—	$V_{REFH}$	V	
C	Input Capacitance		$C_{ADIN}$	—	4.5	5.5	pF	
C	Input Resistance		$R_{ADIN}$	—	5	7	k $\Omega$	
C	Analog Source Resistance	12 bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$	$R_{AS}$	— —	— —	2 5	k $\Omega$	External to MCU
		10 bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$		— —	— —	5 10		
		8 bit mode (all valid $f_{ADCK}$ )		—	—	10		
D	ADC Conversion Clock Freq.	High Speed (ADLPC=0)	$f_{ADCK}$	0.4	—	8.0	MHz	
		Low Power (ADLPC=1)		0.4	—	4.0		

<sup>1</sup> Typical values assume  $V_{DDAD} = 3.0\text{V}$ , Temp = 25°C,  $f_{ADCK} = 1.0\text{MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup> DC potential difference.



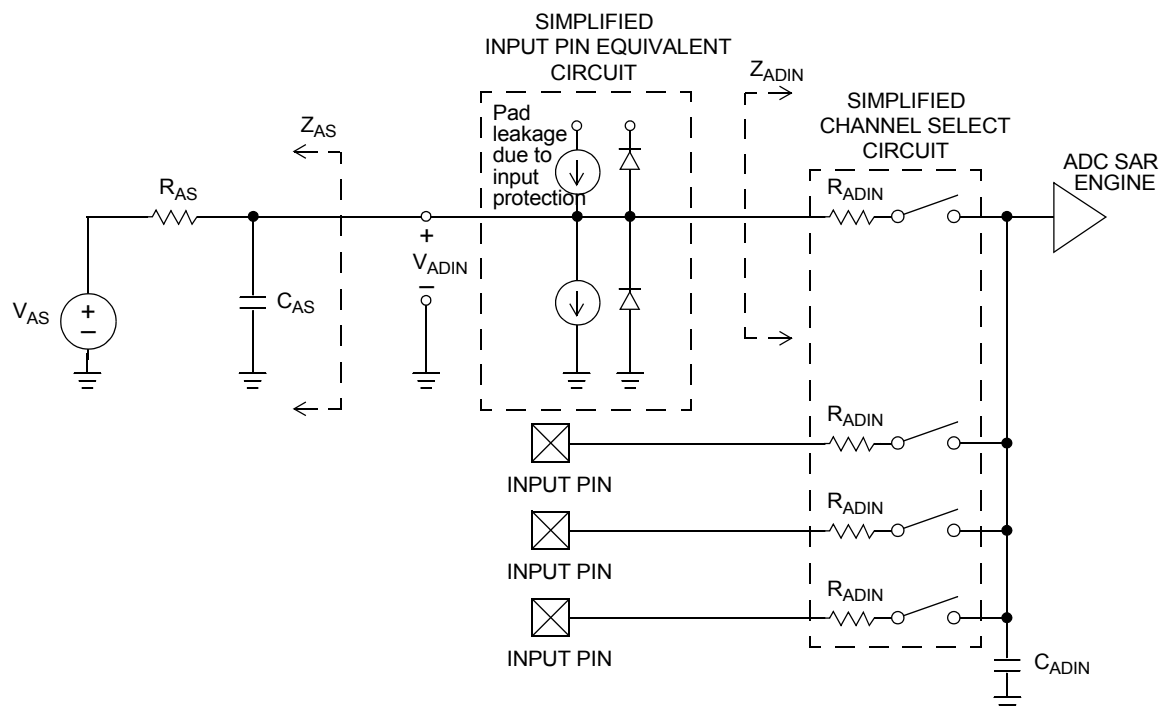
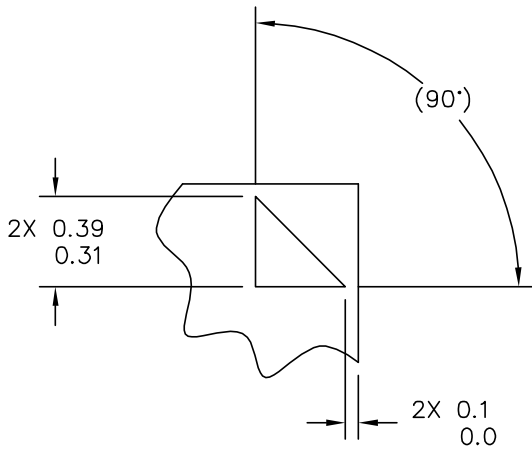
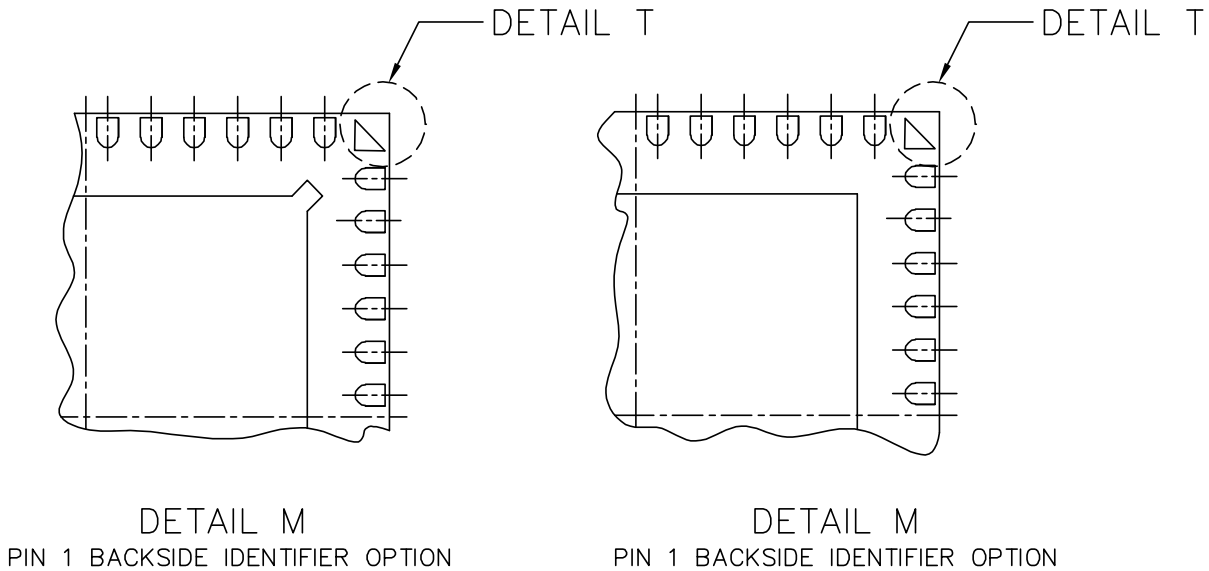


Figure 25. ADC Input Impedance Equivalency Diagram

 Table 18. 12-bit ADC Characteristics ( $V_{REFH} = V_{DDAD}$ ,  $V_{REFL} = V_{SSAD}$ )

Characteristic	Conditions	C	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
Supply Current ADLPC=1 ADLSMP=1 ADCO=1		T	$I_{DDAD}$	—	120	—	$\mu A$	
Supply Current ADLPC=1 ADLSMP=0 ADCO=1		T	$I_{DDAD}$	—	202	—	$\mu A$	
Supply Current ADLPC=0 ADLSMP=1 ADCO=1		T	$I_{DDAD}$	—	288	—	$\mu A$	
Supply Current ADLPC=0 ADLSMP=0 ADCO=1		D	$I_{DDAD}$	—	0.532	1	mA	
Supply Current	Stop, Reset, Module Off	P	$I_{DDAD}$	—	0.007	0.8	$\mu A$	
ADC Asynchronous Clock Source	High Speed (ADLPC=0)	P	$f_{ADACK}$	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
	Low Power (ADLPC=1)	P		1.25	2	3.3		

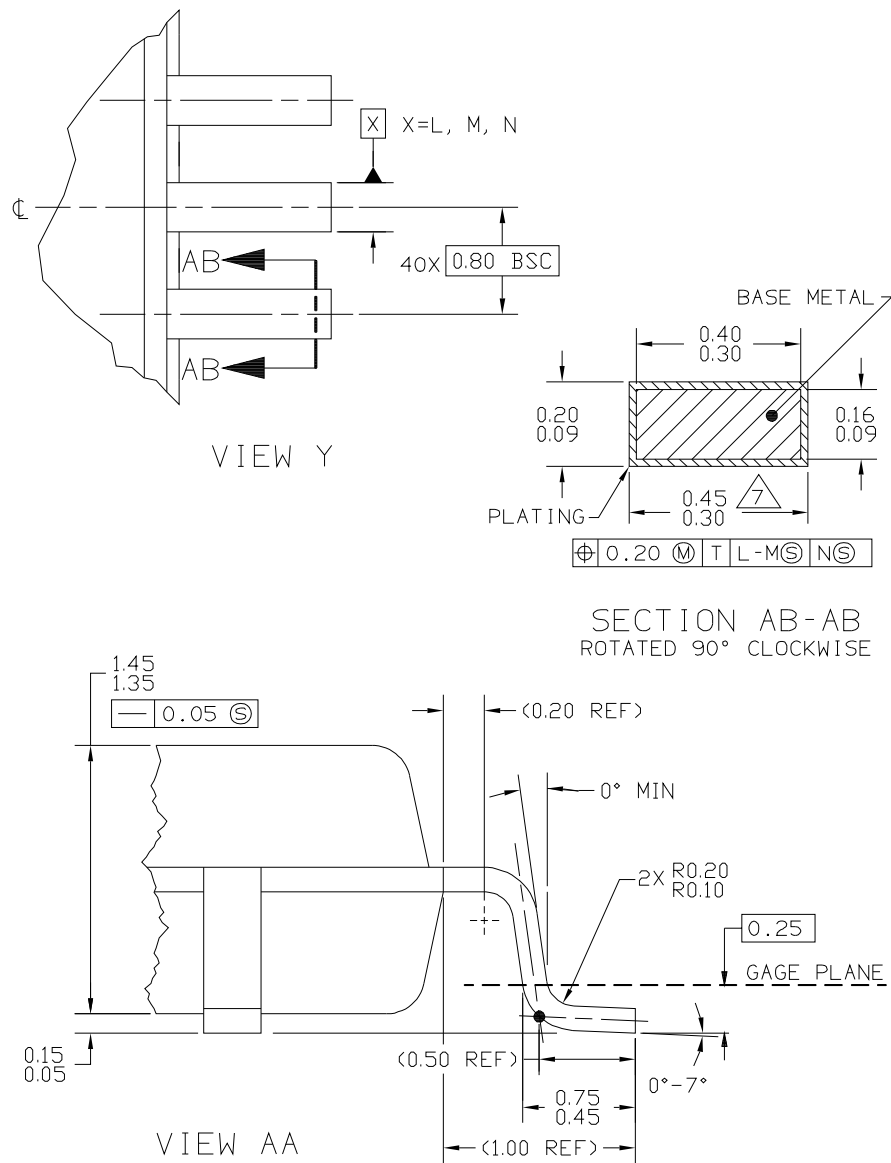


DETAIL T

- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
  3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFN.
  4. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
  5. MIN METAL GAP SHOULD BE 0.2MM.

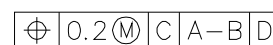
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	<b>MECHANICAL OUTLINE</b>	PRINT VERSION NOT TO SCALE	
		DOCUMENT NO: 98ARH99048A	REV: F
TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)		CASE NUMBER: 1314-05	05 DEC 2005
		STANDARD: JEDEC-MO-220 VKKD-2	

Figure 32. 48-pin QFN Package Drawing (Case 1314, Doc #98ARH99048A), Sheet 3 of 3



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TITLE:  44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK			DOCUMENT NO: 98ASS23225W		REV: D
			CASE NUMBER: 824D-02		26 FEB 2007
			STANDARD: JEDEC MS-026 BCB		

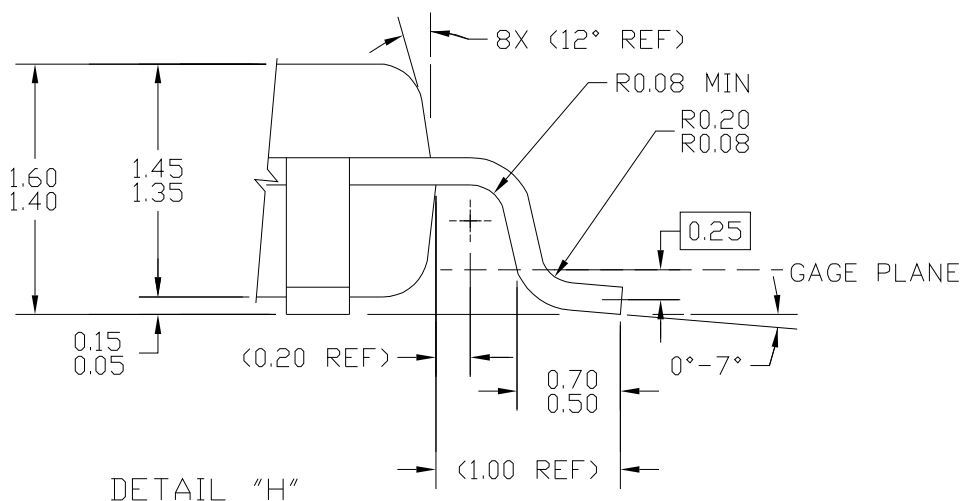
Figure 34. 44-pin LQFP Package Drawing (Case 824D, Doc #98ASS23225W), Sheet 2 of 3



SECTION F-F

ROTATED 90°CW

32 PLACES



**Figure 37. 32-pin LQFP Package Drawing (Case 873A, Doc #98ASH70029A), Sheet 2 of 3**

## Package Information

### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A	REV: D
	CASE NUMBER: 873A-03	19 MAY 2005
	STANDARD: JEDEC MS-026 BBA	

**Figure 38. 32-pin LQFP Package Drawing (Case 873A, Doc #98ASH70029A), Sheet 3 of 3**