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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	32-Bit
Speed	24MHz
Connectivity	SCI, SmartCard, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	68
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b SAR; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2215cubr24v

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions may occur due to the false recognition of the pin state as an input signal. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

2.4.1 General Registers

The H8S/2000 CPU has eight 32-bit general registers. These general registers are all functionally alike and can be used as both address registers and data registers. When a general register is used as a data register, it can be accessed as a 32-bit, 16-bit, or 8-bit register. Figure 2.7 illustrates the usage of the general registers. When the general registers are used as 32-bit registers or address registers, they are designated by the letters ER (ER0 to ER7).

The ER registers divide into 16-bit general registers designated by the letters E (E0 to E7) and R (R0 to R7). These registers are functionally equivalent, providing a maximum sixteen 16-bit registers. The E registers (E0 to E7) are also referred to as extended registers.

The R registers divide into 8-bit general registers designated by the letters RH (R0H to R7H) and RL (R0L to R7L). These registers are functionally equivalent, providing a maximum sixteen 8-bit registers.

The usage of each register can be selected independently.

General register ER7 has the function of stack pointer (SP) in addition to its general-register function, and is used implicitly in exception handling and subroutine calls. Figure 2.8 shows the stack.

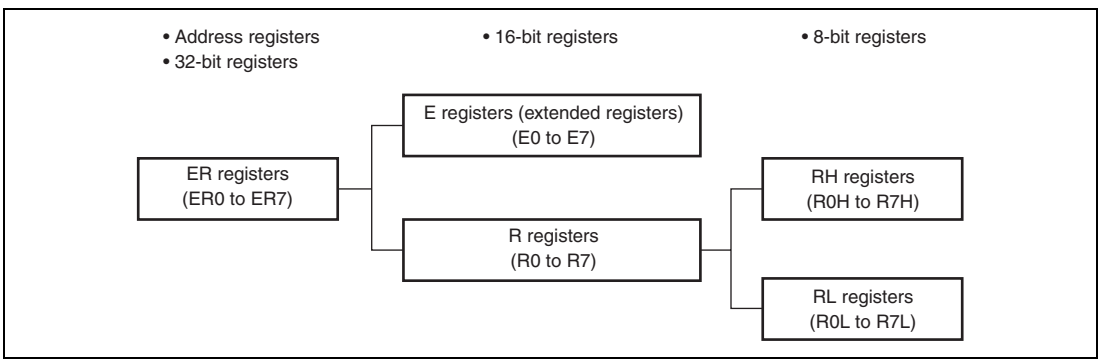


Figure 2.7 Usage of General Registers

- Full Address Mode

Bit	Bit Name	Initial Value	R/W	Description
15	FAE1	0	R/W	Full Address Enable 1 Specifies whether channel 1 is to be used in short address mode or full address mode. In full address mode, channels 1A and 1B are used together as a single channel. 0: Short address mode 1: Full address mode
14	FAE0	0	R/W	Full Address Enable 0 Specifies whether channel 0 is to be used in short address mode or full address mode. In full address mode, channels 0A and 0B are used together as a single channel. 0: Short address mode 1: Full address mode
13, 12	—	All 0	R/W	Reserved Although these bits are readable/writable, only 0 should be written here.

8.2.5 DTC Transfer Count Register A (CRA)

CRA is a 16-bit register that designates the number of times data is to be transferred by the DTC. In normal mode, the entire CRA functions as a 16-bit transfer counter (1 to 65,536). It is decremented by 1 every time data is transferred, and transfer ends when the count reaches H'0000. In repeat mode or block transfer mode, the CRA is divided into two parts: the upper 8 bits (CRAH) and the lower 8 bits (CRAL). CRAH holds the number of transfers while CRAL functions as an 8-bit transfer counter (1 to 256). In block transfer mode, CRAH stores the block size while CRAL functions as an 8-bit block size counter (1 to 256). CRAL is decremented by 1 every time data is transferred, and the contents of CRAH are sent when the count reaches H'00. This operation is repeated.

8.2.6 DTC Transfer Count Register B (CRB)

CRB is a 16-bit register that designates the number of times data is to be transferred by the DTC in block transfer mode. It functions as a 16-bit transfer counter (1 to 65,536) that is decremented by 1 every time data is transferred, and transfer ends when the count reaches H'0000.

8.2.7 DTC Enable Registers (DTCERA to DTCERF)

DTCER which is comprised of seven registers, DTCERA to DTCERF, is a register that specifies DTC activation interrupt sources. The correspondence between interrupt sources and DTCE bits is shown in table 8.2. For DTCE bit setting, use bit manipulation instructions such as BSET and BCLR for reading and writing. If all interrupts are masked, multiple activation sources can be set at one time (only at the initial setting) by writing data after executing a dummy read on the relevant register.

Bit	Bit Name	Initial Value	R/W	Description
7	DTCEn7	0	R/W	DTC Activation Enable 7 to 0
6	DTCEn6	0	R/W	0: Prohibits DTC startup by an interrupt.
5	DTCEn5	0	R/W	1: Selects a corresponding interrupt source as the DTC startup source.
4	DTCEn4	0	R/W	
3	DTCEn3	0	R/W	[Clearing conditions]
2	DTCEn2	0	R/W	• When the DISEL bit is 1 and the data transfer has ended
1	DTCEn1	0	R/W	
0	DTCEn0	0	R/W	• When the specified number of transfers have ended [Holding condition] • These bits are not cleared when the DISEL bit is 0 and the specified number of transfers have not ended

Bit	Bit Name	Initial value	R/W	Description
3	TGFD	0	R/(W)*	Input Capture/Output Compare Flag D Status flag that indicates the occurrence of TGRD input capture or compare match in channel 0. The write value should always be 0 to clear this flag. In channels 1 and 2, bit 3 is reserved. It is always read as 0 and cannot be modified. [Setting conditions] • When TCNT = TGRD while TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal while TGRD is functioning as input capture register [Clearing conditions] • When DTC is activated by TGID interrupt, DISEL bit in MRB of DTC is cleared to 0, and transfer counter value is not 0 • When 0 is written to TGFD after reading TGFD = 1
2	TGFC	0	R/(W)*	Input Capture/Output Compare Flag C Status flag that indicates the occurrence of TGRC input capture or compare match in channel 0. The write value should always be 0 to clear this flag. In channels 1 and 2, bit 2 is reserved. It is always read as 0 and cannot be modified. [Setting conditions] • When TCNT = TGRC while TGRC is functioning as output compare register • When TCNT value is transferred to TGRC by input capture signal while TGRC is functioning as input capture register [Clearing conditions] • When DTC is activated by TGIC interrupt, DISEL bit in MRB of DTC is cleared to 0, and transfer counter value is not 0 • When 0 is written to TGFC after reading TGFC = 1

11.5.4 Timing of Compare Match Clear

The timer counter is cleared when compare match A or B occurs, depending on the setting of the CCLR1 and CCLR0 bits in TCR. Figure 11.7 shows the timing of this operation.

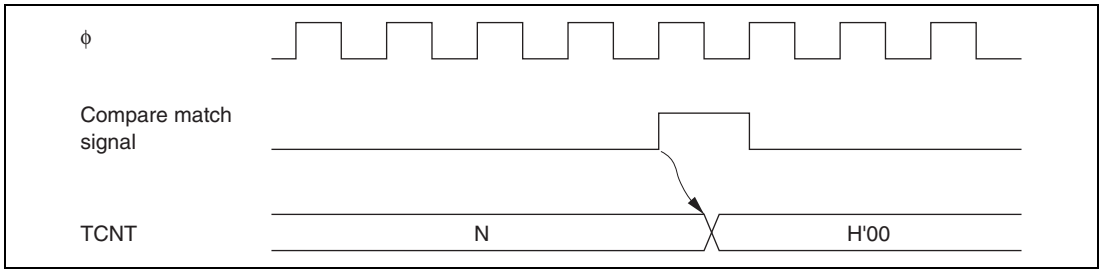


Figure 11.7 Timing of Compare Match Clear

11.5.5 Timing of TCNT External Reset

TCNT is cleared at the rising edge of an external reset input, depending on the settings of the CCLR1 and CCLR0 bits in TCR. The clear pulse width must be at least 1.5 states. Figure 11.8 shows the timing of this operation.

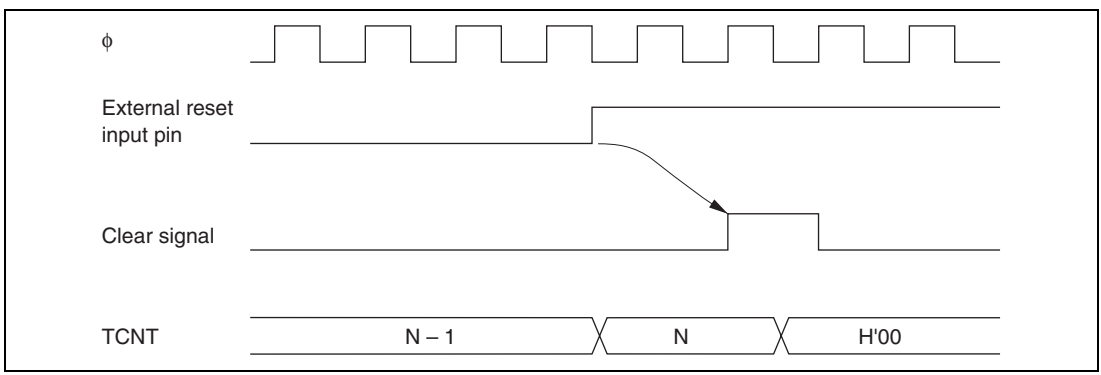


Figure 11.8 Timing of Clearance by External Reset

Bit	Bit Name	Initial Value	R/W	Description
2	ACS2	0	R/W	Asynchronous Clock Source Select 2 to 0
1	ACS1	0	R/W	These bits select the clock source in asynchronous mode.
0	ACS0	0	R/W	When an average transfer rate is selected, the base clock is set automatically regardless of the ABCS value. Note that average transfer rates are not supported for operating frequencies other than 10.667 MHz and 16 MHz. The setting in bits ACS2 to ACS0 is valid when external clock input is used (CKE1 = 1 in SCR) in asynchronous mode (C/A = 0 in SMR). Figures 13.3 and 13.4 show setting examples. 000: External clock input 001: 115.152 kbps average transfer rate (for ϕ = 10.667 MHz only) is selected* (SCI_0 operates on base clock with frequency of 16 times transfer rate) 010: 460.606 kbps average transfer rate (for ϕ = 10.667 MHz only) is selected* (SCI_0 operates on base clock with frequency of 8 times transfer rate) 011: Reserved 100: TPU clock input (AND of TIOCA1 and TIOCA2) The signal generated by TIOCA1 and TIOCA2, which are the compare match outputs for TPU_1 and TPU_2 or PWM outputs, is used as a base clock. Note that IRQ0 and IRQ1 cannot be used since TIOCA1 and TIOCA2 are used as outputs. The high pulse width for TIOCA1 should be its low pulse width or less. 101: 115.196 kbps average transfer rate (for ϕ = 16 MHz only) is selected (SCI_0 operates on base clock with frequency of 16 times transfer rate) 110: 460.784 kbps average transfer rate (for ϕ = 16 MHz only) is selected (SCI_0 operates on base clock with frequency of 16 times transfer rate) 111: 720 kbps average transfer rate (for ϕ = 16 MHz only) is selected (SCI_0 operates on base clock with frequency of 8 times transfer rate)

Note: * Cannot be used in this LSI because the operating frequency ϕ in this LSI is 13 MHz or greater.

Bit	Bit Name	Initial Value	R/W	Description
7	ACS3	0	R/W	Asynchronous Clock Source Select Selects the clock source in asynchronous mode depending on the combination with the ACS2 to ACS0 (bits 2 to 0 in SEMRA_0). For details, see section 13.3.9, Serial Extended Mode Register (SEMR) (Only for channel 0 in H8S/2215).
6 to 4	—	Undefined	—	Reserved The write value should always be 0.
3	TIOCA2E	1	R/W	TIOCA2 Output Enable Controls the TIOCA2 output on the P16 pin. When the TIOCA2 in TPU is output to generate the transfer clock, P16 is used as other function pin by setting this bit to 0. 0: Disables output of TIOCA2 in TPU 1: Enables output of TIOCA2 in TPU
2	TIOCA1E	1	R/W	TIOCA1 Output Enable Controls the TIOCA1 output on the P14 pin. When the TIOCA1 in TPU is output to generate the transfer clock, P14 is used as other function pin by setting this bit to 0. 0: Disables output of TIOCA1 in TPU 1: Enables output TIOCA1 in TPU
1	TIOCC0E	1	R/W	TIOCC0 Output Enable Controls the TIOCC0 output on the P12 pin. When the TIOCC0 in TPU is output to generate the transfer clock, P12 is used as other function pin by setting this bit to 0. 0: Disables output of TIOCC0 in TPU 1: Enables output of TIOCC0 in TPU
0	TIOCA0E	1	R/W	TIOCA0 Output Enable Controls the TIOCA0 output on the P10 pin. When the TIOCA0 in TPU is output to generate the transfer clock, P10 is used as other function pin by setting this bit to 0. 0: Disables output of TIOCA0 in TPU 1: Enables output of TIOCA0 in TPU

Bit	Bit Name	Initial Value	R/W	Description
1	UIFRST	1	R/W	USB Interface Software Reset Controls USB module internal reset. When the UIFRST bit is set to 1, the USB internal modules other than UCTLR, UIER3, and the CK48 READY bit of UIFR3 are all reset. At initialization, the UIFRST bit must be cleared to 0 after the USB operating clock stabilization time has passed following USB module stop mode cancellation. 0: Sets the USB internal modules to the operating state (at initialization, this bit must be cleared after the USB operating clock stabilization time has passed). 1: Sets the USB internal modules other than UCTLR, UIER3, and the CK48 READY bit of UIFR3 reset state. If after being cleared to 0 the UIFIRST bit is again set to 1, the UDCRST bit must also be set to 1 at the same time.
0	UDCRST	1	R/W	UDC Core Software Reset Controls reset of the UDC core in the USB module. When the UDCRST bit is set to 1, the UDC core is reset and USB bus synchronization operation stops. At initialization, UDCRST must be cleared to 0 after D+ pull-up following UIFRST clearing to 0. In the suspend state, to maintain the internal state of the UDC core, enter software standby mode after setting USB module stop mode with the UDCRST bit to be maintained. After VBUS disconnection detection, UDCRST must be set to 1. 0: Sets the UDC core in the USB module to operating state (at initialization, UDCRST must be cleared after D+ pull-up following UIFRST clearing to 0). 1: Sets the UDC core in the USB module to reset state (in the suspend state, UDCRST must not be set to 1; after VBUS disconnection detection, UDCRST must be set to 1).

15.3.5 USB Trigger Register 0 (UTRG0)

UTRG0 generates one-shot triggers to the FIFO for each endpoint EP0 to EP2. For information on accessing this register, see 2.9.4, Accessing Registers Containing Write-Only Bits.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
5	EP2oRDFN	0	W	EP2o Read Completion 0: Performs no operation 1: Writes 1 to this bit after reading data for EP2o OUT FIFO. EP2o FIFO has a dual FIFO configuration. This trigger is generated to the currently effective FIFO.
4	EP2iPKTE	0	W	EP2i Packet Enable 0: Performs no operation 1: Generates a trigger to enable data transfer to the EP2i IN FIFO. EP2i FIFO has a dual FIFO configuration. This trigger is generated for the currently effective FIFO.
3	EP1iPKTE	0	W	EP1i Packet Enable 0: Performs no operation 1: Generates a trigger to enable data transfer to the EP1i IN FIFO.
2	EP0oRDFN	0	W	EP0o Read Completion 0: Performs no operation 1: Writes 1 to this bit after reading data for EP0o OUT FIFO. This trigger enables the next packet to be received.
1	EP0iPKTE	0	W	EP0i Packet Enable 0: Performs no operation 1: Generates a trigger to enable data transfer to the EP0i IN FIFO.

Bit	Bit Name	Initial Value	R/W	Description
0	EP0sRDFN	0	W	EP0s Read Completion 0: Performs no operation. A NAK handshake is returned in response to transmit/receive requests from the host in the data stage until 1 is written to this bit. 1: Writes 1 to this bit after reading data for EP0s OUT FIFO. After receiving the setup command, this trigger enables the next packet to be received by the EP0i and EP0o in the data stage. EP0s can always be overwritten and receive data regardless of this trigger.

Note: As triggers to EP3i and EP3o for Isochronous transfer are automatically generated each time the SOF packet is received from the host, the user need not generate triggers to EP3i and EP3o. Accordingly, data write to UEDR3i and data read from UEDR3o must be completed before the next packet has been received.

15.3.6 USB Trigger Register 1 (UTRG1)

UTRG1 generates one-shot triggers to the FIFO for each endpoint EP4 and EP5. For information on accessing this register, see 2.9.4, Accessing Registers Containing Write-Only Bits.

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
2	EP5iPKTE	0	W	EP5i Packet Enable 0: Performs no operation 1: Generates a trigger to enable data transfer to the EP5i IN FIFO.
1	EP4oRDFN	0	W	EP4o Read Completion 0: Performs no operation 1: Writes 1 to this bit after reading data for EP4o OUT FIFO. EP4o FIFO has a dual FIFO configuration. This trigger is generated to the currently effective FIFO.
0	EP4iPKTE	0	W	EP4i Packet Enable 0: Performs no operation 1: Generates a trigger to enable data transfer to the EP4i IN FIFO. EP4i FIFO has a dual FIFO configuration. This trigger is generated for the currently effective FIFO.

15.3.21 USB Endpoint Data Register 5i (UEDR5i)

UEDR5i is a data register for endpoint 5i (for Interrupt_in transfer). UEDR5i stores data to be sent to the host. The number of data items to be written continuously must be the maximum packet size or less.

UEDR5i is a byte register to which 4-byte address area is assigned. Accordingly, UEDR5i allows the user to write 2-byte or 4-byte data by word transfer or longword transfer. For information on accessing this register, see 2.9.4, Accessing Registers Containing Write-Only Bits.

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	D7 to D0	All 0	W	These bits store data for Interrupt_in transfer

15.3.22 USB Endpoint Receive Data Size Register 0o (UESZ0o)

UESZ0o is the receive data size register for endpoint 0o (for Control_out transfer). UESZ0o indicates the number of bytes of data to be received from the host.

Note that UESZ0o is decremented by 1 every time when 1 byte is read from UEDR0o.

Bit	Bit Name	Initial Value	R/W	Description
7	—	—	R	Reserved
6 to 0	D6 to D0	—	R	These bits indicate the size of data to be received in Control_out transfer

15.3.23 USB Endpoint Receive Data Size Register 2o (UESZ2o)

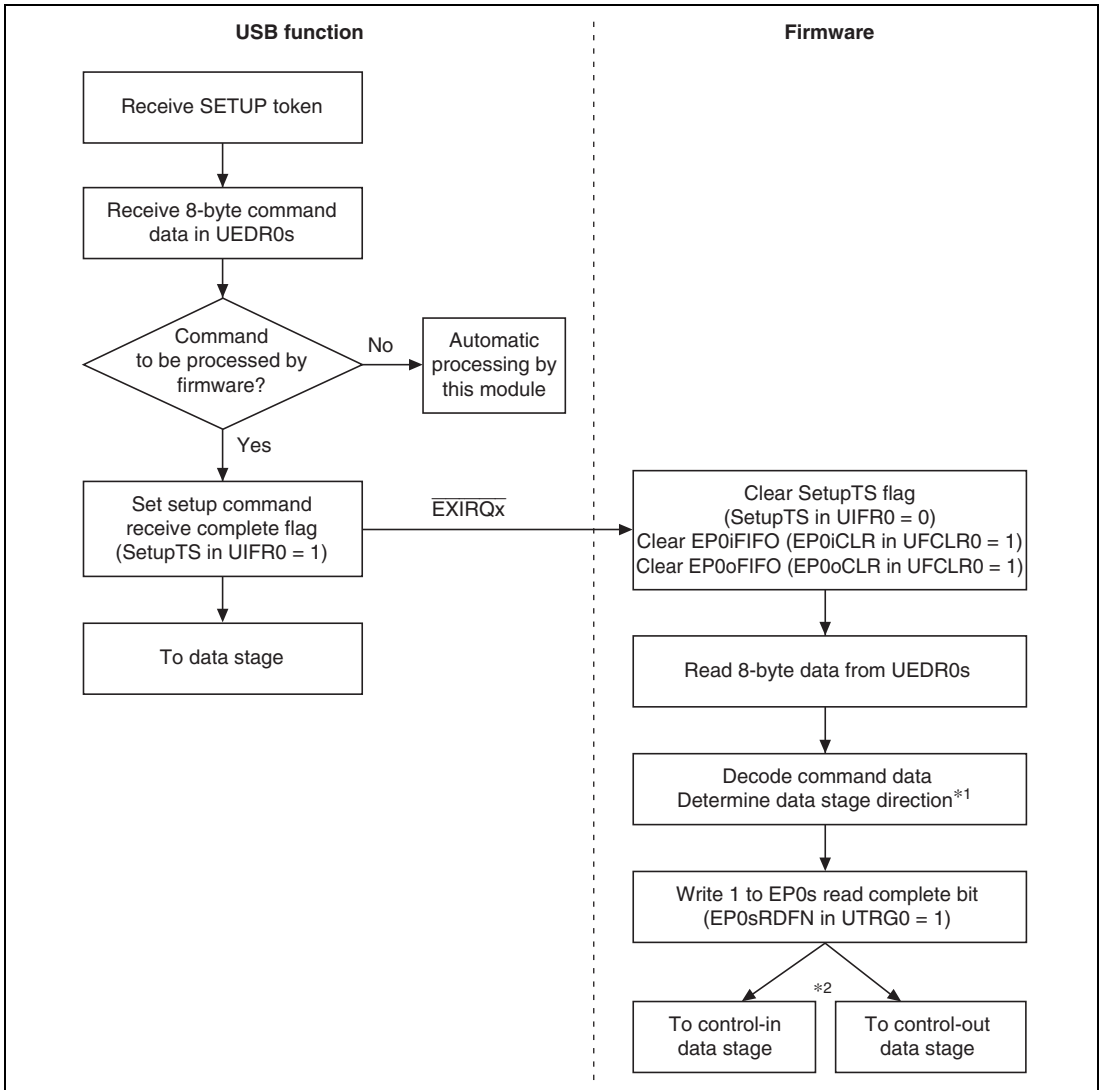
UESZ2o is the receive data size register for endpoint 2o (for Bulk_out transfer). UESZ2o indicates the number of bytes of data to be received from the host.

Note that UESZ2o is decremented by 1 every time when 1 byte is read from UEDR2o.

The FIFO for endpoint 2o (for Bulk_out transfer) has a dual-FIFO configuration. The data size indicated by this register refers to the currently selected FIFO.

Bit	Bit Name	Initial Value	R/W	Description
7	—	—	R	Reserved
6 to 0	D6 to D0	—	R	These bits indicate the size of data to be received in Bulk_out transfer

(1) Setup Stage



Notes: 1. In the setup stage, the firmware first analyzes the command data sent from the host required to be processed by the firmware, and determines subsequent processing. (For example, the data stage direction.)
2. When the transfer direction must be enabled here. When the transfer direction is control-in, an EP0i transfer request interrupt is not required and must be disabled.

Figure 15.13 Setup Stage Operation

Table 15.8 Bit Name Modification List

Abbreviation	R/W	Initial Value	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UDMAR	R/W	H'00	H'C00082	EP6T1	EP6T0	EP5T1	EP5T0	EP1T1	EP1T0	EP2T1	EP2T0
UTRG0	W	H'00	H'C00084	—	—	EP1RDFN	EP2PKTE	EP3PKTE	EP0o RDFN	EP0iPKTE	EP0s RDFN
UTRG1	W	H'00	H'C00085	—	—	—	—	—	EP4PKTE	EP6RDFN	EP5PKTE
UFCLR0	W	H'00	H'C00086	(EPnCLR)	(EPnCLR)	EP1CLR	EP2CLR	EP3CLR	EP0oCLR	EP0iCLR	—
UFCLR1	W	H'00	H'C00087	—	—	—	—	—	EP4CLR	EP6CLR	EP5CLR
UESTL0	R/W	H'00	H'C00088	(EPnSTL)	(EPnSTL)	EP1STL	EP2STL	EP3STL	—	—	EP0STL
UESTL1	R/W	H'00	H'C00089	SCME	—	—	—	—	EP4STL	EP6STL	EP5STL
UIFR0	R/W	H'00	H'C000C0	BRST	—	EP3TR	EP3TS	EP0oTS	EP0iTR	EP0iTS	SetupTS
UIFR1	R/W	H'01*1 or H'09	H'C000C1	(EPnTF)	(EPnTS)	(EPnTF)	(EPnTR)	*2 EP2ALL EMPTY	EP1 READY	EP2TR	EP2 EMPTY
UIFR2	R/W	H'01*1 or H'09	H'C000C2	—	—	EP4TR	EP4TS	*2 EP5ALL EMPTY	EP6 READY	EP5TR	EP5 EMPTY
UIER0	R/W	H'00	H'C000C4	BRSTE	—	EP3TRE	EP3TSE	EP0oTSE	EP0iTRE	EP0iTSE	SetupTSE
UIER1	R/W	H'00	H'C000C5	(EPnTFE)	(EPnTSE)	(EPnTFE)	(EPnTRE)	*2 EP2ALL EMPTYE	EP1 READYE	EP2TRE	EP2 EMPTYE
UIER2	R/W	H'00	H'C000C6	—	—	EP4TRE	EP4TSE	*2 EP5ALL EMPTYE	EP6 READYE	EP5TRE	EP5 EMPTYE
UISR0	R/W	H'00	H'C000C8	BRSTS	—	EP3TRS	EP3TSS	EP0oTSS	EP0iTRS	EP0iTSS	SetupTSS
UISR1	R/W	H'00	H'C000C9	(EPnTFS)	(EPnTSS)	(EPnTFS)	(EPnTRS)	*2 EP2ALL EMPTYS	EP1 READYS	EP2TRS	EP2 EMPTYS
UISR2	R/W	H'00	H'C000CA	—	—	EP4TRS	EP4TSS	*2 EP5ALL EMPTYS	EP6 READYS	EP5TRS	EP5 EMPTYS
UDSR	R	H'00	H'C000CC	—	—	EP4DE	EP5DE	—	EP2DE	EP3DE	EP0iDE

Notes: 1. H'01 in H8S/2215. H'09 in H8S/2215R, H8S/2215T and H8S/2215C.
2. Available only in H8S/2215R, H8S/2215T and H8S/2215C. "—" in H8S/2215.

Table 15.9 shows the EPINFO data for the endpoint configuration shown in figure 15.27.

This USB module is optimized by the hardware specific to the transfer type. Accordingly, endpoints cannot be configured completely freely. Endpoint configuration can be modified within the restriction as shown in table 15.9 (data indicated within parentheses [ ]), data other than that within parentheses [ ] must be specified the value shown in table 15.9. For unused endpoints, dummy data (0) must be written.

17.5 Usage Note

17.5.1 Module Stop Mode Setting

Operation of the D/A converter can be disabled or enabled using the module stop control register. The initial setting is for operation of the D/A converter to be halted. Register access is enabled by clearing module stop mode. For details, refer to section 22, Power-Down Modes.

19.14 Note on Switching from F-ZTAT Version to Masked ROM Version

The masked ROM version does not have the internal registers for flash memory control that are provided in the F-ZTAT version. Table 19.7 lists the registers that are present in the F-ZTAT version but not in the masked ROM version. If a register listed in table 19.7 is read in the masked ROM version, an undefined value will be returned. Therefore, if application software developed on the F-ZTAT version is switched to a masked ROM version product, it must be modified to ensure that the registers in table 19.9 have no effect.

Table 19.9 Registers Present in F-ZTAT Version but Absent in Masked ROM Version

Register	Abbreviation	Address
Flash memory control register 1	FLMCR1	H'FFA8
Flash memory control register 2	FLMCR2	H'FFA9
Erase block register 1	EBR1	H'FFAA
Erase block register 2	EBR2	H'FFAB
RAM emulation register	RAMER	H'FEDB
Serial control register x	SCRX	H'FDB4

21.1.2 Low-Power Control Register (LPWRCR)

LPWRCR selects whether the oscillator's built-in feedback resistor and duty adjustment circuit are used with external clock input.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	R/W	Reserved These bits can be read from or written to, but the write value should always be 0.
3	RFCUT	0	R/W	Built-in Feedback Resistor Control Selects whether the oscillator's built-in feedback resistor and duty adjustment circuit are used with external clock input. This bit should not be accessed when a crystal oscillator is used. After this bit is set when using external clock input, a transition should initially be made to software standby mode. Switching between use and non-use of the oscillator's built-in feedback resistor and duty adjustment circuit is performed when the transition is made to software standby mode. 0: System clock oscillator's built-in feedback resistor and duty adjustment circuit are used 1: System clock oscillator's built-in feedback resistor and duty adjustment circuit are not used
2	—	0	R/W	Reserved This bit can be read from or written to, but the write value should always be 0.
1	STC1	0	R/W	Frequency Multiplication Factor
0	STC0	0	R/W	Specify the frequency multiplication factor of the PLL circuit incorporated into the evaluation chip. The specified frequency multiplication factor is valid after a transition to software standby mode, watch mode, or subactive mode. With this LSI, STC1 and STC0 must both be set to 1. After a reset, STC1 and STC0 are both cleared to 0, and so must be set to 1. 00: × 1 01: × 2 (Setting prohibited) 10: × 4 (Setting prohibited) 11: PLL is bypassed

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Current dissipation*2	All modules stopped	I_{CC}*3	—	15 (V_{CC} = 3.3 V)	—	mA	f = 16 MHz (reference value)
			—	21 (V_{CC} = 3.3 V)	—	mA	f = 24 MHz (reference value)
	Standby mode*4		—	1.0	10	µA	$T_a \leq 50°C$
			—	—	50	µA	$50°C < T_a$
Analog power supply current	During A/D conversion	AI_{CC}	—	0.3	1.5	mA	AV_{CC} = 3.3 V
	Idle		—	0.01	5.0	µA	
Reference power supply current	During A/D conversion	AI_{CC}	—	1.2	2.5	mA	V_{ref} = 3.3 V
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. If the A/D or D/A converter is not used, the AVCC, V_{ref}, and AVSS pins should not be open. Even if the A/D or D/A converter is not used, connect the AVCC and V_{ref} pins to V_{CC} and the AVSS pin to V_{SS}, respectively. In this case, the V_{ref} level should be the AVCC level or less.

2. Current dissipation values are for V_{IH} (min.) = V_{CC} – 0.2 V and V_{IL} (max.) = 0.2 V, with all output pins unloaded and the on-chip MOS pull-up transistors in the off state.

3. I_{CC} depends on V_{CC} and f as follows:

   I_{CC} (max.) = 1.0 (mA) + 0.67 (mA/(MHz x V)) × V_{CC} × f (normal operation, USB halted)

   I_{CC} (max.) = 1.0 (mA) + 0.85 (mA/(MHz x V)) × V_{CC} × f (normal operation, USB operating, f = 16 MHz : PLL 3 × multiplication)

   I_{CC} (max.) = 1.0 (mA) + 0.72 (mA/(MHz x V)) × V_{CC} × f (normal operation, USB operating, f = 24 MHz : PLL 2 × multiplication)

   I_{CC} (max.) = 1.0 (mA) + 0.55 (mA/(MHz x V)) × V_{CC} × f (sleep mode)

4. The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, V_{IH} (min.) = V_{CC} × 0.9, and V_{IL} (max.) = 0.3 V.

5. The FWE pin is effective only in the F-ZTAT version.

6. When $V_{CC} < AV_{CC}$, the maximum value for P40 and P41 is V_{CC} + 0.3 V.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Current dissipation*2	All modules stopped	I_{CC}*3	—	15 (V_{CC} = 3.3 V)	—	mA	f = 16 MHz (reference value)
			—	21 (V_{CC} = 3.3 V)	—	mA	f = 24 MHz (reference value)
	Standby mode*4		—	1.0	10	µA	$T_a \leq 50°C$
			—	—	50	µA	$50°C < T_a$
Analog power supply current	During A/D conversion	AI_{CC}	—	0.3	1.5	mA	AV_{CC} = 3.3 V
	Idle		—	0.01	5.0	µA	
Reference power supply current	During A/D conversion	AI_{CC}	—	1.2	2.5	mA	V_{ref} = 3.3 V
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes:
1. If the A/D or D/A converter is not used, the AVCC, V_{ref}, and AVSS pins should not be open. Even if the A/D or D/A converter is not used, connect the AVCC and V_{ref} pins to V_{CC} and the AVSS pin to V_{SS}, respectively. In this case, the V_{ref} level should be the AVCC level or less.
2. Current dissipation values are for V_{IH} (min.) = V_{CC} – 0.2 V and V_{IL} (max.) = 0.2 V, with all output pins unloaded and the on-chip MOS pull-up transistors in the off state.
3. I_{CC} depends on V_{CC} and f as follows:
   I_{CC} (max.) = 1.0 (mA) + 0.67 (mA/(MHz x V)) × V_{CC} × f (normal operation, USB halted)
   I_{CC} (max.) = 1.0 (mA) + 0.85 (mA/(MHz x V)) × V_{CC} × f (normal operation, USB operating, f = 16 MHz : PLL 3 × multiplication)
   I_{CC} (max.) = 1.0 (mA) + 0.72 (mA/(MHz x V)) × V_{CC} × f (normal operation, USB operating, f = 24 MHz : PLL 2 × multiplication)
   I_{CC} (max.) = 1.0 (mA) + 0.55 (mA/(MHz x V)) × V_{CC} × f (sleep mode)
4. The values are for $V_{RAM} \leq V_{CC} < 3.0$ V, V_{IH} (min.) = V_{CC} × 0.9, and V_{IL} (max.) = 0.3 V.
5. The FWE pin is supported on the F-ZTAT version only.
6. When $V_{CC} < AV_{CC}$, the maximum value for P40 and P41 is V_{CC} + 0.3 V.

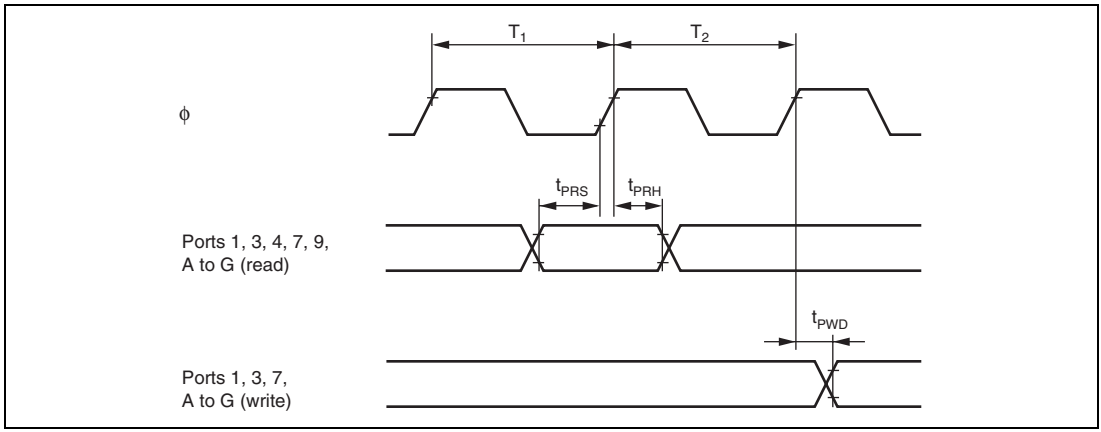


Figure 27.12 I/O Port Input/Output Timing

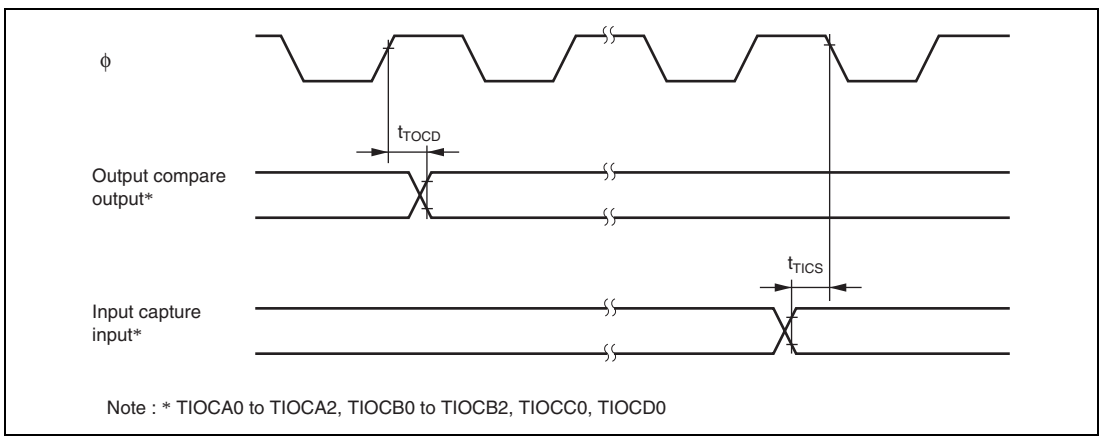


Figure 27.13 TPU Input/Output Timing

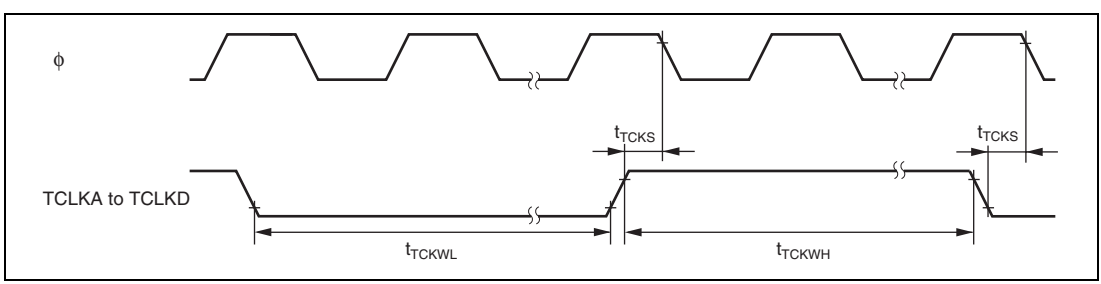


Figure 27.14 TPU Clock Input Timing