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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	24MHz
Connectivity	SCI, SmartCard, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	68
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2215rte24v

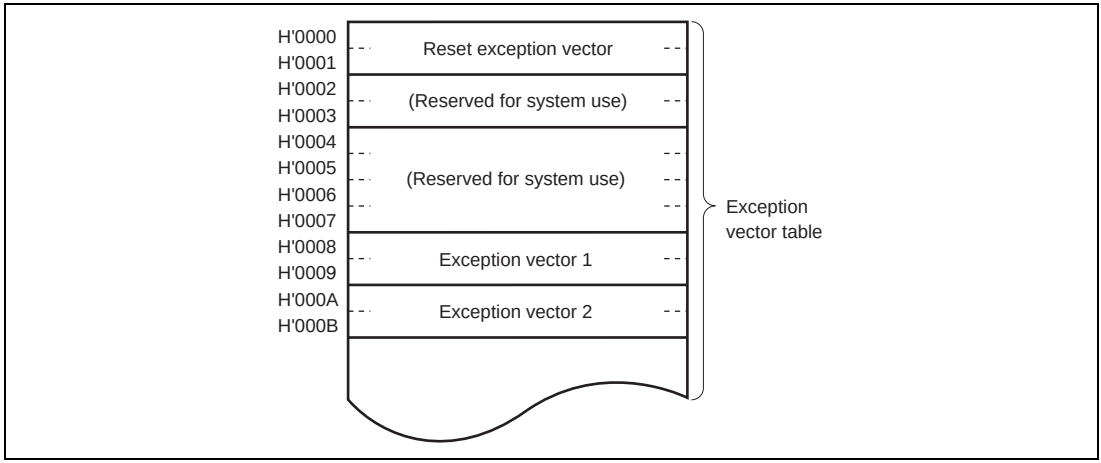
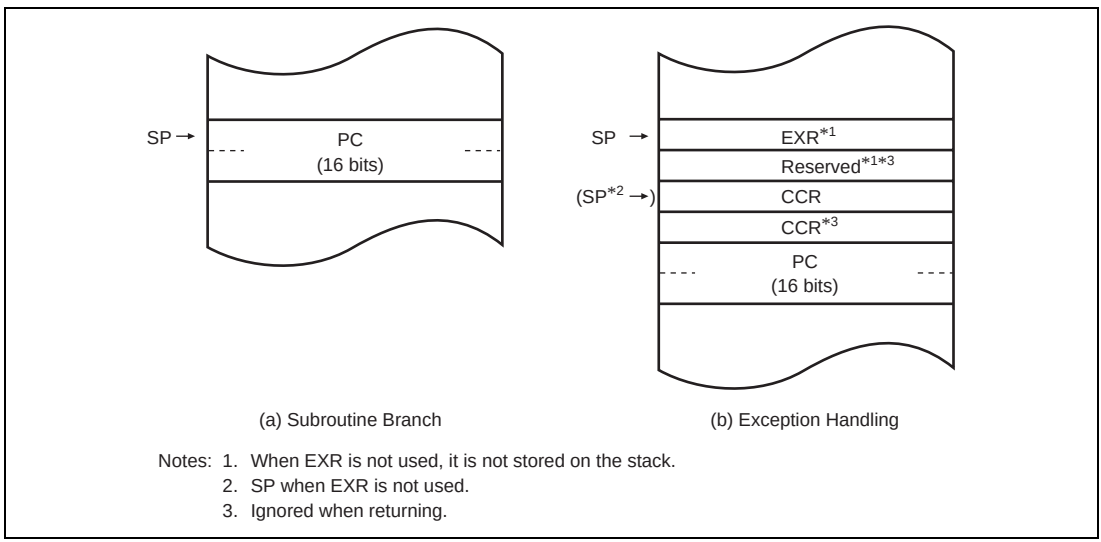


Figure 2.1 Exception Vector Table (Normal Mode)



Notes: 1. When EXR is not used, it is not stored on the stack.
2. SP when EXR is not used.
3. Ignored when returning.

Figure 2.2 Stack Structure in Normal Mode

6.6.4 Wait Control

When accessing external space, this LSI can extend the bus cycle by inserting one or more wait states (T_w). There are two ways of inserting wait states: program wait insertion and pin wait insertion using the $\overline{\text{WAIT}}$ pin.

Program Wait Insertion: From 0 to 3 wait states can be inserted automatically between the T_2 state and T_3 state on an individual area basis in 3-state access space, according to the settings of WCRH and WCRL.

Pin Wait Insertion: Setting the WAITE bit in BCRL to 1 enables wait insertion by means of the $\overline{\text{WAIT}}$ pin. When external space is accessed in this state, program wait insertion is first carried out according to the settings in WCRH and WCRL. Then, if the $\overline{\text{WAIT}}$ pin is low at the falling edge of ϕ in the last T_2 or T_w state, a T_W state is inserted. If the $\overline{\text{WAIT}}$ pin is held low, T_w states are inserted until it goes high.

7.4.3 Idle Mode

Idle mode can be specified by setting the RPE bit and DTIE bit in DMACR to 1. In idle mode, one byte or word is transferred in response to a single transfer request, and this is executed the number of times specified in ETCR. One address is specified by MAR, and the other by IOAR. The transfer direction can be specified by the DTDIR bit in DMACR. Table 7.4 summarizes register functions in idle mode.

Table 7.4 Register Functions in Idle Mode

	Function			
Register	**DTDIR = 0**	**DTDIR = 1**	**Initial Setting**	**Operation**
23 0 MAR	Source address register	Destination address register	Start address of transfer destination or transfer source	Fixed
23 15 0 H'FF IOAR	Destination address register	Source address register	Start address of transfer source or transfer destination	Fixed
15 0 ETCR	Transfer counter		Number of transfers	Decremented every transfer, transfer ends when count reaches H'0000

MAR specifies the start address of the transfer source or transfer destination as 24 bits. MAR is neither incremented nor decremented each time a byte or word is transferred. IOAR specifies the lower 16 bits of the other address. The 8 bits above IOAR have a value of H'FF. Figure 7.5 illustrates operation in idle mode.

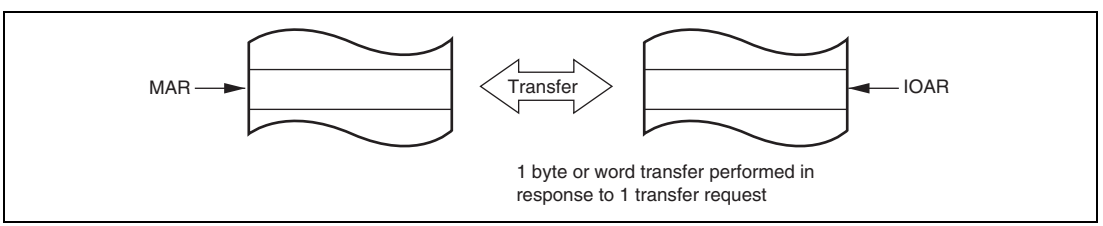


Figure 7.5 Operation in Idle Mode

The number of transfers is specified as 16 bits in ETCR. ETCR is decremented by 1 each time a transfer is executed, and when its value reaches H'0000, the DTE bit is cleared and transfer ends. If the DTIE bit is set to 1 at this time, an interrupt request is sent to the CPU or DTC. The maximum number of transfers, when H'0000 is set in ETCR, is 65,536.

4. Write 1 to the SWDTE bit and the vector number (H'60) to DTVECR. The write data is H'E0.
5. Read DTVECR again and check that it is set to the vector number (H'60). If it is not, this indicates that the write failed. This is presumably because an interrupt occurred between steps 3 and 4 and led to a different software activation. To activate this transfer, go back to step 3.
6. If the write was successful, the DTC is activated and a block of 128 bytes of data is transferred.
7. After the transfer, an SWDTEND interrupt occurs. The interrupt handling routine should clear the SWDTE bit to 0 and perform other wrap-up processing.

8.8 Usage Notes

8.8.1 Module Stop

DTC operation can be prohibited or enabled using the module stop control register. Access to the register is prohibited in the module stop mode. However, the module stop mode cannot be specified while the DTC is operating. For details, see section 22, Power-Down Modes.

8.8.2 On-Chip RAM

The MRA, MRB, SAR, DAR, CRA, and CRB registers are all located in on-chip RAM. When the DTC is used, the RAME bit in SYSCR must not be cleared to 0.

8.8.3 DTCE Bit Setting

For DTCE bit setting, use bit manipulation instructions such as BSET and BCLR. If all interrupts are masked, multiple activation sources can be set at one time (only at the initial setting) by writing data after executing a dummy read on the relevant register.

8.8.4 DMAC Transfer End Interrupt

When DTC transfer is activated by a DMAC transfer end interrupt, the DMAC's DTE bit is not subject to DTC control, regardless of the transfer counter and DISEL bit, and the write data has priority. Consequently, an interrupt request is not sent to the CPU when the DTC transfer counter reaches 0.

Table 9.60 PE1 Pin Function

Operating Mode	Modes 4 to 6			Mode 7	
Bus Mode	8-bit bus mode		16-bit bus mode	—	
PE1DDR	0	1	—	0	1
Pin Function	PE1 input	PE1 output	D1 input/output	PE1 input	PE1 output

Table 9.61 PE0 Pin Function

Operating Mode	Modes 4 to 6			Mode 7	
Bus Mode	8-bit bus mode		16-bit bus mode	—	
PE0DDR	0	1	—	0	1
Pin Function	PE0 input	PE0 output	D0 input/output	PE0 input	PE0 output

10.2 Input/Output Pins

Table 10.2 Pin Configuration

Channel	Symbol	I/O	Function
All	TCLKA	Input	External clock A input pin (Channel 1 phase counting mode A phase input)
	TCLKB	Input	External clock B input pin (Channel 1 phase counting mode B phase input)
	TCLKC	Input	External clock C input pin (Channel 2 phase counting mode A phase input)
	TCLKD	Input	External clock D input pin (Channel 2 phase counting mode B phase input)
0	TIOCA0	I/O	TGRA_0 input capture input/output compare output/PWM output pin
	TIOCB0	I/O	TGRB_0 input capture input/output compare output/PWM output pin
	TIOCC0	I/O	TGRC_0 input capture input/output compare output/PWM output pin
	TIOCD0	I/O	TGRD_0 input capture input/output compare output/PWM output pin
1	TIOCA1	I/O	TGRA_1 input capture input/output compare output/PWM output pin
	TIOCB1	I/O	TGRB_1 input capture input/output compare output/PWM output pin
2	TIOCA2	I/O	TGRA_2 input capture input/output compare output/PWM output pin
	TIOCB2	I/O	TGRB_2 input capture input/output compare output/PWM output pin

Table 10.7 TPSC2 to TPSC0 (channel 2)

	Bit 2	Bit 1	Bit 0	
Channel	**TPSC2**	**TPSC1**	**TPSC0**	**Description**
2	0	0	0	Internal clock: counts on ϕ/1
			1	Internal clock: counts on ϕ/4
		1	0	Internal clock: counts on ϕ/16
			1	Internal clock: counts on ϕ/64
	1	0	0	External clock: counts on TCLKA pin input
			1	External clock: counts on TCLKB pin input
		1	0	External clock: counts on TCLKC pin input
			1	Internal clock: counts on ϕ/1024

Note: This setting is ignored when channel 1 is in phase counting mode.

Bit	Bit Name	Initial value	R/W	Description
1	TGIEB	0	R/W	TGR Interrupt Enable B Enables or disables interrupt requests (TGIB) by the TGFB bit when the TGFB bit in TSR is set to 1. 0: Interrupt requests (TGIB) by TGFB disabled 1: Interrupt requests (TGIB) by TGFB enabled
0	TGIEA	0	R/W	TGR Interrupt Enable A Enables or disables interrupt requests (TGIA) by the TGFA bit when the TGFA bit in TSR is set to 1. 0: Interrupt requests (TGIA) by TGFA disabled 1: Interrupt requests (TGIA) by TGFA enabled

Buffer Operation Timing: Figures 10.36 and 10.37 show the timing in buffer operation.

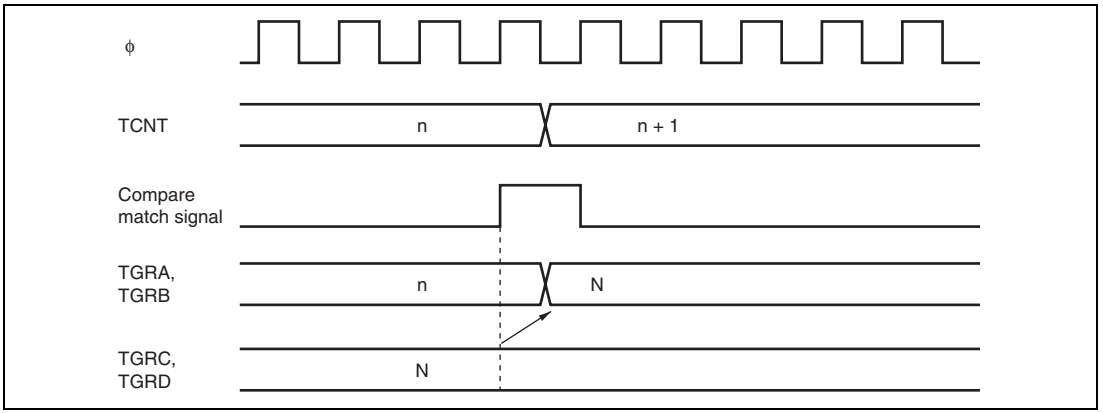


Figure 10.36 Buffer Operation Timing (Compare Match)

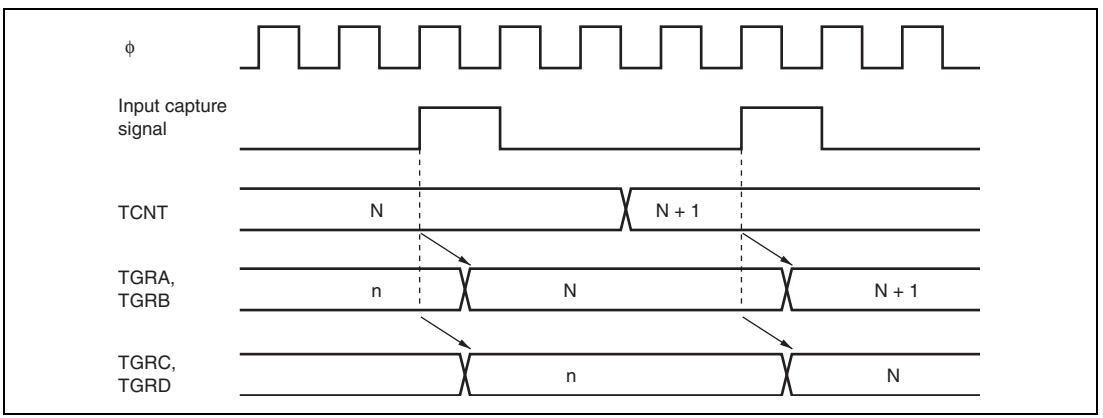


Figure 10.37 Buffer Operation Timing (Input Capture)

11.3.4 Time Control Registers (TCR)

The TCR registers select the clock source and the time at which TCNT is cleared, and enable interrupts.

Bit	Bit Name	Initial Value	R/W	Description
7	CMIEB	0	R/W	Compare Match Interrupt Enable B Selects whether CMFB interrupt requests (CMIB) are enabled or disabled when the CMFB flag in TCSR is set to 1. 0: CMFB interrupt requests (CMIB) are disabled 1: CMFB interrupt requests (CMIB) are enabled
6	CMIEA	0	R/W	Compare Match Interrupt Enable A Selects whether CMFA interrupt requests (CMIA) are enabled or disabled when the CMFA flag in TCSR is set to 1. 0: CMFA interrupt requests (CMIA) are disabled 1: CMFA interrupt requests (CMIA) are enabled
5	OVIE	0	R/W	Timer Overflow Interrupt Enable Selects whether OVF interrupt requests (OVI) are enabled or disabled when the OVF flag in TCSR is set to 1. 0: OVF interrupt requests (OVI) are disabled 1: OVF interrupt requests (OVI) are enabled
4 3	CCLR1 CCLR0	0 0	R/W R/W	Counter Clear 1 and 0 These bits select the method by which TCNT is cleared. 00: Clear is disabled 01: Clear by compare match A 10: Clear by compare match B 11: Clear by rising edge of external reset input
2 1 0	CKS2 CKS1 CKS0	0 0 0	R/W R/W R/W	Clock Select 2 to 0 These bits select the clock input to TCNT and count condition. See table 11.2.

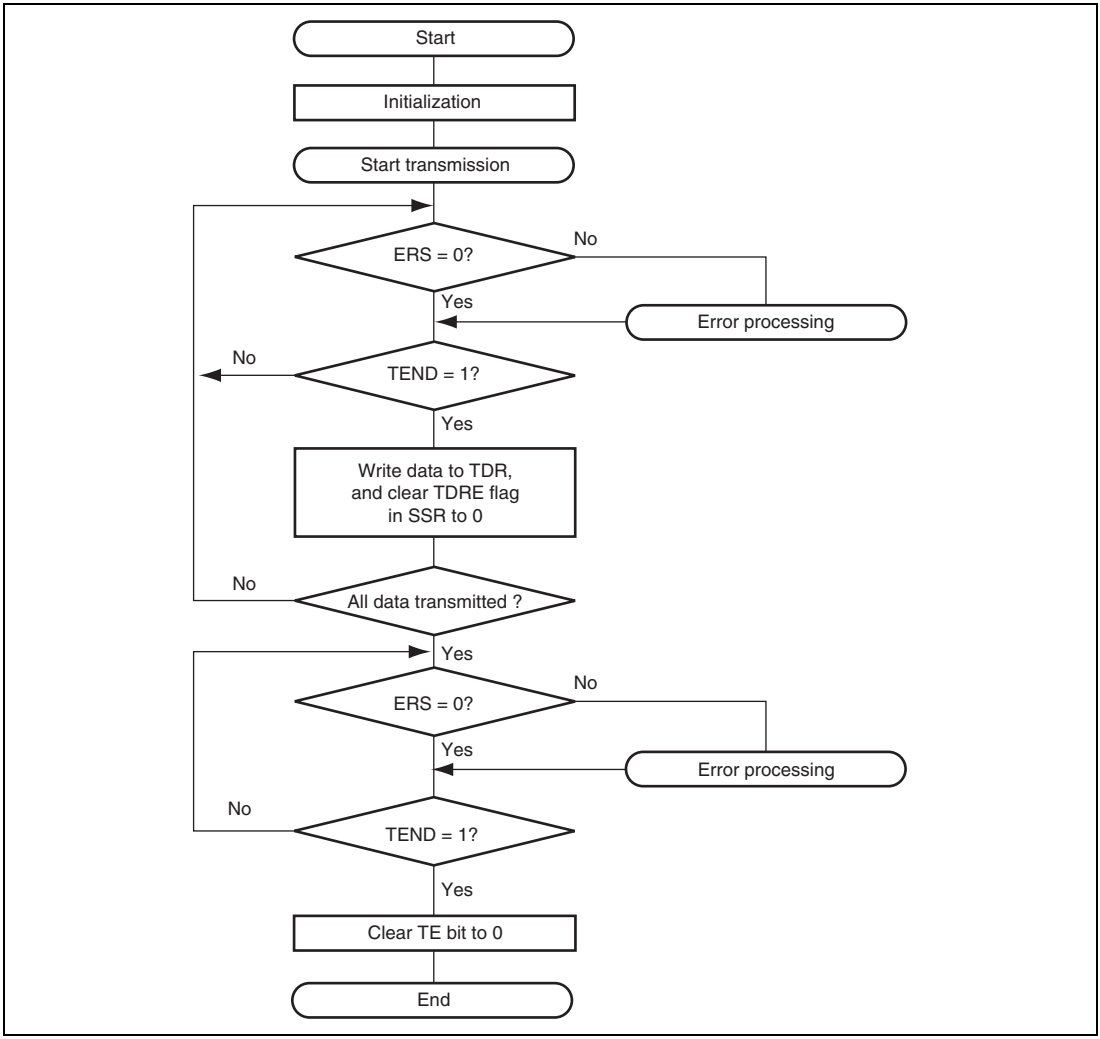


Figure 13.32 Example of Transmission Processing Flow

Bit	Bit Name	Initial Value	R/W	Description
7	BRST	0	R/(W)*	Bus Reset Set to 1 when the bus reset signal is detected on the USB bus. The corresponding interrupt output is $\overline{\text{EXIRQ0}}$ or $\overline{\text{EXIRQ1}}$. Note that BRST is also set to 1if D+ is not pulled-up during USB cable connection.
6	—	0	R	Reserved This bit is always read as 0 and cannot be modified.
5	EP1iTR	0	R/(W)*	EP1i Transfer Request Set to 1 if there is no valid transmit data in the FIFO when an IN token is sent from the host to EP1i. The corresponding interrupt output is $\overline{\text{EXIRQ0}}$ or $\overline{\text{EXIRQ1}}$.
4	EP1iTS	0	R/(W)*	EP1i Transfer Complete Set to 1 if the transmit data written in EP1i is transferred to the host normally and the ACK handshake is returned. The corresponding interrupt output is $\overline{\text{EXIRQ0}}$ or $\overline{\text{EXIRQ1}}$.
3	EP0oTS	0	R/(W)*	EP0o Receive Complete Set to 1 if the EP0o receives data from the host normally and returns the ACK handshake to the host. The corresponding interrupt output is $\overline{\text{EXIRQ0}}$ or $\overline{\text{EXIRQ1}}$.
2	EP0iTR	0	R/(W)*	EP0i Transmit Request Set to 1 if there is no valid transmit data in the FIFO when an IN token is sent from the host to EP0i. The corresponding interrupt output is $\overline{\text{EXIRQ0}}$ or $\overline{\text{EXIRQ1}}$.
1	EP0iTS	0	R/(W)*	EP0i Transmit Complete Set to 1 if the transmit data written in EP0i is transferred to the host normally and the ACK handshake is returned. The corresponding interrupt output is $\overline{\text{EXIRQ0}}$ or $\overline{\text{EXIRQ1}}$.
0	SetupTS	0	R/(W)*	Setup Command Receive Complete Set to 1 if the EP0s normally receives 8-byte data to be decoded by the function from the host and returns the ACK handshake to the host. The corresponding interrupt output is $\overline{\text{EXIRQ0}}$ or $\overline{\text{EXIRQ1}}$.

Note: * The write value should always be 0 to clear this flag.

Bit	Bit Name	Initial Value	R/W	Description
3	SPRSs	0	R	Suspend/Resume Status Indicates the suspend/resume status and cannot request an interrupt. 0: Indicates that the bus is in the normal state. 1: Indicates that the bus is in the suspend state.
2	SPRSi	0	R/(W)*	Suspend/Resume Interrupt Set to 1 if a transition from normal state to suspend state or suspend state to normal state has occurred. The corresponding interrupt output is $\overline{\text{IRQ6}}$. This bit can be used to cancel software standby state at resume.
1	VBUSs	0	R	VBUS Status Indicates the VBUS state by the USB cable connection and disconnection. An interrupt cannot be requested by the VBUSs. 0: Indicates that the VBUS (USB cable) bus is disconnected. 1: Indicates that the VBUS (USB cable) bus is connected.
0	VBUSi	0	R/(W)*	VBUS Interrupt Set to 1 if a VBUS state changes by USB cable connection or disconnection. The corresponding interrupt output is $\overline{\text{EXIRQ0}}$ or $\overline{\text{EXIRQ1}}$.

Note: * The write value should always be 0 to clear this flag.

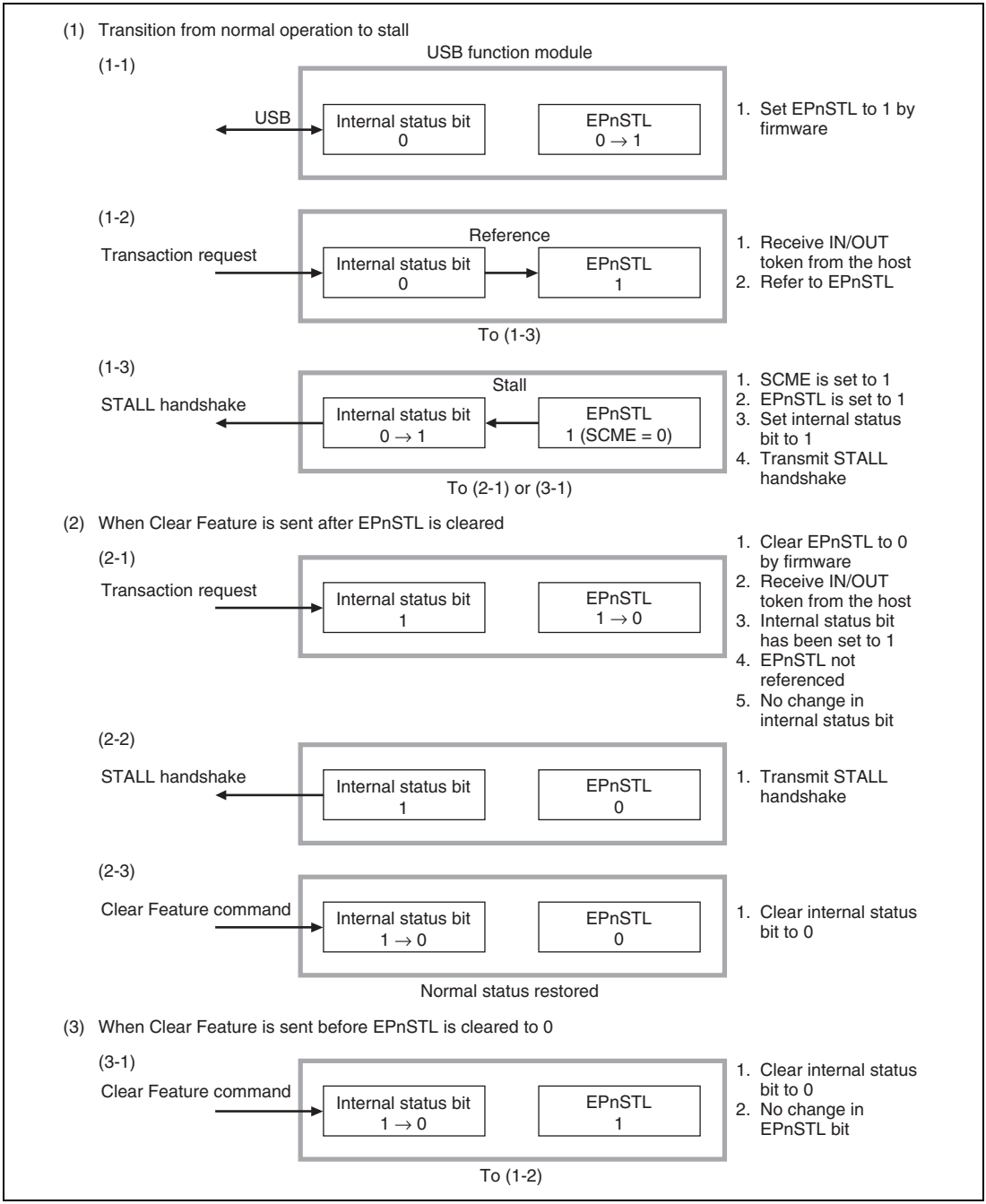
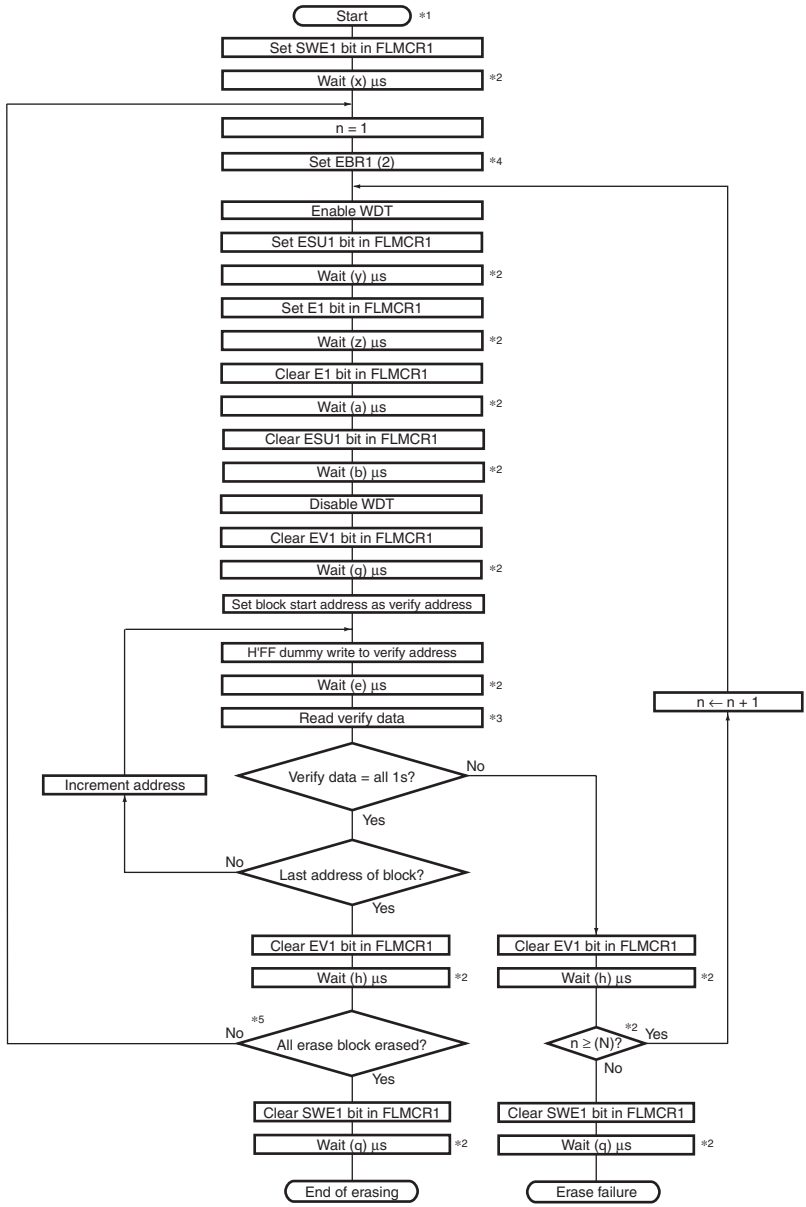


Figure 15.23 Forcible Stall by Firmware



Notes: 1. Pre-write (clearing data in the block to be erased to 0) is not required.
2. x, y, z, a, b, g, e, h, q, and N are shown in section 24.8, Flash Memory Characteristics.
3. Veryfy data is read in 16 bits.
4. Only 1 bit in the EBR register must be set. Two or more bits in EBR cannot be set.
5. Erasure is performed in block units. To erase multiple blocks, each block must be erased sequentially.

Figure 19.12 Erase/Erase-Verify Flowchart

Register Name	Power-on Reset	Manual Reset	High-Speed	Medium-Speed	Sleep	Module Stop	Software Standby	Hardware Standby	Module
UIER1	Initialized*	—	—	—	—	—	—	Initialized	USB
UIER2	Initialized*	—	—	—	—	—	—	Initialized	
UIER3	Initialized*	—	—	—	—	—	—	Initialized	
UISR0	Initialized*	—	—	—	—	—	—	Initialized	
UISR1	Initialized*	—	—	—	—	—	—	Initialized	
UISR2	Initialized*	—	—	—	—	—	—	Initialized	
UISR3	Initialized*	—	—	—	—	—	—	Initialized	
UDSR	Initialized*	—	—	—	—	—	—	Initialized	
UCVR	Initialized*	—	—	—	—	—	—	Initialized	
UTSRH	Initialized*	—	—	—	—	—	—	Initialized	
UTSRL	Initialized*	—	—	—	—	—	—	Initialized	
UTSTR0	Initialized*	—	—	—	—	—	—	Initialized	
UTSTR1	Initialized*	—	—	—	—	—	—	Initialized	
UTSTR2	Initialized*	—	—	—	—	—	—	Initialized	
UTSTRB	Initialized*	—	—	—	—	—	—	Initialized	
UTSTRC	Initialized*	—	—	—	—	—	—	Initialized	
UTSTRD	Initialized*	—	—	—	—	—	—	Initialized	
UTSTRE	Initialized*	—	—	—	—	—	—	Initialized	
UTSTRF	Initialized*	—	—	—	—	—	—	Initialized	
MRA	—	—	—	—	—	—	—	—	DTC
SAR	—	—	—	—	—	—	—	—	
MRB	—	—	—	—	—	—	—	—	
DAR	—	—	—	—	—	—	—	—	
CRA	—	—	—	—	—	—	—	—	
CRB	—	—	—	—	—	—	—	—	
DADR_0	Initialized	Initialized	—	—	—	—	—	Initialized	D/A
DADR_1	Initialized	Initialized	—	—	—	—	—	Initialized	
DACR	Initialized	Initialized	—	—	—	—	—	Initialized	
SCRX	Initialized	Initialized	—	—	—	—	—	Initialized	FLASH
SBYCR	Initialized	Initialized	—	—	—	—	—	Initialized	SYSTEM
SYSCR	Initialized	Initialized	—	—	—	—	—	Initialized	
SCKCR	Initialized	Initialized	—	—	—	—	—	Initialized	
MDCR	Initialized	—	—	—	—	—	—	Initialized	
MSTPCRA	Initialized	Initialized	—	—	—	—	—	Initialized	
MSTPCRB	Initialized	Initialized	—	—	—	—	—	Initialized	SYSTEM
MSTPCRC	Initialized	Initialized	—	—	—	—	—	Initialized	

Note: * The USB registers are no initialized by a power-on reset triggered by the WDT.

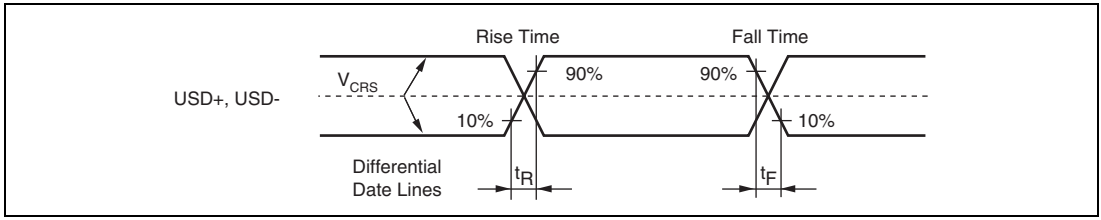


Figure 25.24 Data Signal Timing

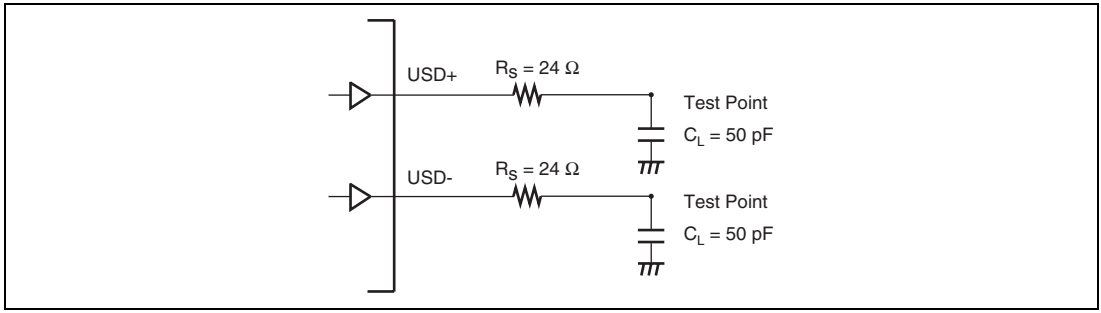


Figure 25.25 Test Load Circuit

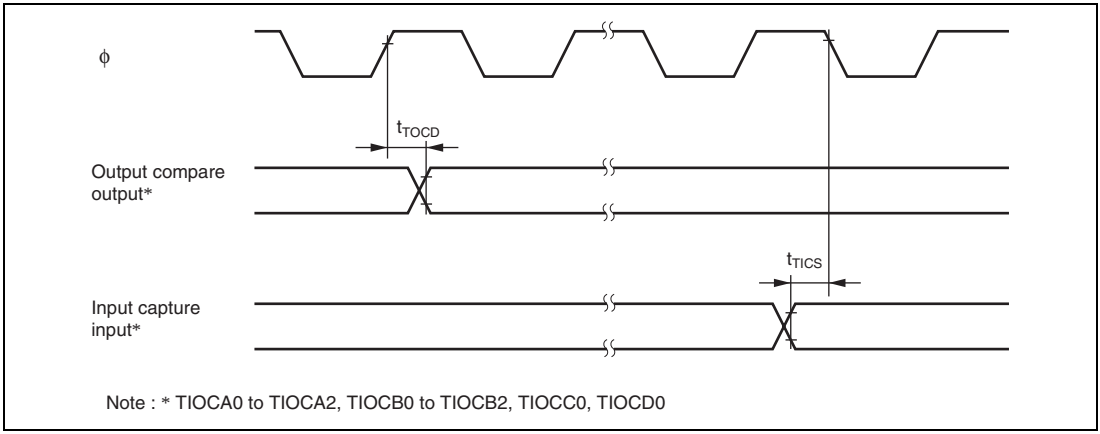


Figure 26.13 TPU Input/Output Timing

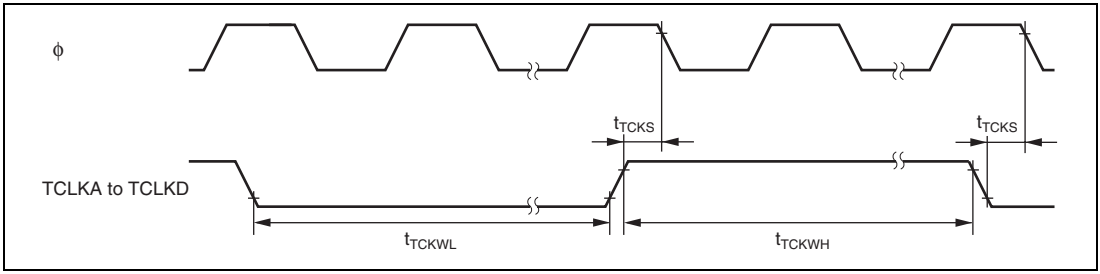


Figure 26.14 TPU Clock Input Timing

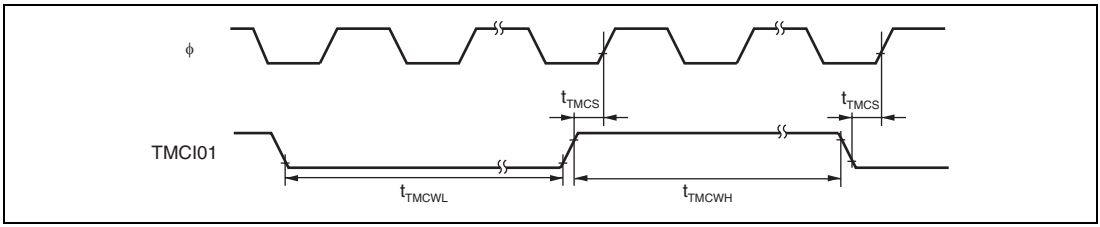


Figure 26.15 8-bit Timer Output Timing

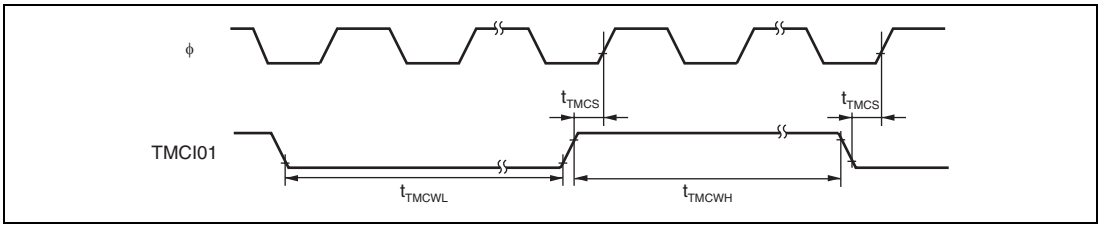


Figure 26.16 8-bit Timer Clock Input Timing

Legend:

H: High level

L: Low level

T: High impedance

keep: Input port level is high impedance, and output port level is retained.

DDR: Data direction register

OPE: Output port enable

WAITE: Wait port enable

BRLE: Bus release enable

Note: * L (address input) in mode 4 or 5