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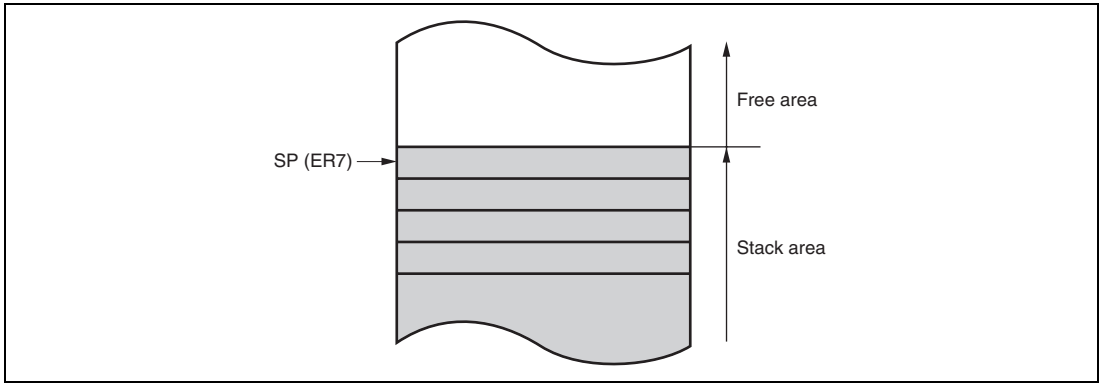


Figure 2.8 Stack

2.4.2 Program Counter (PC)

This 24-bit counter indicates the address of the next instruction the CPU will execute. The length of all CPU instructions is two bytes (one word), so the least significant PC bit is ignored (When an instruction is fetched, the least significant PC bit is regarded as 0).

2.4.3 Extended Control Register (EXR)

EXR is an 8-bit register that manipulates the LDC, STC, ANDC, ORC, and XORC instructions. When these instructions except for the STC instruction is executed, all interrupts including NMI will be masked for three states after execution is completed.

Bit	Bit Name	Initial Value	R/W	Description
7	T	0	R/W	Trace Bit When this bit is set to 1, a trace exception is generated each time an instruction is executed. When this bit is cleared to 0, instructions are executed in sequence.
6 to 3	—	All 1	—	Reserved These bits are always read as 1.
2 to 0	I2 I1 I0	1	R/W	These bits designate the interrupt mask level (0 to 7). For details, refer to section 5, Interrupt Controller.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R/W	Reserved The write value should always be 0.
6	—	0	—	Reserved This bit is always read as 0 and cannot be modified.
5	INTM1	0	R/W	These bits select the control mode of the interrupt controller. For details of the interrupt control modes, see section 5.6, Interrupt Control Modes and Interrupt Operation. 00: Interrupt control mode 0 01: Setting prohibited 10: Interrupt control mode 2 11: Setting prohibited
4	INTM0	0	R/W	
3	NMIEG	0	R/W	NMI Edge Select Selects the valid edge of the NMI interrupt input. 0: An interrupt is requested at the falling edge of NMI input 1: An interrupt is requested at the rising edge of NMI input
2	MRESE	0	R/W	Manual reset Select Enables or disables the $\overline{\text{MRES}}$ pin input. 0: The $\overline{\text{MRES}}$ pin input (manual reset) is disabled 1: The $\overline{\text{MRES}}$ pin input (manual reset) is enabled The $\overline{\text{MRES}}$ input pin can be used.
1	—	0	—	Reserved This bit is always read as 0 and cannot be modified.
0	RAME	1	R/W	RAM Enable Enables or disables the on-chip RAM. The RAME bit is initialized when the reset status is released. 0: On-chip RAM is disabled 1: On-chip RAM is enabled

3.3 Operating Mode Descriptions

3.3.1 Mode 4

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is disabled.

Pins P13 to P10, and ports A, B, and C function as an address bus, ports D and E function as a data bus, and part of port F carries bus control signals.

Pins P13 to P11 function as input ports immediately after a reset. Pin 10 and ports A and B function as address (A20 to A8) outputs immediately after a reset. Address (A23 to A21) output can be enabled or disabled by bits AE3 to AE0 in the pin function control register (PFCR) regardless of the corresponding data direction register (DDR) values. Pins for which address output is disabled among pins P13 to P10 and in ports A and B become port outputs when the corresponding DDR bits are set to 1.

Port C always has an address (A7 to A0) output function.

The initial bus mode after a reset is 16 bits, with 16-bit access to all areas. However, note that if 8-bit access is designated by the bus controller for all areas, the bus mode switches to 8 bits.

3.3.2 Mode 5

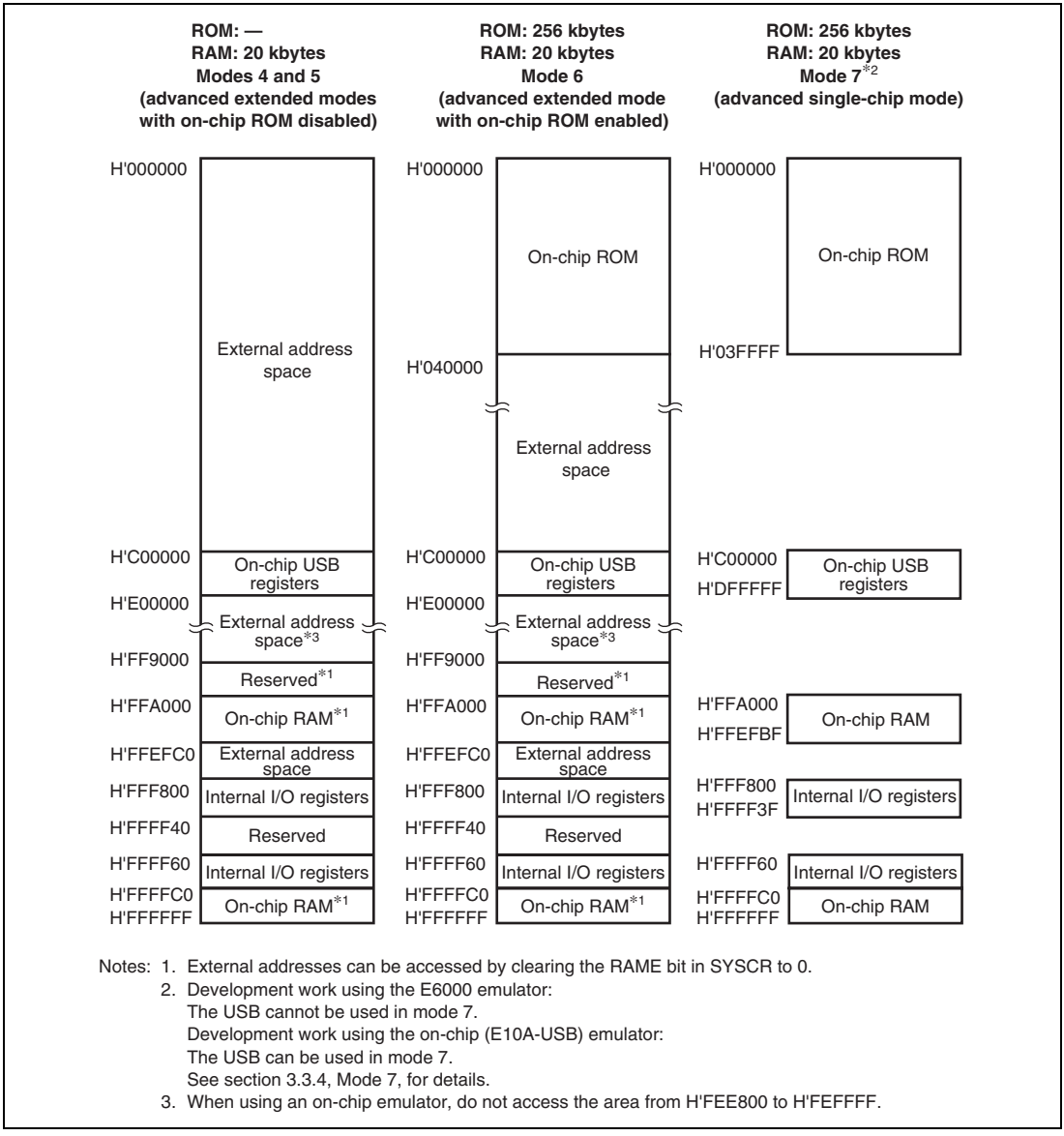
The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is disabled.

Pins P13 to P10, and ports A, B, and C function as an address bus, ports D and E function as a data bus, and part of port F carries bus control signals.

Pins P13 to P11 function as input ports immediately after a reset. Pin 10 and ports A and B function as address (A20 to A8) outputs immediately after a reset. Address (A23 to A21) output can be enabled or disabled by bits AE3 to AE0 in the pin function control register (PFCR) regardless of the corresponding data direction register (DDR) values. Pins for which address output is disabled among pins P13 to P10 and in ports A and B become port outputs when the corresponding DDR bits are set to 1.

Port C always has an address (A7 to A0) output function.

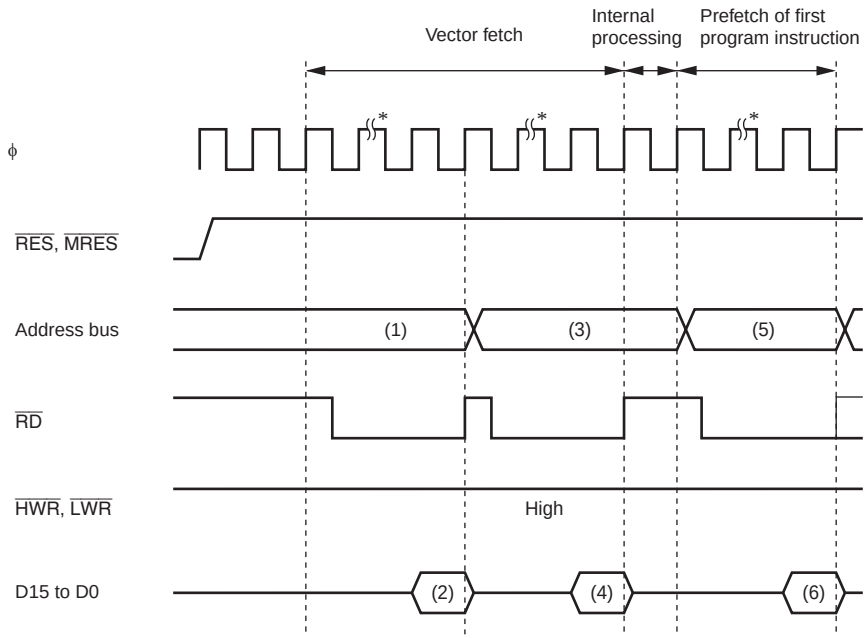
The initial bus mode after a reset is 8 bits, with 8-bit access to all areas. However, note that if 16-bit access is designated by the bus controller for any area, the bus mode switches to 16 bits and port E becomes a data bus.



Notes: 1. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
2. Development work using the E6000 emulator:
The USB cannot be used in mode 7.
Development work using the on-chip (E10A-USB) emulator:
The USB can be used in mode 7.
See section 3.3.4, Mode 7, for details.
3. When using an on-chip emulator, do not access the area from H'FEE800 to H'FEFFFF.

Figure 3.4 Memory Map in Each Operating Mode for HD64F2215R, HD64F2215RU, HD64F2215T, HD64F2215TU and HD64F2215CU

Figures 4.1 and 4.2 show examples of the reset sequence.



(1) (3) Reset exception handling vector address (for power-on reset, (1) = H'000000, (3) = H'000002; for manual reset, (1) = H'000004, (3) = H'000006)
(2) (4) Start address (contents of reset exception handling vector address)
(5) Start address ((5) = (2) (4))
(6) First program instruction

Note: * Three program wait states are inserted.

Figure 4.1 Reset Sequence (Mode 4)

4.8 Notes on Use of the Stack

When accessing word data or longword data, this LSI assumes that the lowest address bit is 0. The stack should always be accessed by word transfer instruction or longword transfer instruction, and the value of the stack pointer (SP: ER7) should always be kept even. Use the following instructions to save registers:

PUSH.W Rn (or MOV.W Rn, @-SP)
PUSH.L ERn (or MOV.L ERn, @-SP)

Use the following instructions to restore registers:

POP.W Rn (or MOV.W @SP+, Rn)
POP.L ERn (or MOV.L @SP+, ERn)

Setting SP to an odd value may lead to a malfunction. Figure 4.4 shows an example of what happens when the SP value is odd.

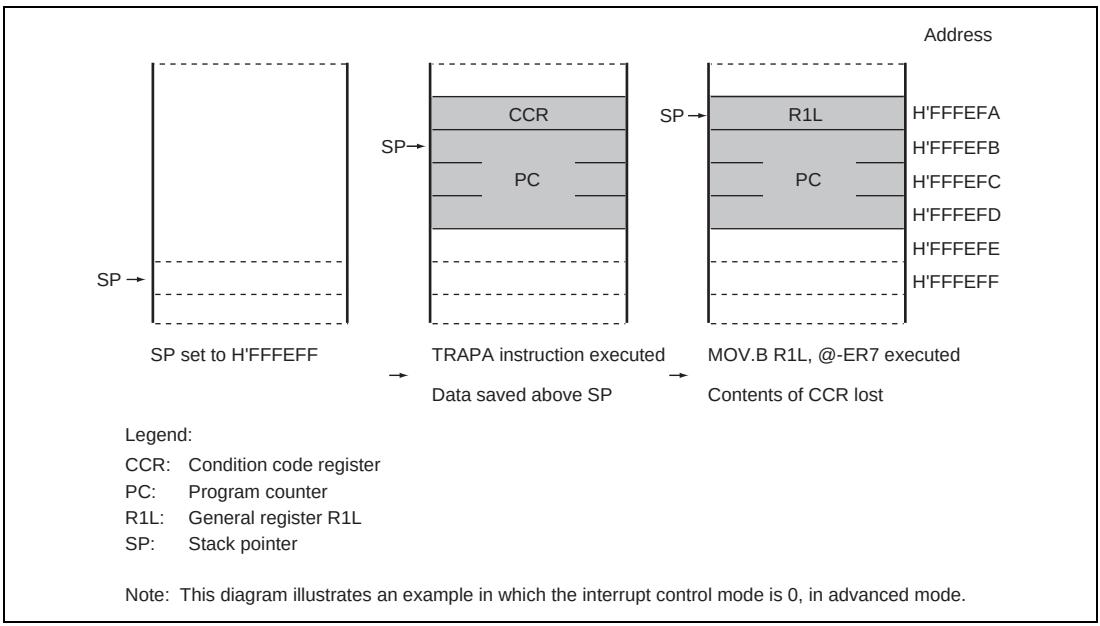


Figure 4.4 Operation when SP Value Is Odd

5.7 Usage Notes

5.7.1 Contention between Interrupt Generation and Disabling

When an interrupt enable bit is cleared to 0 to disable interrupts, the disabling becomes effective after execution of the instruction.

When an interrupt enable bit is cleared to 0 by an instruction such as BCLR or MOV, if an interrupt is generated during execution of the instruction, the interrupt concerned will still be enabled on completion of the instruction, and so interrupt exception handling for that interrupt will be executed on completion of the instruction. However, if there is an interrupt request of higher priority than that interrupt, interrupt exception handling will be executed for the higher-priority interrupt, and the lower-priority interrupt will be ignored.

The same also applies when an interrupt source flag is cleared to 0.

Figure 5.8 shows an example in which the TGIEA bit in the TPU's TIER_0 is cleared to 0.

The above contention will not occur if an enable bit or interrupt source flag is cleared to 0 while the interrupt is masked.

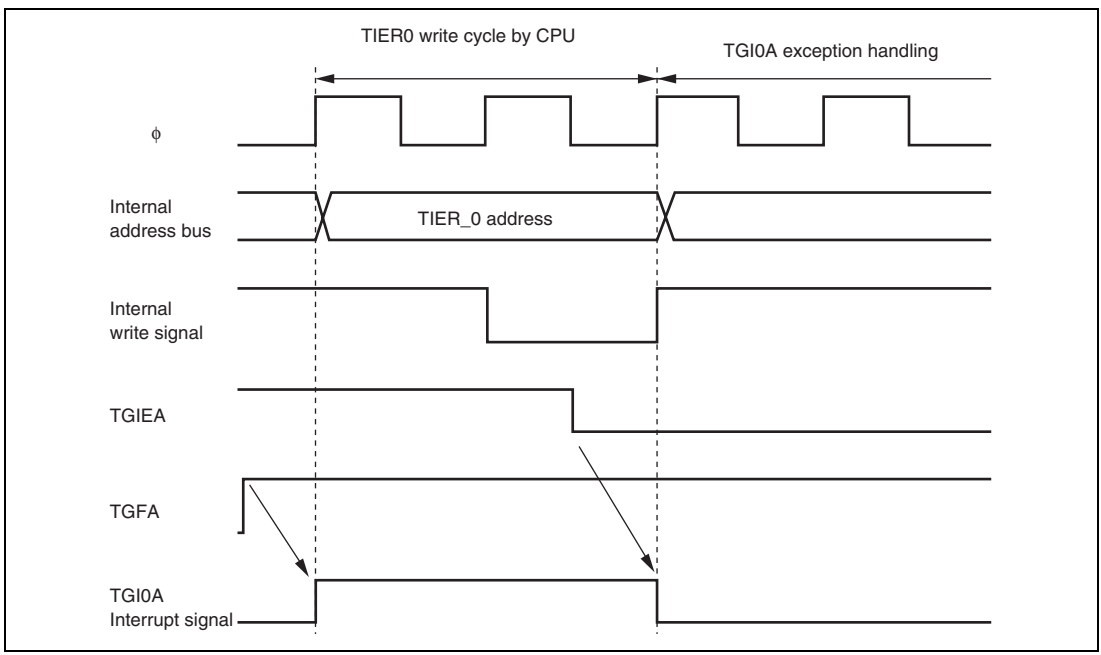


Figure 5.8 Contention between Interrupt Generation and Disabling

7.2 Register Configuration

The DMAC registers are listed below.

- Memory address register 0A (MAR0A)
- I/O address register 0A (IOAR0A)
- Transfer count register 0A (ETCR0A)
- Memory address register 0B (MAR0B)
- I/O address register 0B (IOAR0B)
- Transfer count register 0B (ETCR0B)
- Memory address register 1A (MAR1A)
- I/O address register 1A (IOAR1A)
- Transfer count register 1A (ETCR1A)
- Memory address register 1B (MAR1B)
- I/O address register 1B (IOAR1B)
- Transfer count register 1B (ETCR1B)
- DMA write enable register (DMAWER)
- DMA control register 0A (DMACR0A)
- DMA control register 0B (DMACR0B)
- DMA control register 1A (DMACR1A)
- DMA control register 1B (DMACR1B)
- DMA band control register (DMABCR)

The DMAC register functions differs depending on the address modes: short address mode and full address mode. The DMAC register functions are described in each address mode. Short address mode or full address mode can be selected for channels 1 and 0 independently by means of bits FAE1 and FAE0.

9.7.3 Port B Register (PORTB)

PORTB shows port B pin states.

Bit	Bit Name	Initial Value	R/W	Description
7	PB7	—*	R	If the port B read is performed while PBDDR bits are set to 1, the PBDR values are read. If a port B read is performed while PBDDR bits are cleared to 0, the pin states are read.
6	PB6	—*	R	
5	PB5	—*	R	
4	PB4	—*	R	
3	PB3	—*	R	
2	PB2	—*	R	
1	PB1	—*	R	
0	PB0	—*	R	

Note: * Determined by the status of pins PB7 to PB0.

9.7.4 Port B MOS Pull-Up Control Register (PBPCR)

PBPCR controls the on/off state of input pull-up MOS of port B.

Bit	Bit Name	Initial Value	R/W	Description
7	PB7PCR	0	R/W	When a pin functions specified to an input port, setting the corresponding bit to 1 turns on the input pull-up MOS for that pin.
6	PB6PCR	0	R/W	
5	PB5PCR	0	R/W	
4	PB4PCR	0	R/W	
3	PB3PCR	0	R/W	
2	PB2PCR	0	R/W	
1	PB1PCR	0	R/W	
0	PB0PCR	0	R/W	

Table 10.1 TPU Functions

Item		Channel 0	Channel 1	Channel 2
Count clock		φ/1	φ/1	φ/1
		φ/4	φ/4	φ/4
		φ/16	φ/16	φ/16
		φ/64	φ/64	φ/64
		TCLKA	φ/256	φ/1024
		TCLKB	TCLKA	TCLKA
		TCLKC	TCLKB	TCLKB
		TCLKD		TCLKC
General registers		TGRA_0	TGRA_1	TGRA_2
		TGRB_0	TGRB_1	TGRB_2
General registers/buffer registers		TGRC_0	not possible	not possible
		TGRD_0		
I/O pins		TIOCA0	TIOCA1	TIOCA2
		TIOCB0	TIOCB1	TIOCB2
		TIOCC0		
		TIOCD0		
Counter clear function		TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture
Compare match output	0 output	possible	possible	possible
	1 output	possible	possible	possible
	Toggle output	possible	possible	possible
Input capture function		possible	possible	possible
Synchronous operation		possible	possible	possible
PWM mode		possible	possible	possible
Phase counting mode		not possible	possible	possible
Buffer operation		possible	not possible	not possible

10.3.2 Timer Mode Register (TMDR)

The TMDR registers are used to set the operating mode for each channel. The TPU has three TMDR registers, one for each channel. TMDR register settings should be made only when TCNT operation is stopped.

Bit	Bit Name	Initial value	R/W	Description
7, 6	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
5	BFB	0	R/W	Buffer Operation B Specifies whether TGRB is to operate in the normal way, or TGRB and TGRD are to be used together for buffer operation. When TGRD is used as a buffer register. TGRD input capture/output compare is not generation. In channels 1 and 2, which have no TGRD, bit 5 is reserved. It is always read as 0 and cannot be modified. 0: TGRB operates normally 1: TGRB and TGRD used together for buffer operation
4	BFA	0	R/W	Buffer Operation A Specifies whether TGRA is to operate in the normal way, or TGRA and TGRC are to be used together for buffer operation. When TGRC is used as a buffer register, TGRC input capture/output compare is not generated. In channels 1 and 2, which have no TGRC, bit 4 is reserved. It is always read as 0 and cannot be modified. 0: TGRA operates normally 1: TGRA and TGRC used together for buffer operation
3	MD3	0	R/W	Modes 3 to 0 These bits are used to set the timer operating mode. MD3 is a reserved bit. In a write, the write value should always be 0. See table 10.8, for details.
2	MD2	0	R/W	
1	MD1	0	R/W	
0	MD0	0	R/W	

Example of PWM Mode Setting Procedure: Figure 10.21 shows an example of the PWM mode setting procedure.

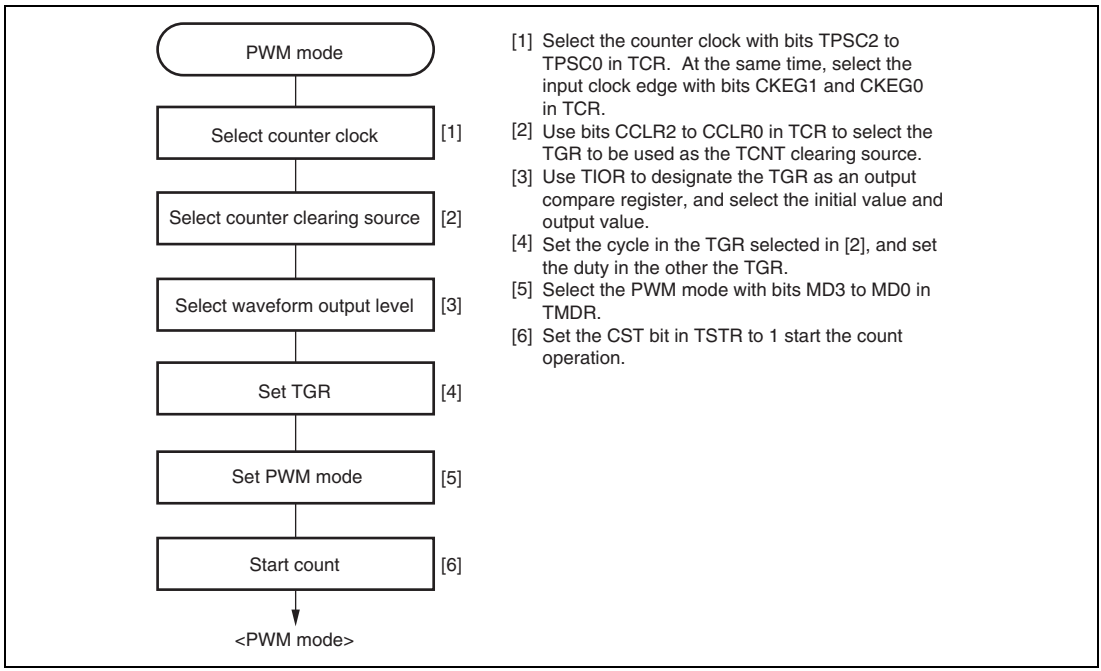


Figure 10.21 Example of PWM Mode Setting Procedure

Examples of PWM Mode Operation: Figure 10.22 shows an example of PWM mode 1 operation.

In this example, TGRA compare match is set as the TCNT clearing source, 0 is set for the TGRA initial output value and output value, and 1 is set as the TGRB output value. In this case, the value set in TGRA is used as the period, and the values set in TGRB registers as the duty.

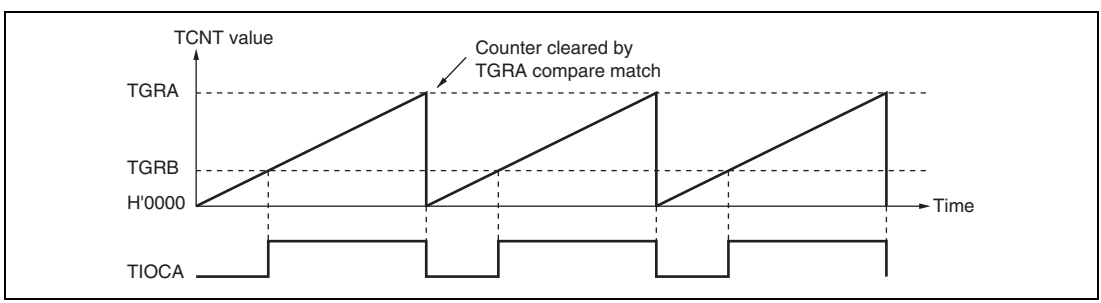


Figure 10.22 Example of PWM Mode Operation (1)

12.3.2 Timing of Setting of Watchdog Timer Overflow Flag (WOVF)

With WDT0, the WOVF bit in RSTCSR is set to 1 if TCNT overflows in watchdog timer mode. If TCNT overflows while the RSTE bit in RSTCSR is set to 1, an internal reset signal is generated for the entire chip. This timing is illustrated in figure 12.3.

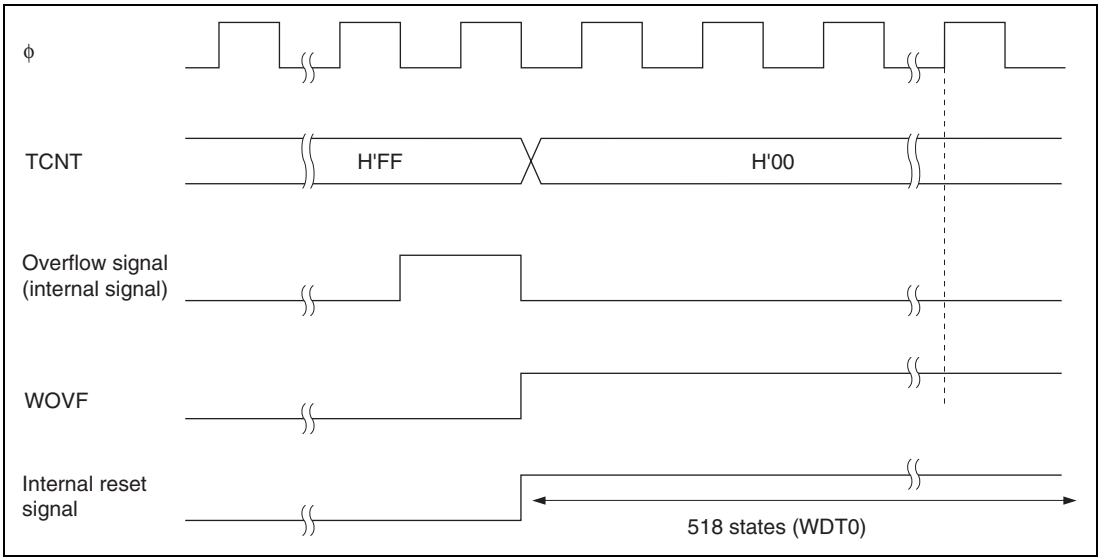


Figure 12.3 Timing of WOVF Setting

a 1-bit transfer interval) can be selected. For details, see section 13.7.5, Receive Data Sampling Timing and Reception Margin. Tables 13.5 and 13.7 show the maximum bit rates with external clock input.

When the ABCS bit in SCI_0's serial extended mode register (SEMR) is set to 1 in asynchronous mode, the maximum bit rates are twice those shown in table 13.3.

Table 13.3 BRR Settings for Various Bit Rates (Asynchronous Mode)

Bit Rate (bit/s)	Operating Frequency ϕ (MHz)											
	2			2.097152			2.4576			3		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	1	141	0.03	1	148	–0.04	1	174	–0.26	1	212	0.03
150	1	103	0.16	1	108	0.21	1	127	0.00	1	155	0.16
300	0	207	0.16	0	217	0.21	0	255	0.00	1	77	0.16
600	0	103	0.16	0	108	0.21	0	127	0.00	0	155	0.16
1200	0	51	0.16	0	54	–0.70	0	63	0.00	0	77	0.16
2400	0	25	0.16	0	26	1.14	0	31	0.00	0	38	0.16
4800	0	12	0.16	0	13	–2.48	0	15	0.00	0	19	–2.34
9600	—	—	—	—	6	–2.48	0	7	0.00	0	9	–2.34
19200	—	—	—	—	—	—	0	3	0.00	0	4	–2.34
31250	0	1	0.00	—	—	—	—	—	—	0	2	0.00
38400	—	—	—	—	—	—	0	1	0.00	—	—	—

EPINFO Data Settings Based on Bluetooth Standard

No.	Register Name	Address	Corresponding Transfer Mode[*1]	UEPIRn_0 to UEPIRn_4 Settings[*2]	UEPIRn_0	UEPIRn_1	UEPIRn_2	UEPIRn_3	UEPIRn_4
18	UEPIR17_0 to UEPIR17_4	H'C00055 to H'C0059	Specific to Isoch out transfer	B'[0000]_01_[00]_[000]_01_0_ [0000000000]_0000000000010001[*5*6]	H'04	H'08	H'00	H'00	H'11
19	UEPIR18_0 to UEPIR18_4	H'C0005A to H'C005E	Specific to Isoch in transfer	B'[0000]_01_[00]_[000]_01_1_ [0000000000]_0000000000010010[*5*6]	H'04	H'0C	H'00	H'00	H'12
20	UEPIR19_0 to UEPIR19_4	H'C0005F to H'C0063	Specific to Isoch out transfer	B'[0000]_01_[00]_[000]_01_0_ [0000000000]_0000000000010011[*5*6]	H'04	H'08	H'00	H'00	H'13
21	UEPIR20_0 to UEPIR20_4	H'C00064 to H'C0068	Specific to Bulk in transfer	B'[0101]_01_[01]_[000]_10_1_ [0001000000]_0000000000010100[*4]	H'55	H'14	H'40	H'00	H'14
22	UEPIR21_0 to UEPIR21_4	H'C00069 to H'C006D	Specific to Bulk out transfer	B'[0110]_01_[01]_[000]_10_0_ [0001000000]_0000000000010101[*4]	H'65	H'10	H'40	H'00	H'15
23	UEPIR22_0 to UEPIR22_4	H'C0006E to H'C0072	Specific to Interrupt in transfer	B'[0100]_01_[01]_[000]_11_1_ [0001000000]_0000000000010110[*3]	H'45	H'1C	H'40	H'00	H'16

Notes:
1. Each endpoint is optimized by the hardware specific for the transfer mode. The transfer mode shown in table 15.8 must be specified. (D28 and D27 for all EPINFO data items must e specified as shown in table 15.8.)
2. Data indicated within parentheses [ ] can be modified. Data other than that within parentheses [ ] must be specified as shown in table 15.8.
3. Maximum packet size of Interrupt transfer must be from 0 to 64.
4. Maximum packet size of Bulk transfer must be 64 when used or 0 when unused.
5. Maximum packet size of Isochronous transfer must be from 0 to 128. Endpoint number of Isochronous_in can differ from that of Isochronous_out. However, note that endpoint numbers of all Isochronous_in must be the same. Endpoint numbers of all Isochronous_out must also be the same.
6. Maximum packet size of the unused endpoint must be 0.

Example in which flash memory block area EB0 is overlapped is shown in figure 19.10.

1. The RAM area to be overlapped is fixed at a 4-kbyte area in the range of H'FFD000 to H'FFDFFF.
2. The flash memory area to overlap is selected by RAMER from a 4-kbyte area among one of the EB0 to EB7 blocks.
3. The overlapped RAM area can be accessed from both the flash memory addresses and RAM addresses.
4. When the RAMS bit in RAMER is set to 1, program/erase protection is enabled for all flash memory blocks (emulation protection). In this state, setting the P1 or E1 bit in FLMCR1 to 1 does not cause a transition to program mode or erase mode.
5. A RAM area cannot be erased by execution of software in accordance with the erase algorithm.
6. Block area EB0 contains the vector table. When performing RAM emulation, the vector table is needed in the overlap RAM.

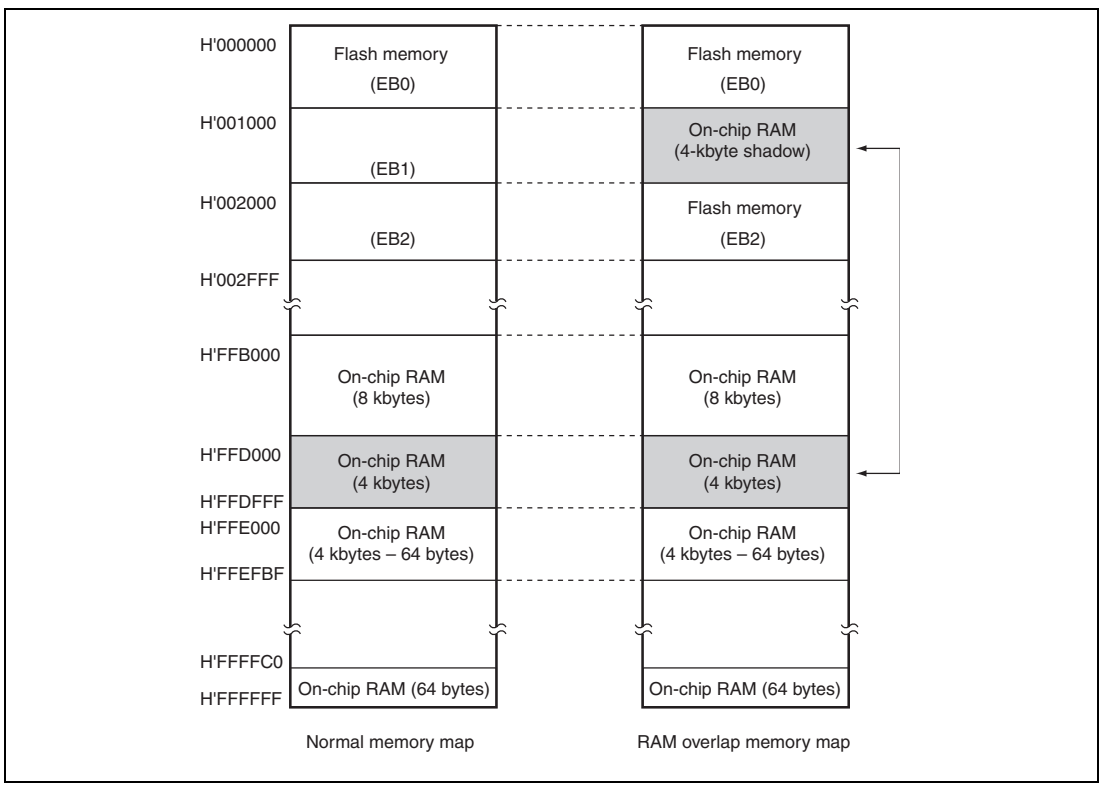


Figure 19.10 Example of RAM Overlap Operation

Register Name	Abbreviation	Number of Bits	Address	Data Bus Width	Number of Access States	Module
Timer general register B_0	TGRB_0	16	H'FF1A	16	2	TPU_0
Timer general register C_0	TGRC_0	16	H'FF1C	16	2	
Timer general register D_0	TGRD_0	16	H'FF1E	16	2	
Timer control register_1	TCR_1	8	H'FF20	16	2	TPU_1
Timer mode register_1	TMDR_1	8	H'FF21	16	2	
Timer I/O control register _1	TIOR_1	8	H'FF22	16	2	
Timer interrupt enable register _1	TIER_1	8	H'FF24	16	2	
Timer status register_1	TSR_1	8	H'FF25	16	2	
Timer counter_1	TCNT_1	16	H'FF26	16	2	
Timer general register A_1	TGRA_1	16	H'FF28	16	2	
Timer general register B_1	TGRB_1	16	H'FF2A	16	2	
Timer control register_2	TCR_2	8	H'FF30	16	2	TPU_2
Timer mode register_2	TMDR_2	8	H'FF31	16	2	
Timer I/O control register 2	TIOR_2	8	H'FF32	16	2	
Timer interrupt enable register 2	TIER_2	8	H'FF34	16	2	
Timer status register_2	TSR_2	8	H'FF35	16	2	
Timer counter_2	TCNT_2	16	H'FF36	16	2	
Timer general register A_2	TGRA_2	16	H'FF38	16	2	
Timer general register B_2	TGRB_2	16	H'FF3A	16	2	
DMA write enable register	DMAWER	8	H'FF60	8	2	DMAC
DMA control register 0A	DMACR0A	8	H'FF62	16	2	
DMA control register 0B	DMACR0B	8	H'FF63	16	2	
DMA control register 1A	DMACR1A	8	H'FF64	16	2	
DMA control register 1B	DMACR1B	8	H'FF65	16	2	
DMA band control register	DMABCR	16	H'FF66	16	2	
Timer control register_0	TCR_0	8	H'FF68	8	2	TMR_0
Timer control register_1	TCR_1	8	H'FF69	8	2	TMR_1
Timer control/status register_0	TCSR_0	8	H'FF6A	8	2	TMR_0
Timer control/status register_1	TCSR_1	8	H'FF6B	8	2	TMR_1
Time constant register A0	TCORA_0	8	H'FF6C	8	2	TMR_0
Time constant register A1	TCORA_1	8	H'FF6D	8	2	TMR_1
Time constant register B0	TCORB_0	8	H'FF6E	8	2	TMR_0

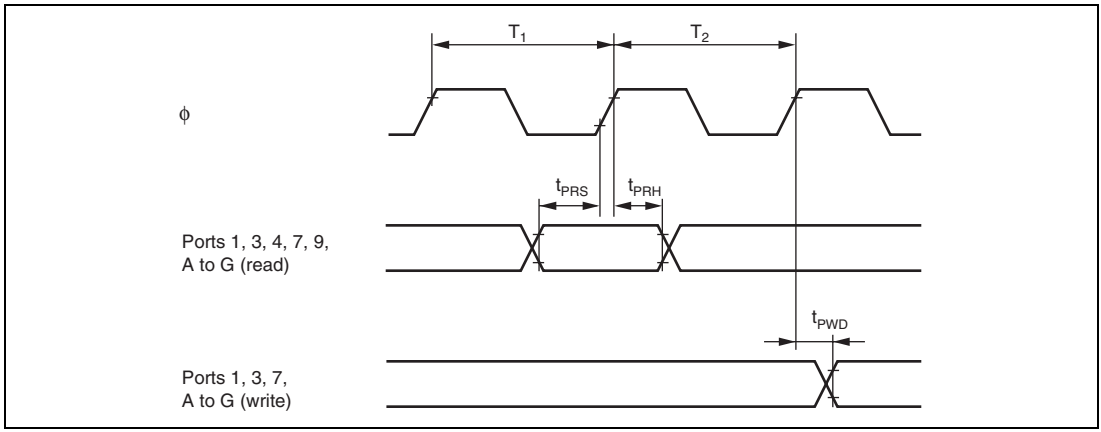


Figure 24.12 I/O Port Input/Output Timing

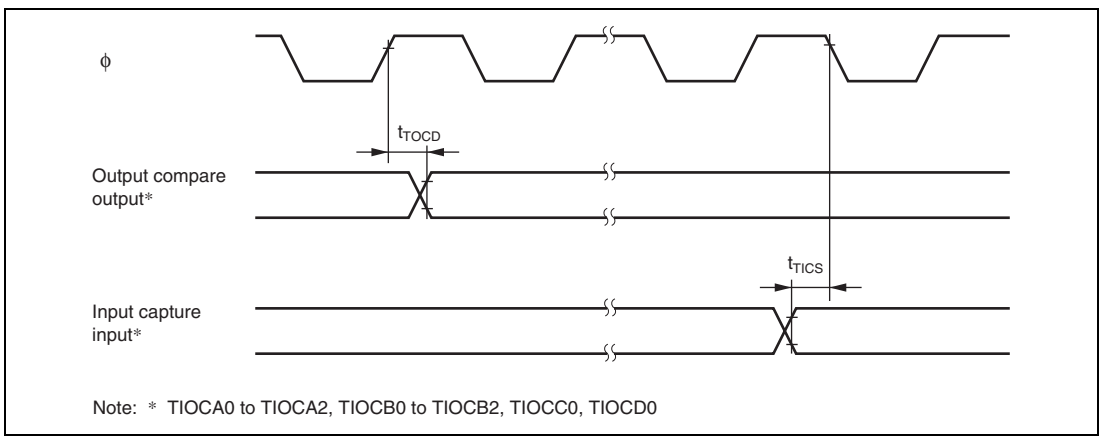


Figure 24.13 TPU Input/Output Timing

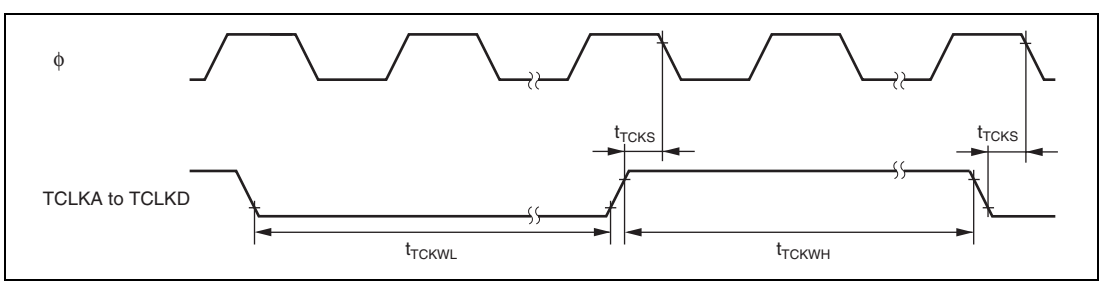
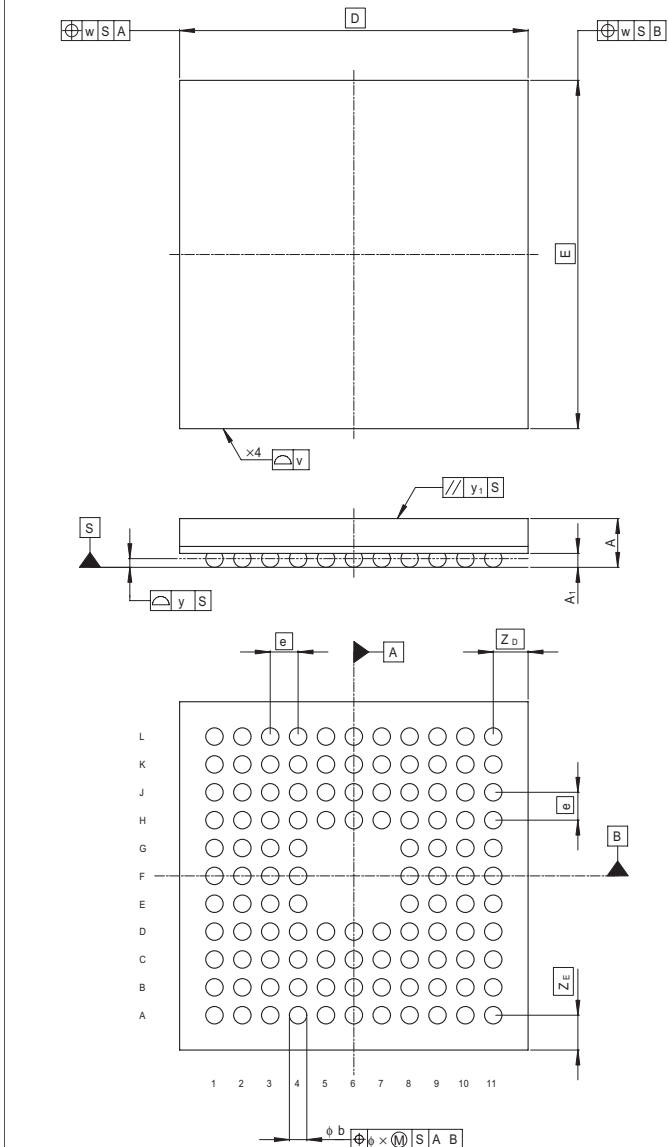


Figure 24.14 TPU Clock Input Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA112-10x10-0.80	PLBG0112GA-A	BP-112/BP-112V	0.3g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.00	—
E	—	10.00	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	1.00	—
Z_E	—	1.00	—

Figure C.2 BP-112, BP-112V Package Dimension

H8S/2215 Group
User's Manual: Hardware

Renesas Electronics Corporation

REJ09B0140-0900